

iC-MSC SIN/COS SIGNAL CONDITIONER WITH FAIL-SAFE 1 Vpp LINE DRIVER



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FEATURES

- ◆ PGA inputs for differential or single-ended signals up to 500 kHz
- ◆ Unity gain capable for high output sensors
- ◆ Selectable adaptation to voltage or current signals
- ◆ Flexible pin assignment due to signal path multiplexer
- ◆ Sine/Cosine signal conditioning for offset, amplitude and phase
- ◆ Separate index signal conditioning
- ◆ Short-circuit-proof and reverse polarity tolerant output drivers (1 Vpp to 100 Ω)
- ◆ Output signal stabilization by advanced sensor control with adjustable deadband
- ◆ Signal and system monitoring with configurable alarm output
- ◆ Supply voltage monitoring with integrated switches for reversed-polarity-safe systems
- ◆ Excessive temperature protection with sensor calibration
- ◆ I²C multi-master interface for in-circuit calibration
- ◆ Supply from 4.3 to 5.5 V, operation within -40 to +125 °C
- ◆ Verifiable chip release code
- ◆ Pin-compatible interpolation ICs available (iC-MQ, iC-PI etc.)

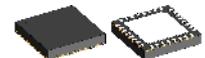
APPLICATIONS

- ◆ Programmable sensor interface for optical and magnetic position sensors
- ◆ Linear gauges and incremental encoders
- ◆ Linear scales

PACKAGES

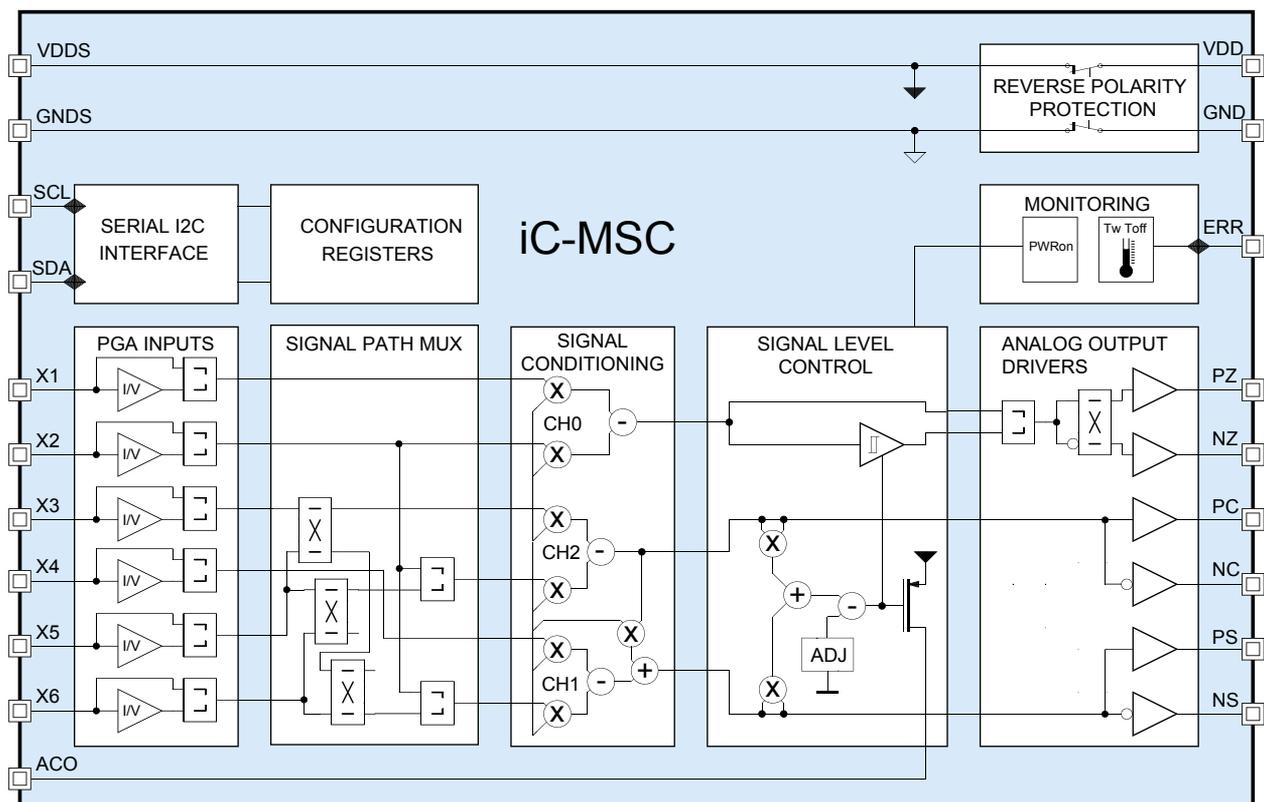


TSSOP20-TP
RoHS compliant



QFN32
5 mm x 5 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



iC-MSC SIN/COS SIGNAL CONDITIONER WITH FAIL-SAFE 1 Vpp LINE DRIVER



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DESCRIPTION

iC-MSC is a signal conditioner with analog line drivers for sine/cosine sensors which are used to determine positions in linear and angular encoders, for example.

Programmable instrumentation amplifiers with selectable gain levels allow differential or single-ended, referenced input signals; an external reference voltage can be connected to input X2 then operated as a reference input.

The modes of operation differentiate between high impedance (V-Modes) and low impedance (I-Modes). This adaptation of the iC to voltage or current signals enables MR sensor bridges or photosensors to be directly connected to the device.

The integrated signal conditioning unit allows signal amplitudes and offset voltages to be calibrated accurately and any phase error between the sine and cosine signals to be corrected. The channel for the index signal can be configured separately. The index signal is then output either as an analog or a differential square-wave signal (with low/high levels analogous to the sine/cosine amplitude).

A control signal is generated from the conditioned signals which can track the transmitting LED of optical encoders via the integrated 50 mA driver stage (output ACO). If MR sensors are connected this driver stage can also track the power supply of the measuring bridges.

By tracking the sensor's energy supply any temperature and aging effects are compensated for, the input signals stabilized and the exact calibration of the input signals is maintained. This enables a constantly accurate signal for the subsequent device, a PLC or motion controller, across the entire operating temperature range.

If control limits are reached, these can be indicated at the maskable error pin ERR. Faults such as signal loss due to wire breakage, short circuiting, dirt or aging, for example, can be detected and indicated.

iC-MSC includes system diagnosis functions which check whether the sensor is working properly or not. For all error events the user can select whether the fault is indicated at the pin ERR or whether the outputs should shutdown. At the same time errors can be stored in the EEPROM to enable failures to be diagnosed at a later stage. For encoder applications the sensor signal regarding signal level and the operating temperature can be monitored, for example, the latter using an adjustable on-chip sensor.

Display error pin ERR is bidirectional; a system fault recognized externally could also be used to shutdown the outputs.

iC-MSC is protected against reverse polarity and offers its monitored supply voltage to the external circuit, thus extending the protection to the system (for load currents up to 20 mA). Reverse polarity protection also covers the short-circuit-proof output drivers so that an unintentional faulty wiring during initial operation is tolerated.

On being activated the device configuration is loaded via the serial I²C interface from an external EEPROM and verified with a CRC. A microcontroller can also configure iC-MSC; the implemented interface is multi-master-capable and allows direct RAM access to configuration data.

General notice on application-specific programming

Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

For magnetic sensor systems: The chip's performance in application is impacted by system conditions like the quality of the magnetic target, field strength and stray fields, temperature and mechanical stress, sensor alignment and initial calibration.

For optical sensor systems: The chip's performance in application is impacted by system conditions like the quality of the optical target, the illumination, temperature and mechanical stress, sensor alignment and initial calibration.

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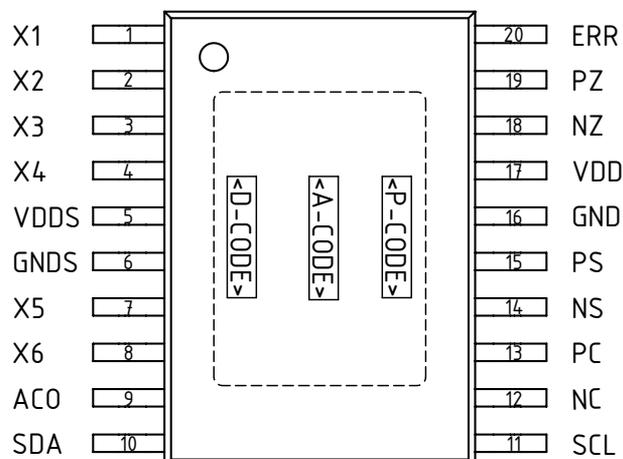
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PACKAGING INFORMATION

PIN CONFIGURATION TSSOP20-TP



PIN FUNCTIONS

No. Name Function

1	X1	Signal Input 1 (Index +)
2	X2	Signal Input 2 (Index -)
3	X3	Signal Input 3
4	X4	Signal Input 4
5	VDDS ¹	Switched Supply Output and Internal Analog Supply Voltage (reverse-polarity-proof, load 20 mA max.)
6	GNDS ¹	Switched Ground (reverse-polarity-proof)
7	X5	Signal Input 5
8	X6	Signal Input 6
9	ACO	Signal Level Control, high-side current source output
10	SDA	Serial Configuration Interface, data line
11	SCL	Serial Configuration Interface, clock line
12	NC	Neg. Cosine Output
13	PC	Pos. Cosine Output
14	NS	Neg. Sine Output
15	PS	Pos. Sine Output
16	GND	Ground
17	VDD	+4.5 to +5.5 V Supply Voltage
18	NZ	Neg. Index Output
19	PZ	Pos. Index Output
20	ERR	Error Signal (In/Out), and Test Mode Trigger Input

TP² Thermal Pad (TSSOP20-TP)

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);

¹ It is advisable to connect a bypass capacitor of about 100 nF (up to 1 μ F max.) close to the chip's analog supply terminals.

² To improve heat dissipation the *thermal pad* of the package (bottom side) should be joined to an extended copper area which must have GNDS potential.

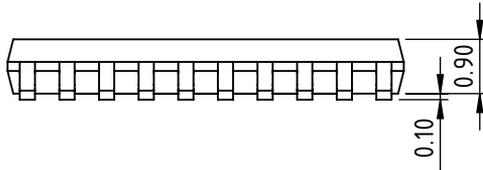
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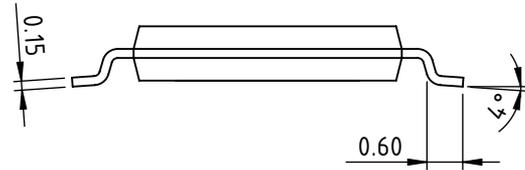
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PACKAGE DIMENSIONS : TSSOP20-TP

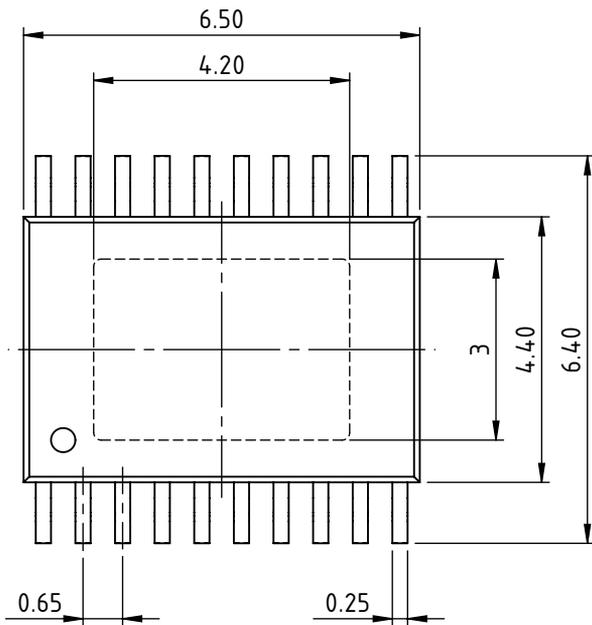
SIDE



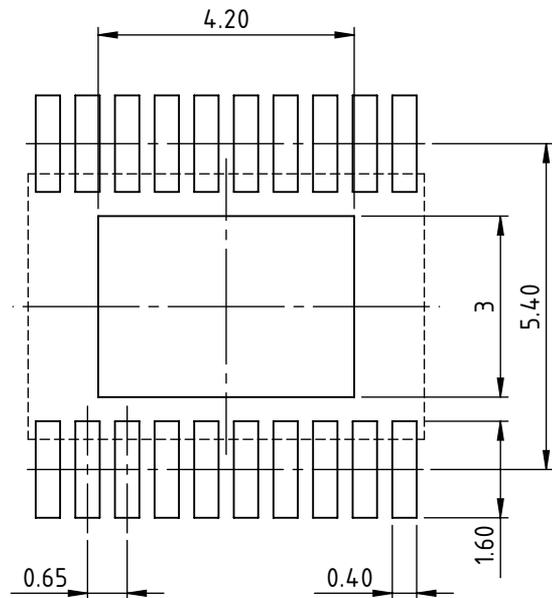
FRONT



TOP



RECOMMENDED PCB-FOOTPRINT



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-153

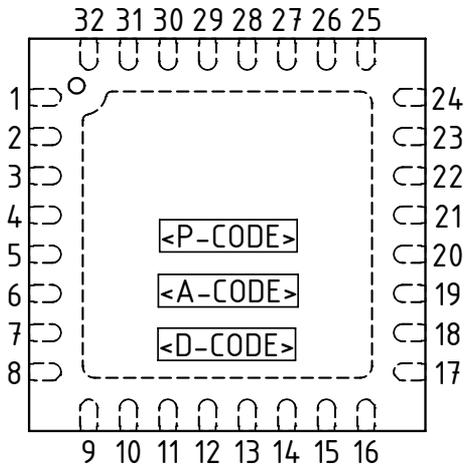
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PIN CONFIGURATION QFN32-5x5



PIN FUNCTIONS

No.	Name	Function
1, 2	n.c. ³	
3	ERR	Error Signal (In/Out), and Test Mode Trigger Input
4, 5	n.c. ³	
6	X1	Signal Input 1 (Index +)
7	X2	Signal Input 2 (Index -)
8, 9	n.c. ³	
10	X3	Signal Input 3
11	X4	Signal Input 4
12	VDD ^S 1	Switched Supply Output and Internal Analog Supply Voltage (reverse-polarity-proof, load 20 mA max.)
13	GNDS ¹	Switched Ground (reverse-polarity-proof)
14	X5	Signal Input 5
15	X6	Signal Input 6
16	n.c. ³	
17	ACO	Signal Level Control, high-side current source output
18	n.c. ³	
19	SDA	Serial Configuration Interface, data line
20, 21	n.c. ³	
22	SCL	Serial Configuration Interface, clock line
23, 24	n.c. ³	
25	NC	Neg. Cosine Output
26	PC	Pos. Cosine Output
27	NS	Neg. Sine Output
28	PS	Pos. Sine Output
29	GND	Ground
30	VDD	+4.5 to +5.5 V Supply Voltage
31	NZ	Neg. Index Output
32	PZ	Pos. Index Output
	BP ²	Backside Paddle

(top view) IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);

¹ It is advisable to connect a bypass capacitor of about 100 nF (up to 1 μF max.) close to the chip's analog supply terminals.

² To improve heat dissipation the backside paddle should be soldered and joined to an extended copper area, which must have GNDS potential.

³ Pin numbers marked n.c. are not connected.

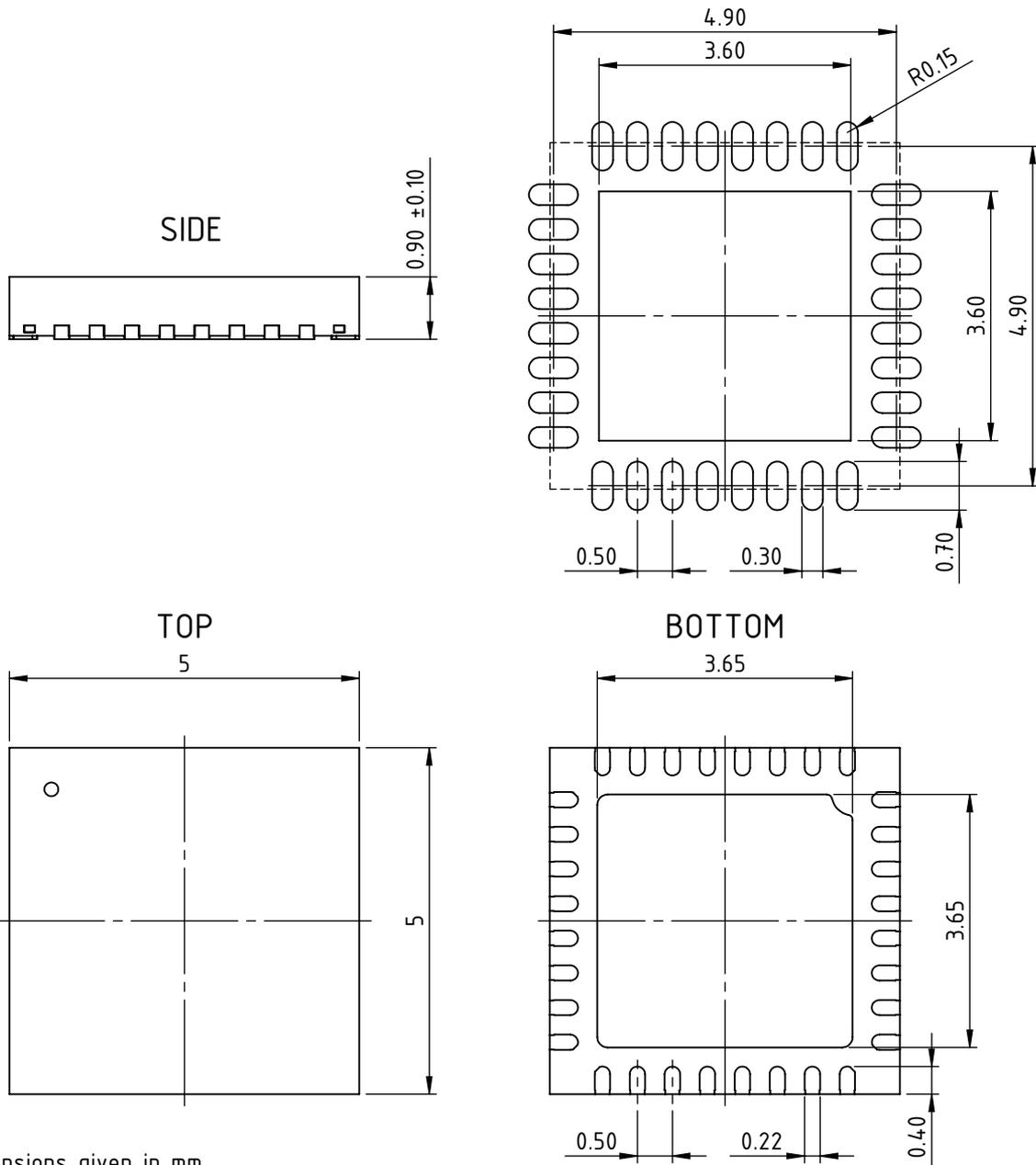
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PACKAGE DIMENSIONS : QFN32-5x5 (5 mm x 5 mm)

RECOMMENDED PCB-FOOTPRINT



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

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ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Limits		Unit
				Min.	Max.	
G001	V()	Voltage at VDD, PC, NC, PS, NS, PZ, NZ, ACO	relative to GND	-6	6	V
G002	V()	Voltage at ERR	relative to GND	-6	8	V
G003	V()	Pin-To-Pin Voltage between VDD, GND, PC, NC, PS, NS, PZ, NZ, ACO, ERR			6	V
G004	V()	Voltage at VDDS	no reversed polarity at VDD and GND		VDD	V
G005	V()	Voltage at GNDS relative to GND	no reversed polarity at VDD and GND	-0.3	+0.3	V
G006	V()	Voltage at X1...X6, SCL, SDA		-0.3	VDDS + 0.3	V
G007	I(VDD)	Current in VDD		-100	100	mA
G008	I()	Current in VDDS, GNDS		-50	50	mA
G009	I()	Current in X1...X6, SCL, SDA, ERR, PC, NC, PS, NS, PZ, NZ		-20	20	mA
G010	I(ACO)	Current in ACO		-100	20	mA
G011	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G012	P _{tot}	Permissible Power Dissipation	TSSOP20-TP, QFN32-5x5		400	mW
G013	T _j	Junction Temperature		-40	150	°C
G014	T _s	Storage Temperature Range		-40	150	°C
G015	V()	Voltage at VDDS	no reversed polarity at VDD and GND		VDD	V

THERMAL DATA

VDD = 4.3...5.5 V

Item No.	Symbol	Parameter	Conditions	Limits			Unit
				Min.	Typ.	Max.	
T01	T _a	Operating Ambient Temperature Range	iC-MSC TSSOP20-TP	-40		125	°C
			iC-MSC QFN32-5x5	-40		125	°C
T02	R _{thja}	Thermal Resistance Chip to Ambient	TSSOP20-TP surface mounted to PCB (incl. the thermal pad), according to JEDEC 51		35		K/W
T03	R _{thja}	Thermal Resistance Chip to Ambient	QFN32-5x5 surface mounted to PCB (incl. the backside paddle), according to JEDEC 51		40		K/W

All voltages are referenced to Pin GNDS unless otherwise stated.

All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

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ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, T_j = -40...140 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
Total Device							
001	VDD	Permissible Supply Voltage VDD versus GND	load current I(VDDS) up to 10 mA load current I(VDDS) up to 20 mA	4.3 4.5		5.5 5.5	V V
002	I(VDD)	Supply Current in VDD to GND	T _j = 27 °C, no load		25	50	mA
003	I(VDDS)	Permissible Load Current VDDS		-20		0	mA
004	Vc _{()hi}	Clamp Voltage hi at all pins				11	V
005	Vc _{()hi}	Clamp Voltage hi at inputs SCL, SDA	Vc _{()hi} = V() – V(VDDS), I() = 1 mA	0.4		1.5	V
006	Vc _{()hi}	Clamp Voltage hi at inputs X1...X6	Vc _{()hi} = V() – V(VDDS), I() = 4 mA	0.3		1.2	V
007	Vc _{()lo}	Clamp Voltage lo at all pins	I() = -4 mA	-1.2		-0.3	V
008	Irev(VDD)	Reverse-Polarity Current VDD vs. GND	V(VDD) = -5.5 V...-4.3 V	-1		1	mA
PGA Inputs and Signal Conditioning: X3...X6							
101	Vin _{()sig}	Permissible V-Mode Input Voltage Range	RIN12(3:0) = 0x01 (V-Mode 1:1) BIAS12 = 1, RIN12(3:0) = 0x09 (V-Mode 4:1) BIAS12 = 0, RIN12(3:0) = 0x09 (V-Mode 4:1)	0.75 0 0		VDDS - 1.5 VDDS VDDS - 1.5	V V V
102	Vin _{()diff}	Recommended Differential V-Mode Input Voltage	Vin _{()diff} = V(PXi) – V(NXi); RIN12(3:0) = 0 (V-Mode 1:1) RIN12(3:0) = 1 (V-Mode 4:1)	10 40		1500 6000	mV _{pp} mV _{pp}
103	Vin _{()os}	V-Mode Input Offset Voltage	referred to side of input, MODE(3:0) = 0x0 (normal), RIN12(3:0) = 0x01 (V-Mode 1:1); Max. gain: GR12, GF1, GF2 = max.	-500		+500	µV
105	Iin ₍₎	V-Mode Input Current	RIN12(3:0) = 0x01 (V-Mode 1:1)	-10		10	µA
106	Iin _{()sig}	Permissible I-Mode Input Current Range	BIAS12 = 1, RIN12(0) = 0 BIAS12 = 0, RIN12(0) = 0	10 -300		300 -10	µA µA
107	Rin ₍₎	I-Mode / V-Mode Input Resistance	referenced to VREFin, T _j = 27 °C; RIN12(3:0) = 0x00 RIN12(3:0) = 0x02 RIN12(3:0) = 0x04 RIN12(3:0) = 0x06 RIN12(3:0) = 0x09 (V-Mode 4:1)	1.1 1.6 2.2 3.2 16	1.7 2.5 3.5 4.9 20	2.1 3.0 4.2 6.0 24	kΩ kΩ kΩ kΩ kΩ
108	R2 ₍₎	I-Mode Conversion Resistor	referenced to VREFin, T _j = 27 °C; RIN12(3:0) = 0x00 RIN12(3:0) = 0x02 RIN12(3:0) = 0x04 RIN12(3:0) = 0x06 RIN12(3:0) = 0x09 (V-Mode 4:1)		1.6 2.3 3.2 4.6 5.0		kΩ kΩ kΩ kΩ kΩ
109	TCRin ₍₎	Temperature Coefficient Rin			0.15		%/K
110	VREFI ₍₎	Internal Reference Voltage VREF ₁₂	BIAS12 = 1, RIN12(0) = 0 BIAS12 = 0, RIN12(0) = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
111	G12	Selectable Gain Factors	RIN12(3:0) = 0x01, GR12, GF1, GF2 = 0x0 RIN12(3:0) = 0x01, GR12, GF1, GF2 = max. RIN12(3:0) = 0x09, GR12, GF1, GF2 = 0x0 RIN12(3:0) = 0x09, GR12, GF1, GF2 = max.		0.667 100		
112	ΔGdiff	Differential Gain Accuracy	calibration range 11 bit	-0.5		0.5	LSB
113	ΔGabs	Absolute Gain Accuracy	calibration range 11 bit, guaranteed monotony	-1		1	LSB
114	VOScal	Offset Calibration Range	referenced to the selected source (VOS12); ORx = 00 ORx = 01 ORx = 10 ORx = 11		±100 ±200 ±600 ±1200		%V() %V() %V() %V()
115	ΔVOSdiff	Differential Linearity Error of Offset Correction	calibration range 11 bit	-0.5		0.5	LSB

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ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, T_j = -40...140 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
116	ΔVOSint	Integral Linearity Error of Offset Correction	calibration range 11 bit	-1		1	LSB
117	PHIkorr	Phase Error Calibration Range	CH1 versus CH2		±10.4		°
118	ΔPHIdiff	Differential Linearity Error of Phase Calibration	calibration range 10 bit	-0.5		0.5	LSB
119	ΔPHLint	Integral Linearity Error of Phase Calibration	calibration range 10 bit	-1		1	LSB
120	f _{in} (max)	Permissible Input Frequency		500			kHz
121	f _c (in)	Input Amplifier Cut-off Frequency (-3dB)		250			kHz
PGA Inputs and Signal Conditioning: X1, X2							
201	V _{in} (sig)	Permissible V-Mode Input Voltage Range	RIN0(3:0) = 0x01 (V-Mode 1:1) BIAS0 = 1, RIN0(3:0) = 0x09 (V-Mode 4:1) BIAS0 = 0, RIN0(3:0) = 0x09 (V-Mode 4:1)	0.75 0 0		VDDS - 1.5 VDDS VDDS - 1.5	V V V
202	V _{in} (diff)	Recommended Differential V-Mode Input Voltage	V _{in} (diff) = V(PXi) - V(NXi); RIN0(3:0) = 0x01 (V-Mode 1:1) RIN0(3:0) = 0x09 (V-Mode 4:1)	10 40		1500 6000	mV _{pp} mV _{pp}
203	V _{in} (os)	V-Mode Input Offset Voltage	referred to side of input, MODE(3:0) = 0x0 (normal), RIN0(3:0) = 0x01 (V-Mode 1:1); Max. gain: GR0, GF0 = max.	-500		+500	µV
205	I _{in} ()	V-Mode Input Current	RIN0(3:0) = 0x01 (V-Mode 1:1)	-10		10	µA
206	I _{in} (sig)	Permissible I-Mode Input Current Range	BIAS0 = 1, RIN0(0) = 0 BIAS0 = 0, RIN0(0) = 0	10 -300		300 -10	µA µA
207	V _{out} (X2)	Output Voltage at X2	BIASEX = 10, referenced to VREFin12; I(X2) = -10...+10 µA I(X2) = -150...+150 µA	95 90	100	105 110	% %
208	V _{in} (X2)	Permissible Input Voltage VREF _{ex} at X2	BIASEX = 11	0.5		VDDS - 2	V
209	R _{in} (X2)	Input Resistance at X2	BIASEX = 11, RIN0(3:0) = 0x01, RIN12(3:0) = 0x01 (all channels in V-Mode 1:1)	20	27	35	kΩ
210	R _{in} ()	I-Mode / V-Mode Input Resistance	referenced to VREFin, T _j = 27 °C; RIN0(3:0) = 0x00 RIN0(3:0) = 0x02 RIN0(3:0) = 0x04 RIN0(3:0) = 0x06 RIN0(3:0) = 0x09 (V-Mode 4:1)	1.1 1.6 2.2 3.2 16	1.6 2.3 3.2 4.6 20	2.1 3.0 4.2 6.0 24	kΩ kΩ kΩ kΩ kΩ
211	R2()	I-Mode Conversion Resistor	referenced to VREFin, T _j = 27 °C; RIN0(3:0) = 0x00 RIN0(3:0) = 0x02 RIN0(3:0) = 0x04 RIN0(3:0) = 0x06 RIN0(3:0) = 0x09 (V-Mode 4:1)		1.6 2.3 3.2 4.6 5.0		kΩ kΩ kΩ kΩ kΩ
212	TCR _{in} ()	Temperature Coefficient Rin			0.15		%/K
213	VREFI()	Internal Reference Voltage VREFI ₀	BIAS0 = 1, RIN0(0) = 0 BIAS0 = 0, RIN0(0) = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
214	G0	Selectable Gain Factors	RIN0(3:0) = 0x01, GR0 and GF0 = 0x0 RIN0(3:0) = 0x01, GR0 and GF0 = max. RIN0(3:0) = 0x09, GR0 and GF0 = 0x0 RIN0(3:0) = 0x09, GR0 and GF0 = max		0.667 100 0.167 25		
215	ΔGdiff	Differential Gain Accuracy	calibration range 5 bit	-0.5		0.5	LSB
216	ΔGabs	Absolute Gain Accuracy	calibration range 5 bit, guaranteed monotony	-1		1	LSB
217	VOScal	Offset Calibration Range	referenced to the selected source (REFVOS); OR0 = 00 OR0 = 01 OR0 = 10 OR0 = 11		±100 ±200 ±600 ±1200		%V() %V() %V() %V()

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ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, T_j = -40...140 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
218	ΔVOSdiff	Differential Linearity Error of Offset Correction	calibration range 6 bit	-0.5		0.5	LSB
219	ΔVOSint	Integral Linearity Error of Offset Correction	calibration range 6 bit	-1		1	LSB
Signal Filter							
301	fc	Cut-off Frequency	ENF = 1, f(in) 100 kHz for sine/cosine			4000	kHz
302	phi	Phase Delay (output vs. input)	ENF = 1, f(in) 500 kHz for sine/cosine			10	°
Index Pulse Comparator Output PZ, NZ							
401	Vpk()	Output Amplitude With Sensor Tracking via ACO	EAZ = 1, ADJ(4:0) = 0x19	225	250	275	mV
402	SR()	Output Slew Rate	EAZ = 1		1		V/µs
Analog Output Drivers: PS, NS, PC, NC, PZ, NZ							
501	Vpk()max	Permissible Max. Output Amplitude	VDD = 4.5 V, DC level = VDD/2, RL = 50 Ω vs. VDD/2			300	mV
502	Vpk()	Output Amplitude With Sensor Tracking via ACO	ADJ(8:0) = 0x19, ADJMODE = 0x1	225	250	275	mV
503	Vdc()	DC Output Voltage	versus GND; reference is VPAH, see 802 for tolerances		50		% VDD
504	fc()out	Cut-off Frequency	CL = 250 pF	500			kHz
505	Isc()	Short-circuit Current	pin shorten to VDD or GND	10	30	50	mA
506	Iik()	Tristate Leakage Current	tristate or reversed supply	-1		1	µA
507	Rout()	Output Impedance	BYP = 0, MODE = 0x02 (Calibration 2)		5		kΩ
508	fout()cal	Permissible Output Frequency for Calibration	BYP = 0, MODE = 0x02 (Calib. 2), CL = 250 pF			2	kHz
509	Rout()tm	Bypass Resistance	BYP = 1, MODE = 0x02, 0x06		7		kΩ
Signal Level Control, Current Source Output ACO							
601	Vs()hi	Saturation Voltage hi at ACO vs. VDD	Vs() = VDD - V(); ADJ(8:0) = 0x11F, I() = -5 mA ADJ(8:0) = 0x13F, I() = -10 mA ADJ(8:0) = 0x15F, I() = -25 mA ADJ(8:0) = 0x17F, I() = -50 mA			1 1 1 1.2	V V V V
602	Isc()hi	Short-circuit Current hi in ACO	V() = 0 ... VDD - Vs()hi; ADJ(8:0) = 0x11F ADJ(8:0) = 0x13F ADJ(8:0) = 0x15F ADJ(8:0) = 0x17F	-10 -20 -50 -100	-66	-5 -10 -25 -50	mA mA mA mA
603	tr()	Current Rise Time in ACO	I(ACO): 0 → 90 % setpoint, ADJMODE = 0x1		1		ms
604	tset()	Current Settling Time in ACO	Square control active, I(ACO): 50 → 100 % setpoint, ADJMODE = 0x1		400		µs
605	It()min	Control Range Monitoring 1: lower limit	referenced to range ADJ(6:5)		3		%Isc
606	It()max	Control Range Monitoring 2: upper limit	referenced to range ADJ(6:5)		90		%Isc
607	Vt()min	Signal Level Monitoring 1: lower limit	referenced to Vscq()		40		%Vpp
608	Vt()max	Signal Level Monitoring 2: upper limit	referenced to Vscq()		130		%Vpp
609	Vin(ACO)	Permissible Input Voltage for Offset-Tracking	versus GNDS, VOS12 = 0x0	0		VDDS	V
Test Current ERR							
701	I(ERR)	Permissible Test Current	test mode activated	0		1	mA

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ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, T_j = -40...140 °C, IBN calibrated to 200 μA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
Bias Current Source and Reference Voltages							
801	IBN()	Bias Current Source	MODE(3:0) = 0x01, I(NC) vs. VDD5	180	200	220	μA
802	VPAH	Reference Voltage VPAH	referenced to GND	45	50	55	%VDD
803	V05	Reference Voltage V05		450	500	550	mV
804	V025	Reference Voltage V025			50		%V05
Power-Down-Reset							
901	VDDon	Turn-on Threshold (power-on release)	increasing voltage at VDD vs. GND	3.7	4	4.3	V
902	VDDoff	Turn-off Threshold (power-down reset)	decreasing voltage at VDD vs. GND	3.2	3.5	3.8	V
903	VDDhys	Threshold Hysteresis	VDDhys = VDDon – VDDoff	0.3			V
Clock Oscillator							
A01	fclk()	Internal Clock Frequency	MODE(3:0) = 0x0A (measured at pin NS)	120	160	200	kHz
Error Input/Output: ERR							
B01	Vs()lo	Saturation Voltage lo	vs. GND, I() = 4 mA			0.4	V
B02	Isc()	Short-circuit Current lo	vs. GND; V(ERR) ≤ VDD V(ERR) > VTMon	4 2			mA mA
B03	Vt()hi	Input Threshold Voltage hi	vs. GND			2	V
B04	Vt()lo	Input Threshold Voltage lo	vs. GND	0.8			V
B05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo	300	500		mV
B06	Ipu()	Input Pull-up Current	V() = 0... VDD – 1 V, EPU = 1	-400	-300	-200	μA
B07	Rpu()	Input Pull-Up Resistor	EPU = 0		500		kΩ
B08	Vpu()	Pull-up Voltage	Vpu() = VDD – V(), I() = -5 μA, EPU = 1			0.4	V
B09	VTMon	Test Mode Activation Threshold	increasing voltage at ERR			VDD + 1.5	V
B10	VTMoff	Test Mode Disabling Threshold	decreasing voltage at ERR	VDD + 0.5			V
B11	VTMhys	Test Mode Hysteresis	VTMhys = VTMon – VTMoff	0.15	0.3		V
B12	I _{lk} ()	Leakage Current	tristate or reversed supply voltage	-1	-10	-50	μA
B13	tp()tri	Propagation Delay System Error to Driver Shutdown (tristate)	V(ERR): hi → lo		35		μs
Supply Switch and Reverse Polarity Protection: VDD5, GNDS							
C01	Vs()	Saturation Voltage VDD5 vs. VDD	Vs(VDD5) = VDD – V(VDD5) I(VDD5) = -10 mA...0 mA I(VDD5) = -20 mA...-10 mA			150 250	mV mV
C02	Vs()	Saturation Voltage GNDS vs. GND	Vs(GNDS) = V(GNDS) – GND I(GNDS) = 0 mA...10 mA I(GNDS) = 10 mA...20 mA			150 250	mV mV
C03	C()	Backup Capacitor Analog Supply VDD5 vs. GNDS		100			nF
Serial I²C Interface: SCL, SDA							
D01	Vs()lo	Saturation Voltage lo	I() = 4 mA			400	mV
D02	Isc()	Short-circuit Current lo		4		80	mA
D03	Vt()hi	Input Threshold Voltage hi				2	V
D04	Vt()lo	Input Threshold Voltage lo		0.8			V
D05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo	300	500		mV
D06	Ipu()	Input Pull-up Current	V() = 0...VDD5 – 1 V	-650	-300	-60	μA
D07	Vpu()	Input Pull-up Voltage	Vpu() = VDD5 – V(), I() = -5 μA			0.4	V
D08	fclk(SCL)	Clock Frequency at SCL	ENFAST = 0 ENFAST = 1	60 240	80 320	100 400	kHz kHz
D09	tbusy()cfg	Duration of Startup Configuration	IBN not calibrated, EEPROM access without read failure, time to outputs operational; ENFAST = 0 ENFAST = 1		40 25	55 35	ms ms

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ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, T_j = -40...140 °C, IBN calibrated to 200 μA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
D10	tbusy()err	End Of I2C Communication; Time Until I2C Slave Is Enabled	IBN not calibrated; V(SDA) = 0 V V(SCL) = 0 V or arbitration lost no EEPROM CRC ERROR		4 indef. 45 95	12 135 285	ms ms ms ms
D11	td()	Start Of Master Activity On I2C Protocol Error	SCL without clock signal: V(SCL) = constant; IBN not calibrated IBN calibrated to 200 μA	25 64	80 80	240 120	μs μs
D12	td()i2c	Delay for I2C-Slave-Mode Enable	no EEPROM, V(SDA) = 0 V		4	6.2	ms
D13	fclk()ext	Permissible External Clock Frequency at SCL				400	kHz
Temperature Monitoring							
E01	VTs	Temperature Sensor Voltage	VTs() = VDD5 – V(PS), T _j = 27 °C, Calibration Mode 3, no load	600	650	700	mV
E02	TCs	Temp. Co. of Temperature Sensor Voltage			-1.8		mV/K
E03	VTth	Temperature Warning Activation Threshold	VTth() = VDD5 – V(NS), T _j = 27 °C, Calibration Mode 3, no load; CFGTA(3:0) = 0x00 CFGTA(3:0) = 0x0F	260 470	310 550	360 630	mV mV
E04	TCth	Temp. Co. Temperature Warning Activation Threshold			0.06		%/K
E05	Thys	Temperature Warning Hysteresis	T _j = 27 °C	4	12	20	°C
E06	ΔT	Relative Shutdown Temperature	ΔT = T _{off} – T _w , T _j = 27 °C	4	12	20	°C

PROGRAMMING

Register Layout	Page 15	Signal Conditioning CH1, CH2 (X3...X6) ..	Page 27
Serial I²C Interface	Page 17	GR12:	Coarse Gain Factor CH1, CH2
ENFAST:	I ² C Fast Mode	GF1:	Fine Gain Factor CH1
ENSL:	I ² C Slave Mode	GF2:	Fine Gain Factor CH2
CHKSUM:	Configuration Data Checksum	VOS12:	Offset Reference Source CH1, CH2
CHPREL:	Chip Release	MP1:	VDC Center Potential CH1
RUN:	Device Enable	MP2:	VDC Center Potential CH2
Bias Current Source and Temperature Sensor	Page 20	OR1:	Coarse Offset Factor CH1
CFGIBN:	Bias Current	OF1:	Fine Offset Factor CH1
CFGTA:	Temperature Monitoring	OR2:	Coarse Offset Factor CH2
Operating Modes	Page 21	OF2:	Fine Offset Factor CH2
MODE:	Operating Mode	PH12:	Phase Correction CH1 to CH2
ENF:	Signal Filtering	Signal Conditioning CH0 (X1, X2)	Page 29
Test Mode	Seite 22	GR0:	Coarse Gain Factor CH0
TMODE:	Test Mode Functions	GF0:	Fine Gain Factor CH0
TMEM:	Test Mode Memory Selection	VOS0:	Offset Reference Source CH0
DEVID:	Device ID of EEPROM	OR0:	Coarse Offset Factor CH0
PGA Input Configuration and Signal Path Multiplexer	Page 23	OF0:	Fine Offset Factor CH0
INMODE:	Diff./Single-Ended Input Mode	Signal Level Control	Page 30
RIN12:	I/V Mode and Input Resistance CH1, CH2	ADJMODE:	Type of Control
BIAS12:	Reference Voltage CH1, CH2	ADJ(10:9):	Control Deadband
PULL12:	Clamp Resistor CH1, CH2	ADJ(8:7):	ACO Output Control Mode
RIN0:	I/V Mode and Input Resistance CH0	ADJ(6:5):	ACO Output Current Range
BIAS0:	Reference Voltage CH0	ADJ(4:0):	Square/Sum Control Setpoint
MUXIN:	Input Multiplexer	ADJ(4:0):	Current Source Setpoint
INVZ:	Index Signal Inversion	Monitoring and Error Output	Page 32
EAZ:	Index Comparator Enable	EPH:	Alarm Output ERR and I/O Logic
BIASEX:	Input Reference Selection	EMTD:	Min. Indication Time Alarm Outp. ERR
BYP	Input-to-Output Bypass	EPU:	Pull-Up Enable Alarm Output ERR
		EMASKA:	Error Mask Alarm Output ERR
		EMASKO:	Error Mask Driver Shutdown
		EMASKE:	Error Mask EEPROM Savings
		ERR1:	Error Protocol: First Error
		ERR2:	Error Protocol: Last Error
		ERR3:	Error Protocol: History
		PDMODE:	Driver Activation

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CONFIGURATION REGISTERS

Register Map								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration Interface								
0x00	ENFAST	DEVID(6:0)**						
Calibration								
0x01	CFGIBN(3:0)				CFGTA(3:0)			
Operating Modes								
0x02	RUN*	1	0	PULL12(1)	MODE(3:0)			
PGA Input Configuration and Signal Path Multiplexer								
0x03	EAZ	0	0	0	INVZ	INMODE	MUXIN(1:0)	
Signal Conditioning CH1, CH2								
0x04	GF2(4:0)					GR12(2:0)		
0x05	GF1(7:0)							
0x06	MP1(4:0)					GF1(10:8)		
0x07	MP2(2:0)			MP1(9:5)				
0x08	OR1(0)	MP2(9:3)						
0x09	OF1(6:0)							OR1(1)
0x0A	OF2(1:0)	OR2(1:0)			OF1(10:7)			
0x0B	OF2(9:2)							
0x0C	PH12(6:0)							OF2(10)
0x0D	BIASEX(1:0)	BYP	1	1	PH12(9:7)			
0x0E	ENF	BIAS12	VOS12(1:0)		RIN12(3:0)			
Signal Level Control								
0x0F	ADJ(0)	ADJMODE	0	1	0	0	0	0
0x10	ADJ(8:1)							
Signal Conditioning CH0								
0x11	GF0(4:0)					GR0(2:0)		
0x12	OF0(5:0)						OR0(1:0)	
0x13	PULL12(0)	BIAS0	VOS0(1:0)		RIN0(3:0)			
Error Monitoring and Alarm Output								
0x14	0	EMASKA(6:0)						
0x15	TMODE(1:0)		EMTD(2:0)			EPH	ADJ(10:9)	
0x16	0	EMASKO(6:0)*						
0x17	EMASKE(3:0)				ENSL	EPU	0	0
0x18	TMEM	PDMODE	0	0	0	EMASKE(6:4)*		
0x19.. 0x1A	not defined							
0x1B.. 0x1E	OEM Data							
Checksum / Chip Release								
0x1F	EEPROM: CHKSUM(7:0) / ROM: CHPREL(7:0)							

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Register Map									
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Error Register									
0x20	–	ERR1(6:0)							
0x21	ERR2(5:0)						–	–	
0x22	ERR3(3:0)			–	–	–	ERR2(6)		
0x23	–	–	–	–	–	ERR3(6:4)			
Notes	<p>The device RAM initially contains random data following power-on.</p> <p>*) Mandatory programming of EEPROM: RUN = 1, EMASKO(6) = 0, EMASKE(6) = 0.</p> <p>**) Programming DEVID is required only if using the Test Mode for data output via pin ERR.</p>								

Table 4: Register Layout (EEPROM)

SERIAL I²C INTERFACE

The multi-master capable I²C interface consists of two bidirectional pins, SCL (for clock) and SDA (for data), and enables iC-MSC to restore its configuration from the external serial EEPROM. For this function, the read-out can be accelerated from ENFAST reading onwards if a higher clock frequency is selected as an option.

The I²C master of iC-MSC addresses I²C devices using an 8-bit register address plus 3 block selection bits as part of the I²C device ID. That way an external EEPROM of up to 2 Kbit is addressed at 0x50 (for '1010 000' without the R/W bit), or 0xA0 respectively (for '1010 0000' with the R/W bit as zero), whereas the block selections bits are zero.

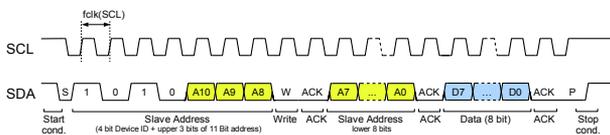


Figure 1: I²C slave addressing for writing a single byte to the EEPROM.

Furthermore, the I²C interface can be enabled to operate as an I²C slave (using ENSL), allowing an external I²C master to monitor and edit iC-MSC's configuration data.

ENFAST	
Code	Function
0	Regular clock rate, f(SCL) approx. 80 kHz
1	High clock rate, f(SCL) approx. 320 kHz
Notes	For in-circuit programming bus lines SCL and SDA require pull-up resistors (e.g. 2.2 kΩ for line capacitances of up to 170 pF and clock rate 320 kHz; the permissible minimum value is 1.5 kΩ). A ground trace between SCL and SDA is recommended to avoid cross talk.

Table 5: I²C Fast Mode

ENSL	
Code	Function
0	I ² C slave mode disabled
1	I ² C slave mode enabled (Device ID 0x55)

Table 6: I²C Slave Mode

I ² C Master Performance	
Protocol	Standard I ² C
Output Clock Rate	100 kHz max. (see Elec.Char. D08), 400 kHz max. using ENFAST = 1
Addressing	11 bit: 8 bit register address plus 3 bit block selection
Access Trials	Read: up to 4x at power-on (I ² C error: acknowledge missing), 1x at byte reading, 1x at byte writing (for consecutive writing with pauses from byte to byte)
Multi-Master Capability	Yes
I ² C Slave Performance	
Input Clock Rate	400 kHz max. (see Elec.Char. D13)
Device ID	0x55 ('1010 101' w/o R/W bit)

Table 7: I²C interface performance

Note: The I²C bus lines are sensitive. Keeping the traces short and shielding them with ground prevents unwanted actions.

The use of pull-up resistors (e.g. 2.2 kΩ at SCL and SDA) supports the bus signals on logic high and improves the EMI immunity.

Note: When programming the EEPROM in-circuit, iC-MSC must be powered up in advance to avoid interferences by its I²C master. Note that power must be maintained (e.g. for 10 ms) to allow the EEPROM finishing its write operation.

Attention: If a power failure interrupts the EEPROM's write operation, the entire page content may be lost.

Attention: If error logging is enabled and periodic errors occur, the maximum permissible write cycles may be exceeded. The recommended precaution is to disable error logging (refer to EMASKE), and to lock the EEPROM by its WP pin after factory calibration.

EEPROM Device Selection

EEPROM Device Requirements	
Supply Voltage	3.3 V to 5.5 V
Power-On Threshold	< 3.3 V (due to Elec.Char. 901)
Addressing	11 bit address max.
Device Address	0x50 ('1010 000' w/o R/W bit), 0xA0 ('1010 0000' with R/W = 0)
Page Buffer	Support of <i>Page Write</i> with pages of at least 4 bytes.
Size Minimum	512 bit (64x8 bit) (address range used is 0x00 to 0x3F)
Size Maximum	8 Kbit (4x 256x8 bit), type 24C08 If I ² C Slave Mode is disabled: 16 Kbit (8x 256x8 bit), type 24C16

Table 8: EEPROM Device Requirements

If the EEPROM does not feature *Page Write*, error events can not be saved (EMASKE must be configured to 0x00).

The following EEPROMs have been recommended, but may need to be re-tested for the above conditions: Atmel AT24C01, ST M24C01, ST M24C02 (2K), ROHM BR24L01A-W, BR24L02-W.

Attention: EEPROMs that ignore the block select or upper address bits in the control byte (such as the Microchip 24AA0x/24LC0xB, and maybe other 5-pin devices) should not be used with the iC-MSC. EEPROMs that use the address pins as additional enable bits should be used instead.

Attention: When I²C Slave Mode is enabled, iC-MSC responds to device ID 0x55, limiting the maximum EEPROM size to 8 Kbit (0x50 to 0x53 addresses 4x 256 bytes).

Device Startup

Once the supply has been switched on, i.e. after a power down reset, the iC-MSC outputs are high impedance (tristate) until a valid configuration is read from the EEPROM using device ID 0x50.

If the configuration data is not confirmed by its checksum, the readin process is repeated. If no valid configuration data is available after a fourth attempt, iC-MSC terminates communication with the EEPROM and enables I²C slave mode. For timing information, refer to the Electrical Characteristics, items D10 and D11.

For devices loading valid configuration data from the EEPROM, bit ENSL decides whether the I²C slave function is enabled or not.

Configuration Data Checksum

The checksum at address 0x1F is used to initially confirm the configuration data read from the EEPROM.

CHKSUM	Addr. 0x1F, bit 7:0
Code	Function
0x00... ...0xFF	Checksum for address range 0x00 to 0x1E; CRC polynomial 0x11D ($x^8 + x^4 + x^3 + x^2 + 1$) Start value: 0x01

Table 9: Configuration Data Checksum

Example of CRC Calculation Routine:

```

unsigned char ucDataStream = 0;
int iCRCPoly = 0x11D;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 1; // start value !!!
for (iReg = 0; iReg<31; iReg ++ )
{
    ucDataStream = ucGetValue(iReg);
    for (i=0; i<=7; i++) {
        if ((ucCRC & 0x80) != (ucDataStream & 0x80))
            ucCRC = (ucCRC << 1) ^ iCRCPoly;
        else
            ucCRC = (ucCRC << 1);
        ucDataStream = ucDataStream << 1;
    }
}
    
```

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I²C Slave Mode (ENSL = 1)

In this mode iC-MSC behaves like an I²C slave with the device ID 0x55 and the configuration interface permits reading and writing to and from iC-MSC's internal registers.

For chip release verification purposes an identification value is stored under ROM address 0x1F; writing to this address is not permitted.

CHPREL		Addr. 0x1F, bit 7:0 (ROM)
Code	Chip Release	
0x40	iC-MSC 0	

Table 10: Chip Release

RUN		Addr. 0x02, bit 7
Code	Function	
0	Device standby: output drivers disabled (tristate)	
1	Device enabled: state of output drivers depends on error conditions (tristate on temperature or checksum error).	
Notes	RUN is evaluated only during I ² C slave mode. Writing changes the function. Reading does not return the chip's state.	

Table 11: Device Enable

Register		Read access in I ² C slave mode (ENSL = 1)
Address	Content	
0x00...18	Configuration: register addresses 0x00...0x18	
0x19...1A	Not available	
0x1B...1E	OEM data (4 bytes) (see EEPROM addresses 0x1B...0x1E)	
0x1F	Chip release (ROM)	
0x20...23	Configuration: register addresses 0x20-0x23	
0x24...37	Not available	
0x38	Configuration: register address 0x18	
0x39...3A	Not available	
0x3B...3E	OEM data (4 bytes) (see EEPROM addresses 0x1B...0x1E)	
0x3F	Chip release (ROM)	
0x40...43	Current error memory (only active if enabled by EMASKE; messages are transferred to EEPROM addresses 0x20...0x23)	
0x44...7F	Not available	

Table 12: RAM Read Access

Register		Write access in I ² C slave mode (ENSL = 1)
Address	Access and conditions	
0x00	Changes possible, no restrictions	
0x01	Changes possible (wrong entries for CFGIBN can limit functions)	
0x02	Bit 7 = 0 (RUN): changes to bits (6:0) permitted A change of operating mode follows only on writing Bit 7 = 1 (RUN); when doing so, changes to bits (6:0) are not permitted.	
0x03...16	Changes possible, no restrictions	
0x17	Bit 3 = 1 (ENSL): changes to bits (7:4) and (2:0) permitted	
0x18	Changes possible, no restrictions	
0x19...1A	Not available	
0x1B...1E	Changes possible, no restrictions	
others	No changes permitted	

Table 13: RAM Write Access

BIAS CURRENT SOURCE AND TEMPERATURE SENSOR

Bias Current Calibration

The calibration of the bias current source in operating mode *Calibration 1* (refer to Table 16 for an overview of operating modes) is required to adhere to the given Electrical Characteristics and also instrumental in determining the chip timing (e.g. SCL clock frequency).

The IBN bias current is measured by connecting **pin VDDS** and **pin NC** with a 10 kΩ resistor. When the voltage drop is 2 V, the bias current is adjusted to its target value of 200 μA.

Note: The outputs may not be tristate when measuring the IBN bias current. Therefore, a virgin EEPROM must first be configured (e.g. by a default setup with CRC) and the power cycled to obtain active outputs.

CFGIBN Addr. 0x01, bit 7:4			
Code k	IBN ~ $\frac{31}{39-k}$	Code k	IBN ~ $\frac{31}{39-k}$
0x0	79 %	0x8	100 %
0x1	81 %	0x9	103 %
0x2	84 %	0xA	107 %
0x3	86 %	0xB	111 %
0x4	88 %	0xC	115 %
0x5	91 %	0xD	119 %
0x6	94 %	0xE	124 %
0x7	97 %	0xF	129 %

Table 14: Bias Current

Temperature Sensor Calibration

The temperature monitoring is calibrated in operating mode *Calibration 3* (refer to Table 16 for an overview of operating modes).

First, the temperature sensor voltage at which the warning message is generated, VTs, must be determined. A voltage ramp from VDDS towards GNDS is applied to pin PS until pin ERR pulls low (at approx. 4.4 V when coming from 5.0 V). The following settings are required for this measurement: EMASKA = 0x20 (excessive temperature warning enabled), EMTD = 0x00 (shortest alarm indication time), and EPH = 0x00 (alarm output active low).

Note that the signal at pin ERR switches from tristate to low (on reaching VTs) and already at just 25 mV lower

from low to tristate (on overshooting the temperature shutdown threshold, which is not relevant to calibration). To avoid confusion, a clear change of state (from high → low → high) should be generated using an external pull-up resistor at pin ERR.

Example: VTs(T₁) is approx. 640 mV, measured from VDDS versus PS, with T₁ = 25 °C;

The necessary warning activation threshold, VTth(T₁), is then calculated. The required warning temperature T₂, temperature coefficients TCs and TCth (see Electrical Characteristics, Section E), and measurement value VTs(T₁) are entered into this calculation:

$$VTth(T_1) = \frac{VTs(T_1) + TCs \cdot (T_2 - T_1)}{1 + TCth \cdot (T_2 - T_1)}$$

Example: for T₂ = T₁ + 100 K VTth(T₁) must be programmed to 434 mV.

Reference voltage VTth(T₁) is provided for a high impedance measurement (10 MΩ) at output pin NS (measurement against VDDS) and must be set to the calculated value by programming CFGTA(3:0).

Example: altering VTth(T₁) from 315 mV (measured with CFGTA(3:0) = 0x0) to 434 mV is equivalent to 138 %, the closest value for CFGTA is 0x8;

CFGTA Addr. 0x01, bit 3:0			
Code k	VTth ~ $\frac{65 + 3.25k}{65}$	Code k	VTth ~ $\frac{65 + 3.25k}{65}$
0x0	100 %	0x8	140 %
0x1	105 %	0x9	145 %
0x2	110 %	0xA	150 %
0x3	115 %	0xB	155 %
0x4	120 %	0xC	160 %
0x5	125 %	0xD	165 %
0x6	130 %	0xE	170 %
0x7	135 %	0xF	175 %
Notes	CFGTA = 0xC: Tw is approx. 85 °C, and Toff is approx. 97 °C typically. CFGTA = 0x8: Tw is approx. 125 °C, and Toff is approx. 137 °C typically.		

Table 15: Temperature Monitoring

iC-MSC SIN/COS SIGNAL CONDITIONER WITH FAIL-SAFE 1 Vpp LINE DRIVER



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OPERATING MODES

The iC-MSC has several operating modes, for which the functions of outputs PS, NS, PC, NC, PZ, NZ and ERR are different.

In order to condition the input signals and to calibrate and test the iC-MSC, various Calibration and Test modes are available. The analog test signals which are provided must always be measured at high load

impedance. The output drivers and the reverse polarity protection feature are not active during Calibration and Test modes.

During Normal operating mode the analog output drivers are engaged to allow driving terminated lines (by differential 1 Vpp signals into 120 Ω), and also the reverse polarity protection feature is active.

MODE(3:0)		Addr. 0x02; bit 3:0						
BYP		Addr. 0x0D; bit 5						
Code	Operating Mode	Pin PS	Pin NS	Pin PC	Pin NC	Pin PZ	Pin NZ	Pin ERR
0x00	Normal operation	PS	NS	PC	NC	PZ	NZ	ERR
0x01	Calibration 1	TANA0(2)	VREFI0	VREFI12	IBN	PZI	NZI	ERR
0x02	Calibration 2, BYP = 0 Calibration 2, BYP = 1*	PCH1 X4	NCH1 X6	PCH2 X3	NCH2 X5	VDC1 X1	VDC2 X2	—
0x03	iC-Haus Test 1	VPAH	VPD	—	CGUCK	IPF	V05	IERR
0x04	iC-Haus Test 2	PS_out	NS_out	PC_out	NC_out	PZ_out	NZ_out	IERR
0x05	iC-Haus Test 3	PS_out	NS_out	PC_out	NC_out	PZ_out	NZ_out	ERR
0x06	iC-Haus Test 4, BYP = 0 iC-Haus Test 4, BYP = 1*	TANA12(0) X4	TANA12(1) X6	TANA12(2) X3	TANA12(3) X5	TANA12(4) X1	TANA12(5) X2	IERR
0x07	Calibration 3	VTs	VTth	—	—	—	—	ERR
0x08	Saturation low	SCL, SDA and ERR low						
0x09	—	—	—	—	—	—	—	—
0x0A	iC-Haus Test 5	—	—	TP	CLK6	—	—	—
0x0B	—	—	—	—	—	—	—	—
0x0C	—	—	—	—	—	—	—	—
0x0D	—	—	—	—	—	—	—	—
0x0E	IDDQ-Test	All PU/PD resistors, oscillator and supply voltage deactivated						
0x0F	—	—	—	—	—	—	—	—
Notes	Analog calibration signals are output via approx. 5 kΩ source impedance (see Elec. Char. No. 507). For accuracy of calibration the signal frequency should not exceed 2 kHz (see Elec. Char. No. 508). * Bypass function: inputs (without voltage divider) to outputs, approx. 7 kΩ source impedance (see Elec. Char. No. 509).							

Table 16: Operating Modes

Calibration Op. Modes

In mode *Calibration 1* the user can measure the BIAS current (IBN), input amplifier reference potential VREFI and the analog signals from channel 0 following signal conditioning (PCH0 and NCH0).

In mode *Calibration 2* the conditioned signals from channels 1 and 2 are output (PCH1, NCH1, and PCH2, NCH2). In addition, the VDC offset references generated in the input circuits are also available for calibration of their center potentials (CH1: VDC1, CH2: VDC2).

In mode *Calibration 3* the internal temperature monitoring signals are provided.

Special Device Test Functions

IDDQ-Test, *Saturation Low*, *Saturation High*, and *Test 1 to 5* are test modes for iC-Haus device tests. With

an activated bypass (BYP = 1), mode *iC-Haus Test 4* permits the direct feedthrough of X1 - X6 input signals to the output pins; in this instance the output's source impedance is quite high. Furthermore, if the input voltage divider is selected (by RINx = 1--1), it reduces the signal amplitudes to approx. 7/8 of the original.

Signal Filter

iC-MSC has a noise limiting signal filter to smooth the conditioned analog signals. This can be activated using ENF.

ENF		Addr. 0x0E, bit 7
Code	Function	
0	Noise limiter deactivated	
1	Noise limiter activated	

Table 17: Signal Filtering

PGA INPUTS CONFIGURATION

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Single-ended input signals can be processed by applying the input signal's reference voltage to the negative inputs, or rather to X2, when using the single-ended input configuration.

Both voltage and current signals can be accepted as input signals. For selection, use registers RIN12 and RIN0.

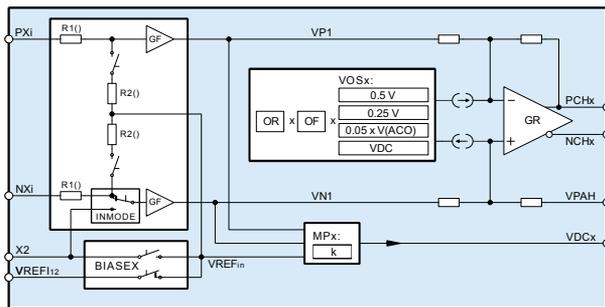


Figure 3: Signal conditioning input circuit.

Voltage Signals

In voltage mode (V-Mode), an optional voltage divider can be selected for high input amplitudes. This voltage divider reduces the input signal's amplitude to 25 % of the original. The internal circuit corresponds to the circuit in current mode, just the in-line resistor R1 is altered.

Current Signals

In current mode (I-Mode), an internal resistor R2() becomes active at each input, converting the current signal into a voltage signal. The effective input resistance Rin() is always determined by the sum of R1 and R2, whereas R2 links to the selectable reference voltage VREFin.

R2 should be set to obtain approx. 125 mV to 250 mV for the VDC offset references (for VDC1 and VDC2, using operating mode Calibration 2).

Note: The input circuit is not suitable for back-to-back photodiodes.

INMODE	
Code	Function
0	Differential input signals
1	Single-ended input signals *
Note	* Input X2 is reference for all inputs.

Table 20: Diff./Single-Ended Input Mode

RIN12		RIN0	
Addr. 0x0E, bit 3:0		Addr. 0x13, bit 3:0	
Code	In-line R1()	Internal R2()	I/V Mode
-000	0.1 kΩ	1.6 kΩ	I-Mode
-010	0.2 kΩ	2.3 kΩ	I-Mode
-100	0.3 kΩ	3.2 kΩ	I-Mode
-110	0.3 kΩ	4.6 kΩ	I-Mode
0—1	3.5 kΩ	See Table 24	V-Mode 1:1*
1—1	15 kΩ	5 kΩ	V-Mode 4:1*
Notes	Nominal values; Rin = R1() + R2(); for tolerances refer to Elec.Char. No. 107, 108, 210, 211. VREFin is the voltage divider's footpoint. Input currents may be positive or negative (Vin > VREFin, or Vin < VREFin). When using X2 as reference and single-ended input configuration (INMODE = 1), use RIN12 = RIN0. *) See Elec.Char. No. 101 for permissible input voltage range.		

Table 21: I/V Mode and Input Resistance

Input Reference Voltages

The parameters BIAS12 and BIAS0 determine the input circuit's internal reference voltages VREFI12 and VREFI0.

In the generation of the VDC offset references, BIAS12 also determines whether the reference voltage VREFin is subtracted from the sum of the particular input signals or the sum is subtracted from VREFin.

BIAS12	
Addr. 0x0E, bit 6	
BIAS0	
Addr. 0x13, bit 6	
Code	Function
0	VREFI = 2.5 V for low-side current sinks (e.g. photodiodes with common anode at GNDS) Note*: V(PXi) + V(NXi) < 2 x VREFin
1	VREFI = 1.5 V for high-side current-sources (e.g. photodiodes with common cathode at VDD5) for voltage sources relative to ground (e.g. iC-SM2, Wheatstone sensor bridges) for voltage sources with low-side reference (e.g. iC-LSHB, when using BIASEX = 11) Note*: V(PXi) + V(NXi) > 2 x VREFin
Notes	*) Condition is relevant only if using - the VDC offset references (see Table 32) - the input voltage divider (see Table 21) - sum control mode (see Table 43)

Table 22: Reference Voltage

In the generation of the VDC offset references it is also essential that the input circuit refers to the same footpoint as the incoming sensor signals.

For footpoint levels above ground, BIASEX = 11 allows both internal VREF_{I12} and VREF_{I0} sources to be replaced by the sensor's reference voltage, connected as VREF_{ex} to input X2.

Vice versa, using BIASEX = 10, iC-MSC's internal VREF_{I12} can be output to X2, to be used as reference for the external sensor circuit (using an opamp for buffering is required).

Note that whenever X2 is used to output VREF_{I12} or to input VREF_{ex}, the internal reference VREF_{in} is always the same for CH1, CH2, and CH0.

BIASEX	Addr. 0x0D, bit 7:6	
Code	X2 Function	Input Reference Voltage
00	Input X2 ← Index-	VREF _{in12} = VREF _{I12} VREF _{in0} = VREF _{I0}
10	Output* VREF _{I12} → X2	VREF _{in12} = VREF _{in0} = VREF _{I12}
11	Input** X2 ← VREF _{ex}	VREF _{in12} = VREF _{in0} = VREF _{ex}
Notes	*) Output signal should be buffered.) See Elec. Char. Nos. 208 and 209.	

Table 23: Input Reference Selection

Input Clamping Resistors

For ease of detection of a broken sensor wire, optional input clamping resistors can be enabled using PULL12. When a connection fails, the corresponding input clamping resistor reduces the input amplitude to trigger signal monitoring alarms.

Note: Using the built-in clamping resistors may not fulfill the application requirements for functional safety.

PULL12(1) Addr. 0x02, bit 4	
PULL12(0) Addr. 0x13, bit 7	
Code	Function
0	1 MΩ clamp resistor at PXi and NXi against VREF _{in}
1	1 MΩ clamp resistor at PXi and NXi against X2
2	1 MΩ clamp resistor at PXi and NXi against GNDS
3	No clamp resistor at PXi and NXi
Note	CH0 includes fixed 2 MΩ resistor between X1, X2

Table 24: Input Clamping CH1, CH2

Examples of Permissible Input Voltages

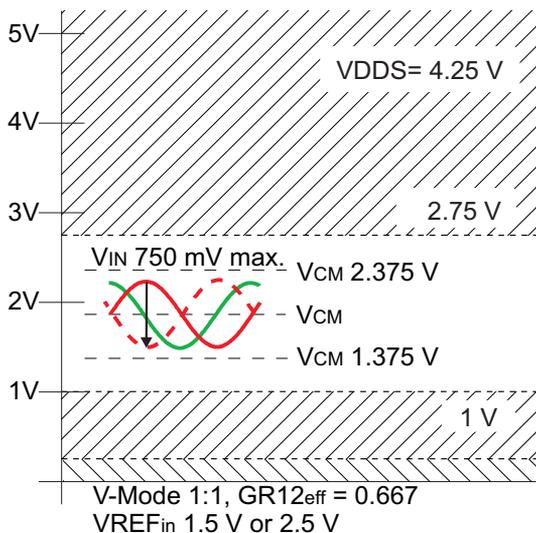


Figure 4: Permissible maximum input amplitude V_{IN} and common mode input range V_{CM} for $G12_{eff} = 0.667$ and V-Mode 1:1.

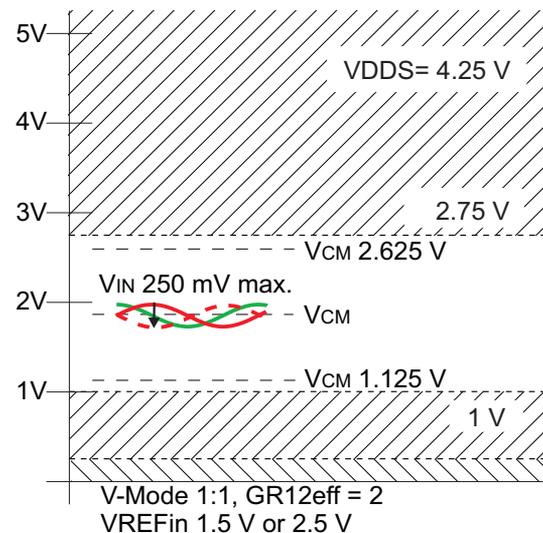


Figure 5: Permissible maximum input amplitude V_{IN} and common mode input range V_{CM} for $G12_{eff} = 2.0$ and V-Mode 1:1.

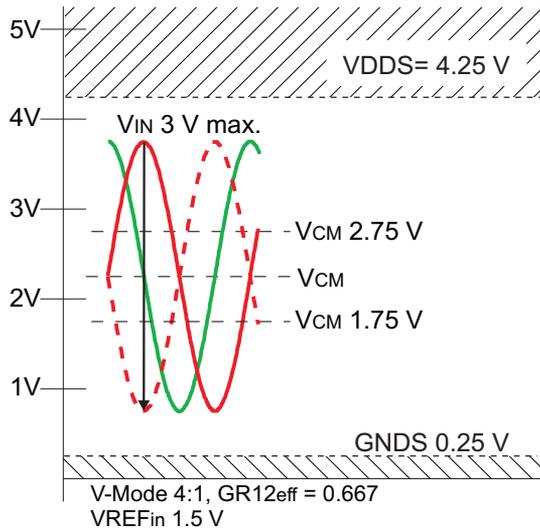


Figure 6: Permissible maximum input amplitude V_{IN} and common mode input range V_{CM} for $G_{12_{eff}} = 0.667$ and V-Mode 4:1.

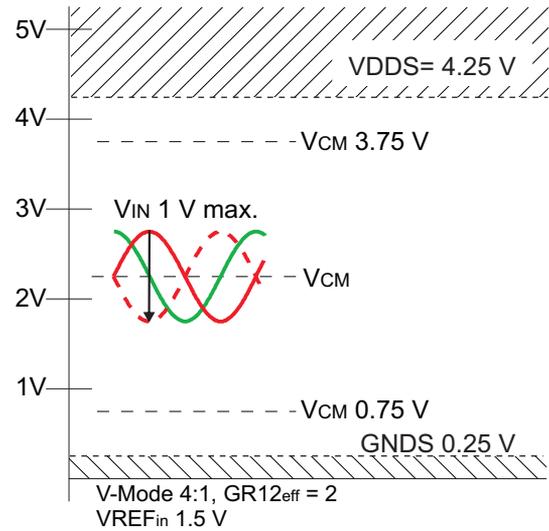


Figure 7: Permissible maximum input amplitude V_{IN} and common mode input range V_{CM} for $G_{12_{eff}} = 2.0$ and V-Mode 4:1.

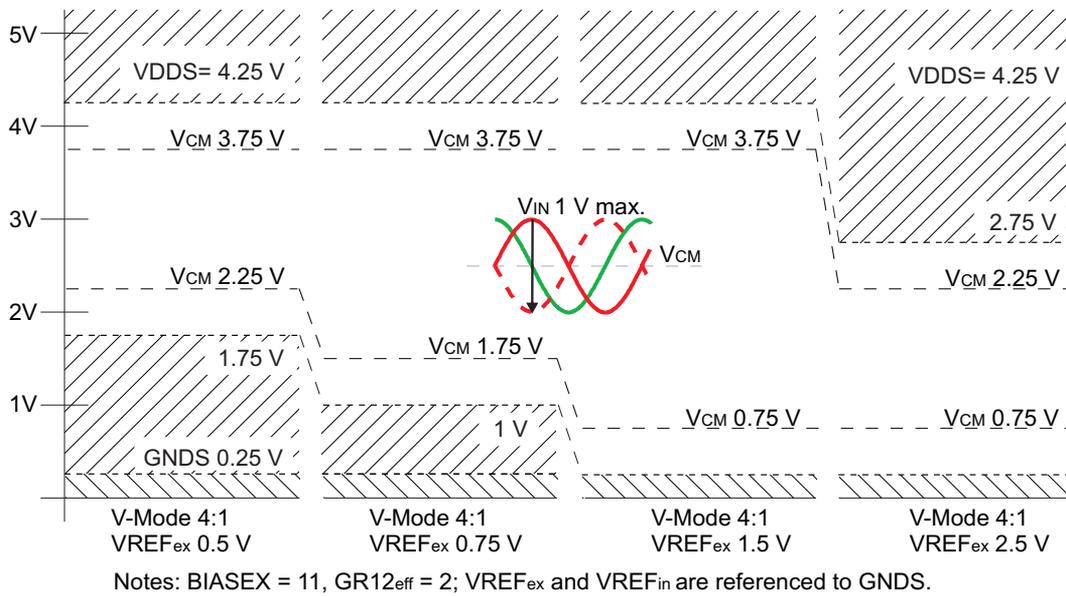


Figure 8: Permissible maximum input amplitude V_{IN} and common mode input range V_{CM} for $G_{12_{eff}} = 2.0$ and V-Mode 4:1 in dependency to the reference voltage.

SIGNAL PATH MULTIPLEXER

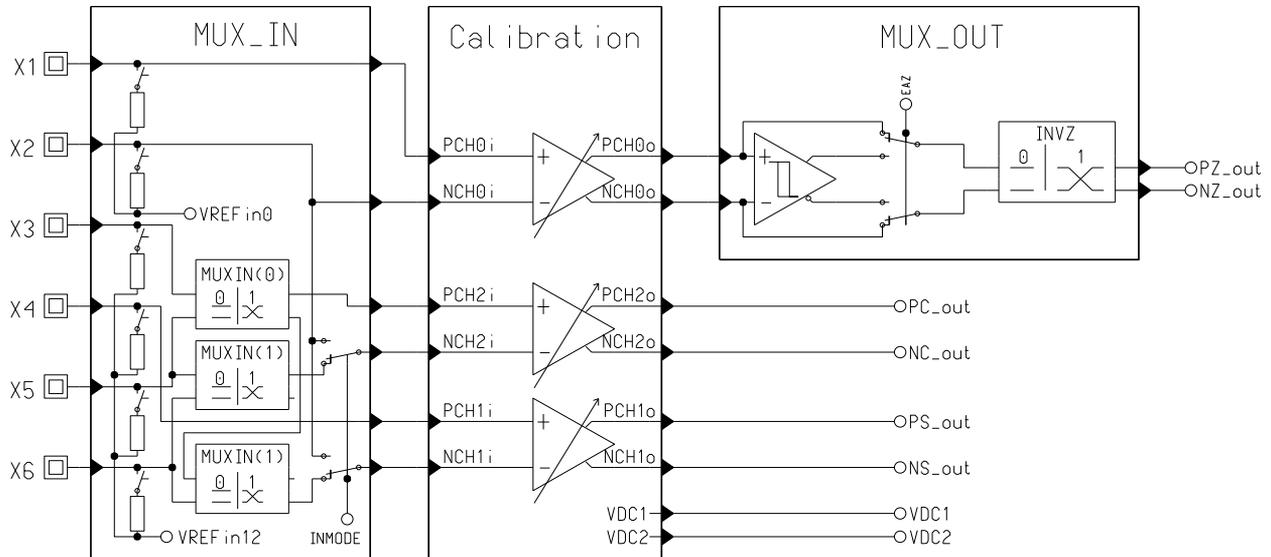


Figure 9: Multiplexer Schematics

The index signals for channel CH0 are to be connected to pins X1 and X2, and the positive-going sine signal for channel CH1 to pin X4.

For the pins X3 to X6, a flexible allocation to channel CH1 and CH2 is possible using MUXIN.

INMODE can be activated for single-ended, referenced input signals; this then selects pin X2 as the reference input (refer to Table 20, page 23).

INVZ allows to invert the index signal's output phase.

EAZ permits the activation of an analog comparator for index channel CH0. When enabled, the PZ and NZ outputs deliver a compared index signal with analog high and low levels, which are generated from the square control's quadrature circuit. Thus, the differential output amplitude at PZ versus NZ follows the square control's setpoint (refer to ADJ(4:0), Table 46, page 30).

Note: When the PZ and NZ outputs show a ripple using EAZ=1, the sin/cos signals of CH1 and CH2 may not have been calibrated accurately.

MUXIN 0x03, bit 1:0				
Code	PCH1i	NCH1i	PCH2i	NCH2i
00	X4	X6	X3	X5
01	X4	X6	X5	X5
10	X4	X5	X3	X6
11	X4	X3	X5	X6

Table 25: Input Multiplexer for INMODE = 0

MUXIN 0x03, bit 1:0				
Code	PCH1i	NCH1i	PCH2i	NCH2i
-0	X4	X2	X3	X2
-1	X4	X2	X5	X2

Table 26: Input Multiplexer for INMODE = 1

INVZ Addr. 0x03, bit 3		
Code	PZ_out	NZ_out
0	PCH0o	NCH0o
1	NCH0o	PCH0o

Table 27: Index Signal Inversion

EAZ Addr. 0x03, bit 7	
Code	Function
0	Comparator bypass
1	Comparator active

Table 28: Index Comparator Enable

SIGNAL CONDITIONING CH1, CH2

The voltage signals necessary for the conditioning of channels 1 and 2 can be measured in operating mode *Calibration 2*.

Gain Settings

The gain is set in four steps:

1. The signal level control is to be shut down and the constant current source for the ACO output is set to a suitable output current (register ADJ; a value close to the later operating point).
2. The coarse gain factor is selected so that differential signal amplitudes of approx. 1 Vpp are to be produced (signal Px vs. Nx, see Figure below).
3. Using fine gain factor GF2, the CH2 signal amplitude is then to be adjusted to exactly 1 Vpp.
4. Finally, the CH1 signal amplitude can then be adjusted precisely to the CH2 signal amplitude via fine gain factor GF1.

This results in a total gain of $GR12 \times GFx$ for differential input signals.

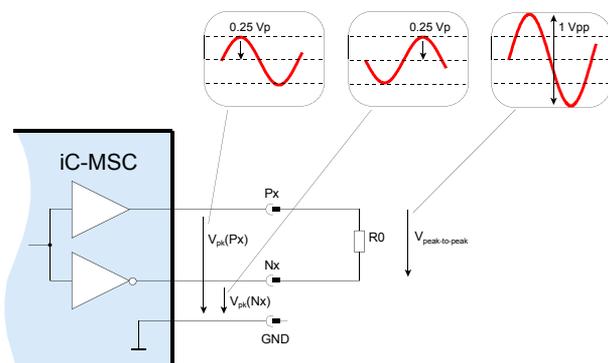


Figure 10: Definition of 1 Vpp differential signal. Termination R0 must be high-impedance (resistive) during all *Test* and *Calibration* modes.

GR12	
Addr. 0x04, bit 2:0	
Code	Factor
0x0	0.667
0x1	2.0
0x2	4.1
0x3	6.7
0x4	8.7
0x5	10.5
0x6	13.2
0x7	16.0
Notes	The effective total gain is calculated using: $G12_{\text{eff}} = GFx \times GR12$, or $G12_{\text{eff}} = 1/4 \times GFx \times GR12$ if using the input voltage divider (RIN12 = 0x9).

Table 29: Coarse Gain Factor CH1, CH2

GF2	
Addr. 0x04, bit 7:3	
Code	Factor
0x00	1.00
0x01	1.06
...	$6.25^{\frac{\text{Code}}{31}}$
0x1F	6.25

Table 30: Fine Gain Factor CH2

GF1	
Addr. 0x06, bit 2:0, Addr. 0x05, bit 7:0	
Code	Factor
0x000	1.0
0x001	1.0009
...	$6.25^{\frac{\text{Code}}{1984}}$
0x7FF	6.6245

Table 31: Fine Gain Factor CH1

Offset Calibration

In order to calibrate the offset the reference source must first be selected using VOS12. Two fixed voltages and two dependent sources are available for this purpose. The fixed voltage sources should be selected for external sensors which provide stable, self-regulating signals.

So that photosensors can be operated in optical encoders iC-MSC tracks changes in offset voltages via the signal-dependent source VDC when used in conjunction with the controlled sensor current source for LED supply (pin ACO). The VDC potential automatically tracks higher DC photocurrents. To do this, the center potentials for the VDC offset references can be adjusted to minimize their AC ripple, using parameters MP1 for VDC1, and MP2 for VDC2 (refer to the k factor of Table 33).

The feedback of pin voltage V(ACO) fulfills the same task as the VDC offset references when MR bridge sensors are supplied by the ACO output (using the controlled current source), or by supply VDDS (with pin ACO linked to VDDS to measure the bridge's supply).

VOS12 Addr. 0x0E, bit 5:4	
Code	Type of source
0x0	Feedback of ACO pin voltage: V(ACO)/20 for sensor supply-dependent diff. voltage signals for Wheatstone sensor bridges to measure VDDS (relative to GNDS)
0x1, 0x2	Fixed reference: V05 of 500 mV, V025 of 250 mV for single-ended current or voltage signals for single-ended or differential stabilized signals (regulated sensor or waveform generator)
0x3	Self-tracking VDC offset references (125...250 mV) for differential current signals for differential voltage signals (measured relative to VREFin*)
Notes	*) Requires BIASEX = 11 and the sensor's reference level connected to input X2 (see Elec. Char. No. 201 for acceptable input voltage).

Table 32: Offset Reference Source CH1, CH2

MP1 Addr. 0x07, bit 4:0; Addr. 0x06, bit 7:3	
MP2 Addr. 0x08, bit 6:0; Addr. 0x07, bit 7:5	
Code	$VDCi = (1 - k) \cdot VPi + k \cdot VNi$
0x000	$k = 1/3$
0x001	$k = 0.3337$
...	$k = 1/3 + 1/3 \cdot Code/1023$
0x200	$k = 0.5000$ (center setting)
...	...
0x3FF	$k = 2/3$
Notes	Adjustment is required only if VOS12 = 0x3

Table 33: VDC Center Potential CH1, CH2

The offset calibration range for CH1 and CH2 is set using the coarse offset factors OR1 and OR2. Both sine and cosine signals are then calibrated using the fine offset factors OF1 and OF2. The calibration target is reached when the DC component of the differential signals PCHx to NCHx is zero.

OR1 Addr. 0x09, bit 0; Addr. 0x08, bit 7	
OR2 Addr. 0x0A, bit 5:4	
Code	Factor
0x0	1
0x1	2
0x2	6
0x3	12

Table 34: Coarse Offset Factor CH1, CH2

OF1 Addr. 0xA, bit 3:0; Addr. 0x9, bit 7:1	
OF2 Addr. 0xC, bit 0; Addr. 0xB, bit 7:0; Addr. 0xA, bit 7:6	
Code	Factor
0x000	0
0x001	0.00098
...	+ Code/1023
0x3FF	+ 1
0x400	0
0x401	- 0.00098
...	- (Code - 1024)/1023
0x7FF	- 1

Table 35: Fine Offset Factor CH1, CH2

Phase Correction CH1 to CH2

The phase shift between CH1 and CH2 can be adjusted using parameter PH12. After phase calibration other calibration parameters may have to be adjusted again (those as amplitude compensation, center potentials and offset voltages).

PH12 Addr. 0xD, bit 2:0; Addr. 0xC, bit 7:1	
Code	Correction angle
0x000	0°
0x001	+ 0.0204°
...	+ 10.42° · Code/511
0x1FF	+ 10.42°
0x200	0°
0x201	- 0.0204°
...	- 10.42° · (Code - 512)/511
0x3FF	- 10.42°

Table 36: Phase Correction CH1 to CH2

SIGNAL CONDITIONING CH0

The test signals required to calibrate channel 0 are available in mode *Calibration 1*.

Gain Settings CH0

The CH0 gain is set using the following steps:

1. The signal level control is to be shut down and the constant current source for the ACO output set to the same values as during the calibration of CH1 and CH2 (register ADJ; current value close to the later operating point).
2. The coarse gain is to be selected so that a differential signal amplitude of approx. 1 Vpp is produced (signal PCHx to NCHx).
3. GF0 then permits fine gain adjustment to 1 Vpp. The resulting gain is GR0 x GF0.

GR0		Addr. 0x11, bit 2:0
Code	Factor	
0x0	0.667	
0x1	2.0	
0x2	4.1	
0x3	6.7	
0x4	8.7	
0x5	10.5	
0x6	13.2	
0x7	16.0	
Notes	The effective total gain is calculated using: $G_{0\text{eff}} = GF0 \times GR0$, or $G_{0\text{eff}} = 1/4 \times GF0 \times GR0$ if using the input voltage divider (RIN0 = 0x9).	

Table 37: Coarse Gain Factor CH0

GF0		Addr. 0x11, bit 7:3
Code	Factor	
0x00	1.00	
0x01	1.06	
...	$6.25 \frac{GFZ}{31}$	
0x1F	6.25	

Table 38: Fine Gain Factor CH0

Offset Calibration CH0

The offset reference source is selected with VOS0. The offset compensation is set with OR0 and OF0 (see Offset Calibration CH1 and CH2 for further information). When selecting the self-tracking VDC offset reference, the source VDC1 of channel 1 is used.

VOS0		Addr. 0x13, bit 5:4
Code	Source	
0x0	0.05 · V(ACO)	
0x1	0.5 V	
0x2	0.25 V	
0x3	VDC (= VDC1)	

Table 39: Offset Reference Source CH0

OR0		Addr. 0x12, bit 1:0
Code	Factor	
0x0	1	
0x1	2	
0x2	6	
0x3	12	

Table 40: Coarse Offset Factor CH0

OF0		Addr. 0x12, bit 7:2
Code	Factor	
0x00	0	
0x01	0.0322	
...	+ Code/31	
0x1F	1	
0x20	0	
0x21	− 0.0322	
...	− (Code − 32)/31	
0x3F	− 1	

Table 41: Fine Offset Factor CH0

SIGNAL LEVEL CONTROL and SIGNAL MONITORING

iC-MSC's signal level control can keep the input signals for the sine/cosine signal conditioning circuit constant, regardless of temperature and aging effects, when using control output ACO to track the sensor supply.

ADJ(6:5) presets the output current range of pin ACO, the control's highside current source output, and ADJ(8:7) defines its control mode.

The control's operating range and the resulting internal signal amplitude are both monitored and thus can be used for error messaging.

ADJ(6:5) Addr. 0x10, bit 5:4	
Code	Current Range
00	0.05 mA ... 5 mA
01	0.1 mA ... 10 mA
10	0.25 mA ... 25 mA
11	0.5 mA ... 50 mA
Note	The range defines the ACO output's guaranteed driving capability. Refer to Elec. Char. No. 602 for the corresponding short-circuit current.

Table 42: ACO Output Current Range (applies for control modes and constant current source)

ADJ(8:7) Addr. 0x10, bit 7:6	
Code	Operating Mode
00	Sine/cosine square control
01	Sum control
10	Constant current source
11	Not permitted (device test only)

Table 43: ACO Output Control Mode

Deadband Control

Using deadband control mode (refer to ADJMODE), a deviation of the signal level is balanced only if the configured control deadband is exceeded (refer to ADJ(10:9)). Using this hysteresis, the square control's influence on the sensor's signal quality (THD) can be significantly reduced.

Using continuous control mode, any level deviation will be balanced immediately over the ACO output.

ADJMODE Addr. 0x0F, bit 6	
Code	Function
0	Deadband control
1	Continuous control
Note	This function is available with <i>square control</i> and <i>sum control</i> modes.

Table 44: Type of Control

ADJ(10:9) Addr. 0x15, bit 1:0	
Code	Hysteresis to setpoint
0x0	2.5%
0x1	5%
0x2	7.5%
0x3	10%

Table 45: Control Deadband

Square Control Mode

The standard control mode is *square control* which uses $(\sin^2 + \cos^2)$ to adjust the ACO output current. ADJ(4:0) determines the internal signal amplitudes within the closed-loop control and, simultaneously, the amplitude monitoring thresholds. The ideal setting is when the sin/cos test signals available in operating mode *Calibration 2* are at 500 mVpp.

ADJ(4:0) Addr. 0x10, bit 3:0; Addr. 0x0F, bit 7	
Code	Square control ADJ(8:7) = 00
0x00	$V_{pp}() \approx 300 \text{ mV} (60 \%)$
0x01	$V_{pp}() \approx 305 \text{ mV} (61 \%)$
...	... $\approx 300 \text{ mV} \frac{77}{77 - (1.25 * Code)}$
0x19	$V_{pp}() \approx 500 \text{ mV} (101 \%)$
...	...
0x1F	$V_{pp}() \approx 600 \text{ mV} (120 \%)$

Table 46: Square Control Setpoint (internal sin/cos signal amplitude)

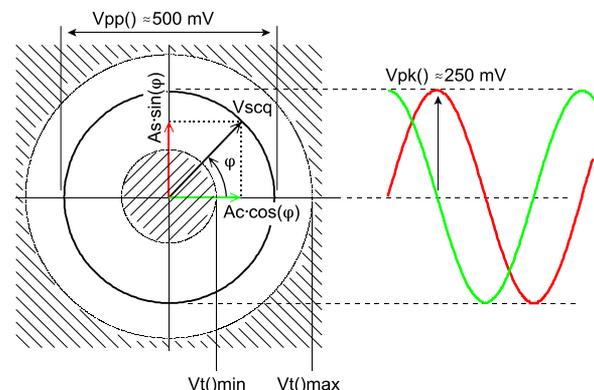


Figure 11: Internal signal monitoring and test signals in mode *Calibration 2* (example for ADJ(8:0) = 0x19);

The signal monitoring thresholds are tracked according to ADJ(4:0) and fit for *square control mode*. When using *sum control mode* a different operating point may be required for which the monitoring thresholds may

not be suitable. In this case signal monitoring should be disabled via the error mask (see EMASKA etc.).

Signal monitoring and thresholds			
ADJ (4:0)	Vt()min ... max	ADJ (4:0)	Vt()min ... max
0x00	120 mV...390 mV	0x19	200 mV ...650 mV
0x01	122 mV...397 mV
...	...	0x1F	240 mV...780 mV
Notes	All values nominal, see also Elec. Char. Nos. 607, 608		

Table 47: Signal Monitoring

Note: Following power up and after the configuration data has been read successfully, the sine/cosine square control starts operation from a zero output current.

Note: Excessive input signals or internal signal clipping can interfere with the control operation, so that the preset operating point may not be reached (upon power up) or maintained (upon disturbances). Use Control Error 2 and Signal Error 1 for monitoring and configuring EMASKA accordingly.

Sum Control Mode

With *sum control* mode selected, the DC references (VDC1 + VDC2) are used to adjust the output current of pin ACO.

ADJ (4:0)		Addr. 0x10, bit 3:0; Addr. 0x0F, bit 7
Code	Sum control ADJ(8:7) = 01	
0x00	VDC1 + VDC2 \approx 245 mV	
0x01	VDC1 + VDC2 \approx 249 mV	
...	...	$\approx 245mV \frac{77}{77-(1.25*Code)}$
0x1F	VDC1 + VDC2 \approx 490 mV	

Table 48: Sum Control Setpoint (DC average)

Constant Current Source

The *constant current source* is intended for signal conditioning purposes, i.e. for the adjustment of gain, offset and phase correction values independent of signal level controlling.

ADJ (4:0)		Addr. 0x10, bit 3:0; Addr. 0x0F, bit 7
Code	Constant current source ADJ(8:7) = 10	
0x00	I(ACO) \approx 3.125% Isc(ACO)	
0x01	I(ACO) \approx 6.25% Isc(ACO)	
...	...	$\approx 3.125% * (Code + 1) * Isc(ACO)$
0x1F	I(ACO) \approx 100% Isc(ACO)	
Note	The setpoint defines the ACO output current relative to Isc(ACO), the output's short-circuit current (see Elec. Char. No. 602) which depends on the selected range.	

Table 49: Current Source Setpoint (ACO output current)

MONITORING AND ERROR OUTPUT

The following table gives the errors which can both be recognized by iC-MSC and enabled either for messaging, output shutdown or protocol in the EEPROM.

Mask EMASKA stipulates that errors should be signaled at pin ERR, mask EMASKO determines whether the line drivers are to be shutdown or not (with PDMODE defining reactivation) and mask EMASKE governs the storage of error events in the EEPROM.

EMASKA	Addr. 0x14, bit 6:0
EMASKO	Addr. 0x16, bit 6:0
EMASKE	Addr. 0x18, bit 2:0; Addr. 0x17, bit 7:4
Bit	Error Event
6*	Configuration error (SDA or SCL pin error, no acknowledge signal from EEPROM or invalid checksum);
5	Excessive temperature warning
4	External system error
3	Control error 2: range at max. limit
2	Control error 1: range at min. limit
1	Signal error 2: clipping
0	Signal error 1: loss of signal (wrong s/c phase, poor differential amplitude, may also result from excessive input signals or internal signal clipping)
EMASKA	Error Mask Alarm Output ERR
1	Enable: event changes state of pin ERR (if EMASKO does not disable the output function).
0	Disable: event does not affect pin ERR.
*Note	EMASKA(6): Pin ERR can not pull low on config. error. Use EPH = 1 for high-active error logic.
EMASKO	Error Mask Driver Shutdown
1	Enable: event resets pin ACO to the 5 mA range, tristates the output drivers and pin ERR (i.e. low-active error messages can not be displayed)
0	Disable: output functions remain active
*Note	EMASKO(6) = 1 (ROM bit): The output drivers remain high impedance (tristate) when cycling power. Program EMASKO(6) = 0 to EEPROM. This allows to reactivate disabled output drivers by toggling bit RUN (set zero, then one). If set to 1, the driver shutdown persists and can not be resolved.
EMASKE	Error Mask EEPROM Savings
1	Enable: event will be latched
0	Disable: event will not be latched
*Note	Program EMASKE(6) = 0 to EEPROM. This avoids conflicts with I ² C programming adapters which are not multi-master capable.

Table 50: Error Masking

Error Input/Output: pin ERR

Pin ERR is operated by a current-limited open-drain output driver and has an internal pull-up which can be

disabled. The output logic (low or high active) is configured by EPH, and the minimum indication time by EMTD.

Pin ERR also acts as an input for error messages of the external system. This function requires EPH = 0 and an external error being low active. Pin ERR can also switch iC-MSC to test mode, for which a voltage of larger than VTMon must be applied (see page 22).

EPH			Addr. 0x15, bit 2
Code	State with error	State w/o error	
0*	active low	high impedance (evaluation of low active external system error)	
1	high impedance (or optional pull-up)	active low	
Note	*) Pin ERR is disabled during driver shutdown and cannot indicate errors in this case.		

Table 51: Alarm Output ERR and I/O Logic

EMTD				Addr. 0x15, bit 5:3
Code	Indication Time	Code	Indication Time	
0x0	0 ms	0x4	50 ms	
0x1	12.5 ms	0x5	62.5 ms	
0x2	25 ms	0x6	75 ms	
0x3	37.5 ms	0x7	87.5 ms	

Table 52: Min. Indication Time, Alarm Output ERR

EPU		Addr. 0x17, bit 2
Code	Function	
0	No internal pull-up	
1	Internal 300 µA pull-up current source active	

Table 53: Pull-Up Enable, Alarm Output ERR

Excessive Temperature Warning

Exceeding the temperature warning threshold T_w (corresponds to T_2 , refer to Temperature Sensor, page 20) can be signaled at pin ERR or used to shut down the output drivers (via mask EMASKO). The temperature warning is cleared when the temperature falls below $T_w - T_{hys}$.

Note: If the temperature shutdown threshold $T_{off} = T_w + \Delta T$ is exceeded, the output drivers are shut down independently of EMASKO. For ΔT refer to Elec. Char. E06.

Analog Output Drivers Shutdown

PDMODE	
Code	Function
0	Driver shutdown terminates with the error event
1	Permanent driver shutdown until cycling power

Table 54: Driver Activation

Error Protocol

Out of the errors enabled by EMASKE both the first error (under ERR1) and last error (under ERR2) which occur after the iC-MSC is powered up are stored in the EEPROM.

The EEPROM also has a memory area in which all occurring errors can be stored (ERR3). Only the fact that

an error has occurred can be recorded, with no information as to the time and count of appearance of that error given. Error recording can be used to statistically evaluate the causes of system failure, for example.

ERR1	
ERR2	
ERR3	
Bit	Error Event
6:0	Assignment according to EMASKE
Code	
Code	Function
0	No event
1	Registered error event

Table 55: Error Protocol

ANALOG OUTPUT DRIVERS

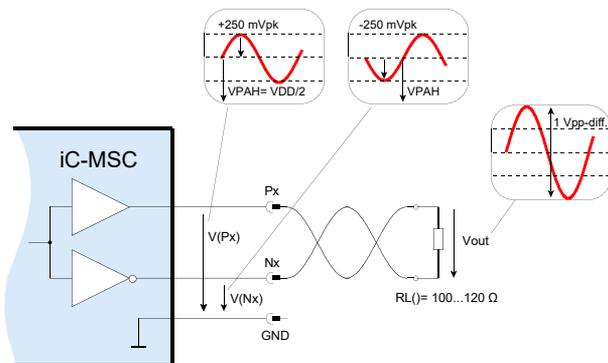


Figure 12: Output amplitude and offset according to Elec. Char. 502 and 503.

iC-MSC outputs differential 1 Vpp signals with approx. 2.5 V in offset onto the transmission cable, which is terminated with 100 Ω or 120 Ω at the receiver end (PLC).

The output drivers are shut down (tristated) in case of excessive temperature (see page 32), or when reverse polarity is detected (see section Reverse Polarity Protection, page 33).

Using EMASKO for error masking, further events can be selected to shut down the output drivers (see Table 50). Using PDMODE, the duration of a shutdown can be prolonged until power was cycled (see Table 54).

If there is no EEPROM or no valid configuration provided on power up, the output drivers will not be enabled.

REVERSE POLARITY PROTECTION

The analog output drivers of iC-MSC are protected against reverse polarity and short-circuiting. A defective or wrongly connected device cable causes no damage, neither to iC-MSC nor to the components protected against reverse polarity by VDDS and GNDS.

The following pins feature reverse polarity protection: PC, NC, PS, NS, PZ, NZ, ERR, VDD, GND and ACO (as long as GNDS is only loaded relative to VDDS). The maximum voltage difference between these pins should not exceed 6 V (8 V for pin ERR).

Reverse polarity is permanently monitored and detected if the voltage at a protected pin undershoots the ground potential at GND.

If the state of reverse polarity is resolved, iC-MSC reboots from the EEPROM and enables the output drivers.

Note: When iC-MSC is linked to a PLC and does not enable its output drivers on power up, a negative line potential could be the root cause. Refer to Application Hints, page 34, for details and recommended countermeasures.

APPLICATION HINTS

Connecting MR sensor bridges for safety-related applications

For safety-related applications iC-MSC requires an external overvoltage protection of supply VDD (Zener diode with fuse, for instance) and external pull-down resistors at the inputs X3 to X6 towards GNDs (of up to 100 kΩ).

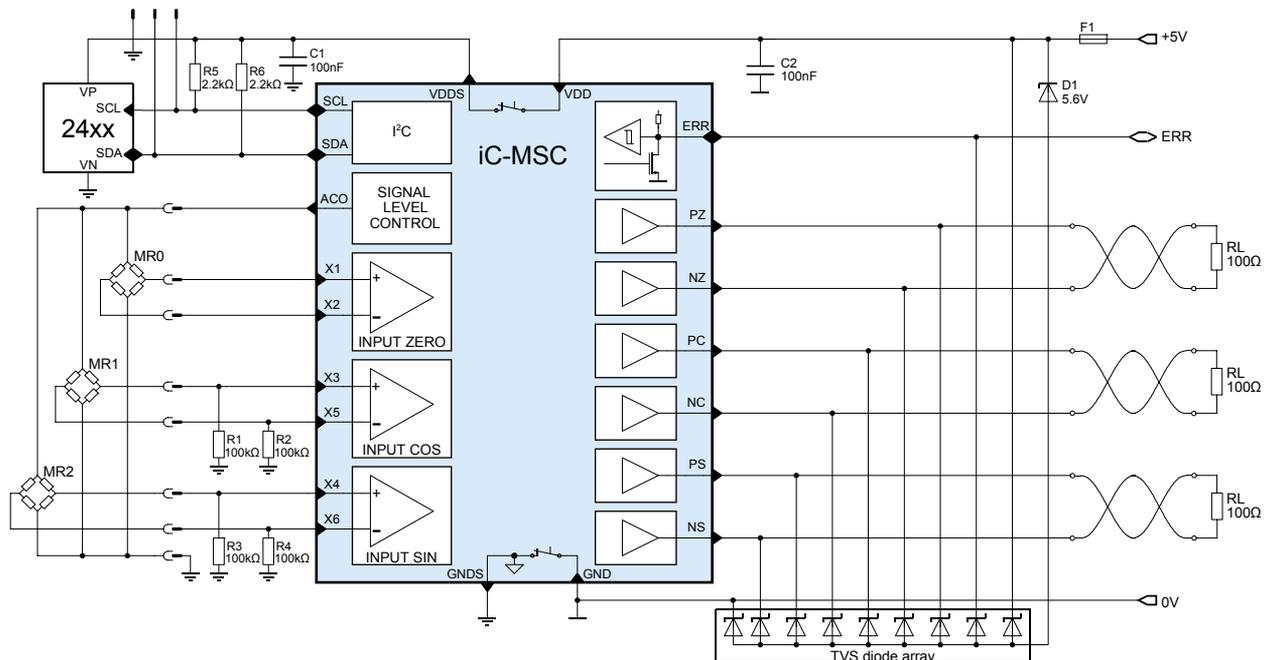


Figure 13: Example circuit for safety-related applications.

PLC Operation

There are PLCs with a remote sense supply which require more time for the voltage control to settle. At the same time the PLC inputs can have high-impedance resistances relative to an internal, negative supply voltage which define the input potential for open inputs.

In this instance iC-MSC's reverse polarity protection feature can be activated as the outputs are tristate during the start phase and the resistances in the PLC determine the pin potential. During the start phase

neither the supply VDD nor the output pins, which are also monitored, must fall to below ground potential (pin GND), otherwise the device will not be configured and the outputs remain permanently set to tristate.

Note: In order to ensure that iC-MSC starts with the PLCs mentioned above pull-up resistors can be used in the encoder. Values of 100 kΩ are usually sufficient; it is, however, recommended that PLC specifications be specifically referred to here.

iC-MSC SIN/COS SIGNAL CONDITIONER WITH FAIL-SAFE 1 Vpp LINE DRIVER



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REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2018-04-17	All	Initial release	

Rel.	Rel. Date*	Chapter	Modification	Page
A2	2018-08-15	PACKAGING INFORMATION	Footnote: value of bypass cap Package TSSOP20-TP: update of pinout, and dimensions added	4, 6
		ELECTRICAL CHARACTERISTICS	Items 102, 202: formula corrected Items 103, 203: conditions and limits Items 601, 602: conditions reduced	9
		ABSOLUTE MAXIMUM RATINGS	Item G001, G002: condition added Item G004, G005: items added	8
		BIAS CURRENT SOURCE AND TEMPERATURE SENSOR CALIBRATION	Measurement of IBN: note box updated Temperature sensor calibration: description updated Table 15: correction of formula, footnote updated	20
		SIGNAL LEVEL CONTROL and SIGNAL MONITORING	Table 42: min. range and note added Table 49: note added	30, 31
		ERROR MONITORING AND ALARM OUTPUT	Table 55: corrected to bits 6:0	33

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2020-08-19	BLOCK DIAGRAM	Update of block diagram, adaption of section titles	1ff
		DESCRIPTION	Note box added	2
		ELECTRICAL CHARACTERISTICS	Item 001: condition completed; items 102, 202: formula corrected; Item 502: condition added Item 503, D13: added as new items	9ff
		CONFIGURATION REGISTERS	Note added on DEVID programming	15
		SERIAL I ² C INTERFACE	Update of description, Figure 1 added, Table 5: note updated, Table 7 added, note and attention boxes added; Section EEPROM Device Selection: Table 8 max. size corrected, update of description, note boxes added; Section I ² C Slave Mode: Table 11: update of content	17ff
		ANALOG OUTPUT DRIVERS	Section added	33
		REVERSE POLARITY PROT.	Description updated	33
		ORDERING INFORMATION	Listing updated	36

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* Release Date format: YYYY-MM-DD

iC-MSC SIN/COS SIGNAL CONDITIONER WITH FAIL-SAFE 1 Vpp LINE DRIVER



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ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-MSC	20-pin TSSOP with Thermal Pad RoHS compliant	Temperature range -40 °C to +125 °C	iC-MSC TSSOP20-TP
	32-pin QFN, 5 mm x 5 mm, thickness 0.9 mm, RoHS compliant	Temperature range -40 °C to +125 °C	iC-MSC QFN32-5x5
Evaluation Board			iC-MSC EVAL MSB1D

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