iC-NE
LIGHT-GRID PULSE RECEIVER

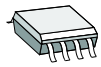
FEATURES

- Photoelectric amplifier adapted to standard photodiodes
- Built-in bandpass filter with 300 kHz center frequency
- Differential current-signal output with open drain low-side drivers
- Nonlinear transfer function results in wide dynamic range of 100 nA to 1.5 mA for pulsed photocurrents
- Fast flash recovery time of max. 30 µs
- Recovery time below 10 µs for excessive photocurrents of up to 1.8 mA
- 3-step shift register and control logic
- Compatible to CMOS levels
- Single 5 V supply
- Low standby current; circuit activation by input data
- Power-down reset
- Suited for high-risk applications according to IEC 61496-1
- ESD protection
- **Option:** extended temperature range of -20 to 85 °C

APPLICATIONS

- Light curtains
- Light barriers
- Electro-sensitive protective equipment (ESPE)

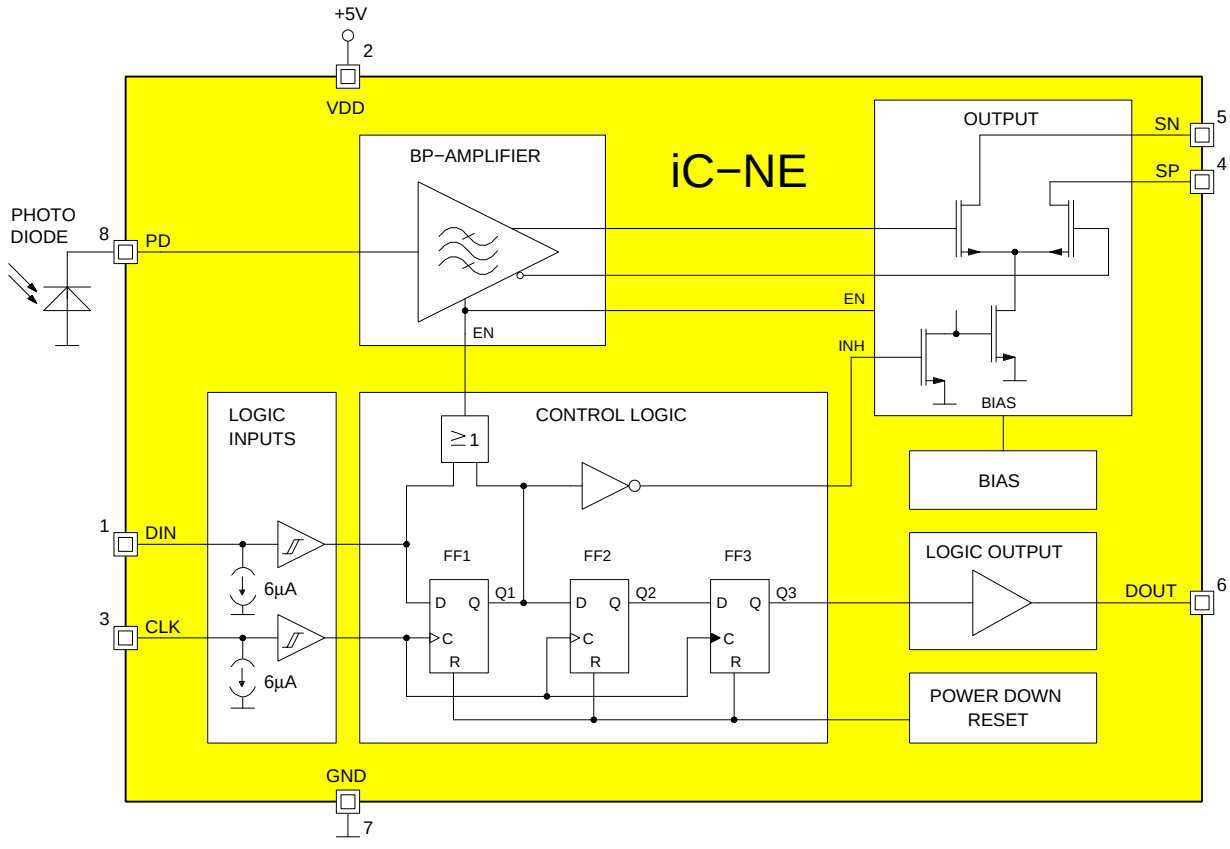
PACKAGES



SO8

MSOP8

BLOCK DIAGRAM



DESCRIPTION

The iC-NE device is a light-grid receiver IC. Typical applications cover light curtains, light barriers and electro-sensitive protective equipment in general.

Integrated on a single silicon chip the iC-NE contains a bandpass amplifier with a center frequency of typically 300 kHz, a differential current-signal output plus control logic to activate the amplifier and the output. Deactivated, the current consumption is very low and the current-signal outputs SN and SP are switched to high impedance (zero current).

The logic consists of a three-stage shift register in which the first two stages are triggered by the rising edge of the clock input CLK. The third flipflop is triggered with the falling clock edge, which produces an artificial delay in order to avoid race conditions when shifting the input data via the serial output to the next device in the chain.

The bandpass amplifier is activated when DIN reads a logical *1*. The output stage still remains disabled (zero current) until the output of the first flipflop changes to *1*. This activates the bias for the complete signal path from light detection to the differential current output. The differential outputs SP and SN are powered up to an equal current, as far as the attached photodiode does not receive any changes in light.

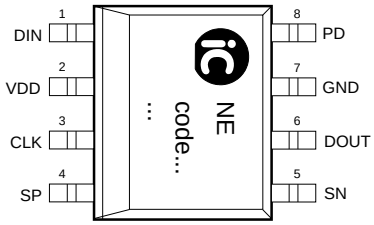
The rising edge of a received light pulse (which produces an increase of photocurrent), causes the output current at SP to increase and at SN to decrease by an equal value. The sum of I(SP) + I(SN) is kept constant. For light curtain applications in which only one device is activated at a time, the outputs SN and SP can be attached to a two-wire bus.

After processing the serial input data at DIN, the activated amplifier and output automatically return to standby mode, when the clock input receives the second rising edge. Therefore, a chain circuitry with multiple beams has to be set up with just a single data bit within a shift cycle.

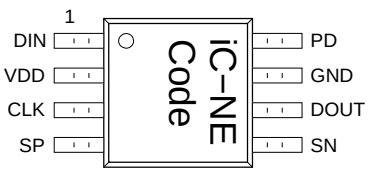
The IC contains protective diodes to prevent destruction by ESD. Logic input pins feature Schmitt-trigger characteristics for high noise immunity. All pins are short-circuit proof.

PACKAGES SO8, MSOP8 to JEDEC Standard

PIN CONFIGURATION SO8
(top view)



PIN CONFIGURATION MSOP8
(top view)



PIN FUNCTIONS

No.	Name	Function
1	DIN	Data Input
2	VDD	+5 V Supply Voltage
3	CLK	Clock Input
4	SP	Pos. Differential Current Output
5	SN	Neg. Differential Current Output
6	DOUT	Data Output
7	GND	Ground
8	PD	Photocurrent Input, photodiode cathode

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.5	7	V
G002	V()	Voltage at DIN, CLK, DOUT, SN, SP, PD		-0.5	VDD + 0.5	V
G003	Vd()	ESD Susceptibility at DIN, CLK, DOUT, PD, SN, SP	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G004	Tj	Junction Temperature		-40	150	°C
G005	Ts	Storage Temperature		-40	150	°C

THERMAL DATA

Operating Conditions: VDD = 5 V ±10%

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended temperature range of -20 to 85 °C on request)		0		70	°C

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 5 V ±10%, V(SN, SP) = VDD − 2 V...VDD, Tj = -20...85 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage Range		4.5		5.5	V
002	VDD	Required Supply Voltage for logic function	decreasing voltage VDD	1.7			V
003	I(VDD)	Supply Current in VDD (Standby)	DIN = lo, CLK = hi or lo: BP-amplifier and output stage disabled, logic levels: lo = 0...0.45 V, hi = VDD − 0.45 V...VDD			60	µA
004	I(VDD)	Supply Current in VDD	EN = hi: BP-amplifier activated, INH = hi: output stage disabled, I(PD) = -15...0 µA Tj = 27 °C		 0.3	0.5 	mA mA
005	I(VDD)	Supply Current in VDD	EN = hi, INH = lo: BP-amplifier and output stage activated Tj = 27 °C		 1.1	3.0 	mA mA
006	VDDon	Turn-on Threshold VDD (Power-on release)				4.2	V
007	VDDoff	Undervoltage Threshold at VDD (Power-down reset)	decreasing voltage VDD	2.6			V
008	VDDhys	Hysteresis	VDDhys = VDDon − VDDoff	200		500	mV
009	Vc()hi	Clamp Voltage hi at DIN, CLK, DOUT, PD, SN, SP	Vc()hi = V() − VDD, I() = 1 mA	0.4		1.25	V
010	Vc()lo	Clamp Voltage lo at DIN, CLK, DOUT, PD, SN, SP	I() = -10 mA, VDD = 0 V, other pins open	-1.25		-0.4	V
Bandpass Amplifier and Output Stage PD, SN, SP							
101	C(PD)	Permissible capacitance at PD				100	pF
102	V(PD)	Voltage at PD			0.9		V
103	I(PD)	Permissible DC-photocurrent in PD (ambient light supression)		-15		0	µA
104	I(PD)mg	Monotone Gain Range of I(PD)pk	|Ipn()| increases or remains constant when |I(PD)pk| increases (see Fig. 3)	-1.5		0	mA
105	twhi	Permissible Photocurrent Pulse Duration	(see Fig. 3, 4)	1.0			µs
106	twlo	Permissible Photocurrent Pause Duration	2^{nd} Gpk ≥ 90% 1^{st} Gpk resp. of single pulse (see Fig. 4)	2.0			µs
107	trec	Flash Recovery Time	I(PD)pk = -1.8 mA			10	µs
108	trec	Power-Flash Recovery Time	I(PD)pk = -5 mA, magnitude of photocurrent integral equals 15 mAs			30	µs
109	Gpk	Pulse Current Gain	Gpk = (Ipn() − IO ∗ ISUM) / I(PD)pk; I(PD)dc = -15...0 µA, I(PD)pk = -1...-0.1 µA, tr = tf = 0.5 µs, twpk = 1 µs (see Fig. 3)	360	490	620	
110	fl	Lower Cut-off Frequency (-3 dB)	I(PD)dc = -15...-2.5 µA, I(PD)ac = 5 µApp sinusoidal waveform	65	100	155	kHz
111	fh	Upper Cut-off Frequency (-3 dB)	I(PD)dc = -15...-2.5 µA, I(PD)ac = 5 µApp sinusoidal waveform	380	530	750	kHz
112	fΔ	Bandwidth (-3 dB)	fΔ = fh − fl	270	430	670	kHz
113	V()out	Permissible Output Voltage Range at SN, SP with reference to VDD	V()out = VDD − V()			2	V
114	ISUM	Output currents I(SN) + I(SP)	V(SN, SP) = 4...5 V Tj = 27 °C	4.9	 7.5	9.7	mA mA
115	IO	Relative Current Offset	IO = (I(SN) − I(SP)) / ISUM; I(PD) = 0 Tj = -20 °C	-10 -15		10 15	% %
116	Ilk	Leakage Current I(SN) + I(SP)	output disabled			4.0	µA
117	Idlk()	Differential Leakage Current	Idlk() = I(SN) − I(SP); I(PD)pk = -600 µA, twhi = 3 µs, output disabled (see Fig. 3)	-0.1		0.1	µA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 5 V ±10%, V(SN, SP) = VDD − 2 V...VDD, Tj = -20...85 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
118	Ipn()	Differential Output Current	Ipn() = I(SN) − I(SP); I(PD)pk = -10 µA (see Fig. 3)	-7.0	-5.0	-3.0	mA
119	Ipn()	Differential Output Current	Ipn() = I(SN) − I(SP); I(PD)pk = -100 µA (see Fig. 3)	-9.7	-7.3	-4.0	mA
120	INoise	Differential Output Current Noise (RMS)	I(PD)dc = -15 µA, Rgen = 500 kΩ, no additional filter, Tj = 27 °C (see Fig. 5)		5		µA
121	INoise	Differential Output Current Noise (RMS)	I(PD)dc = -15 µA, Rgen = 500 kΩ, with BP-filter 50 kHz...1.2 MHz, Tj = 27 °C (see Fig. 5)		3.5		µA
122	tp()IDCon	Output Stage Turn-on Delay: CLK lo → hi to 90% I(SN), I(SP)	I(PD)dc = -15 µA...0, I(PD)ac = 0 (see Fig. 4)			3.0	µs
123	tp()IDCoff	Output Stage Turn-off Delay: CLK lo → hi to 10% I(SN), I(SP)	I(PD)dc = -15 µA...0, I(PD)ac = 0 (see Fig. 4)			3.0	µs
Control Inputs DIN, CLK							
201	Vt()hi	Threshold Voltage hi				66	%VDD
202	Vt()lo	Threshold Voltage lo		33			%VDD
203	Vhys()	Schmitt-Trigger Input Hysteresis		400			mV
204	Ipd()	Pull-Down Current	V() = 1 V...VDD Tj = 27 °C	3	 6	12	µA µA
Output Buffer DOUT							
301	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(DOUT); I() = -4 mA			0.4	V
302	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	V
303	Isc()hi	Short-Circuit Current hi	V() = 0 V Tj = 27 °C	-100	 -40	-25	mA mA
304	Isc()lo	Short-Circuit Current lo	V() = VDD Tj = 27 °C	25	 40	100	mA mA
305	tr()	Rise Time	CL() = 50 pF Tj = 27 °C		 20	60	ns ns
306	tf()	Fall Time	CL() = 50 pF Tj = 27 °C		 20	60	ns ns
Timing Characteristics							
401	tplh(CLK-DOUT)	Propagation Delay: CLK hi → lo until DOUT lo → hi	CL(DOUT) = 50 pF (see Fig. 2) Tj = 27 °C		 26	60	ns ns
402	tphl(CLK-DOUT)	Propagation Delay: CLK hi → lo until DOUT hi → lo	CL(DOUT) = 50 pF (see Fig. 2) Tj = 27 °C		 25	60	ns ns

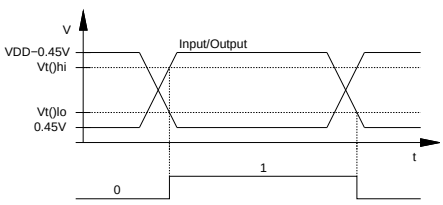


Figure 1: Reference levels

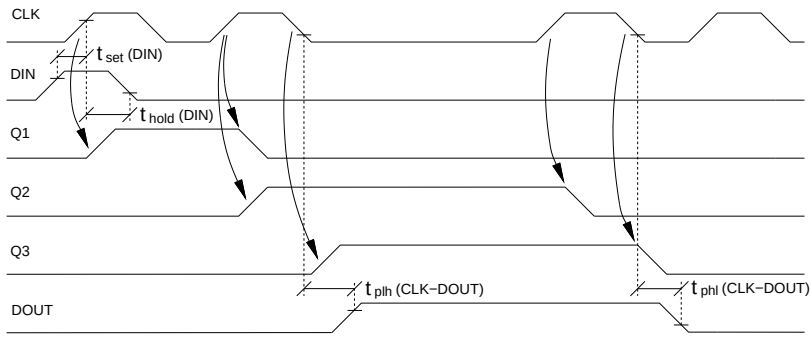


Figure 2: Timing characteristics

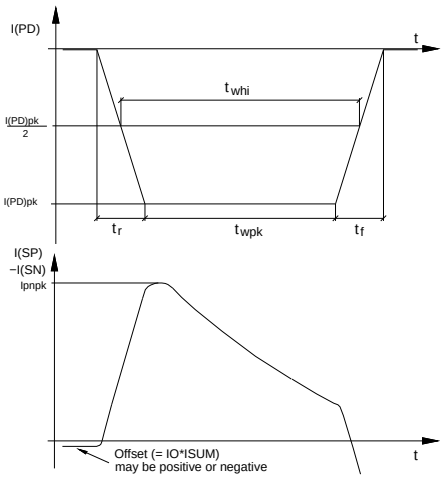


Figure 3: Differential output current pulse at SP and SN versus input current pulse at PD

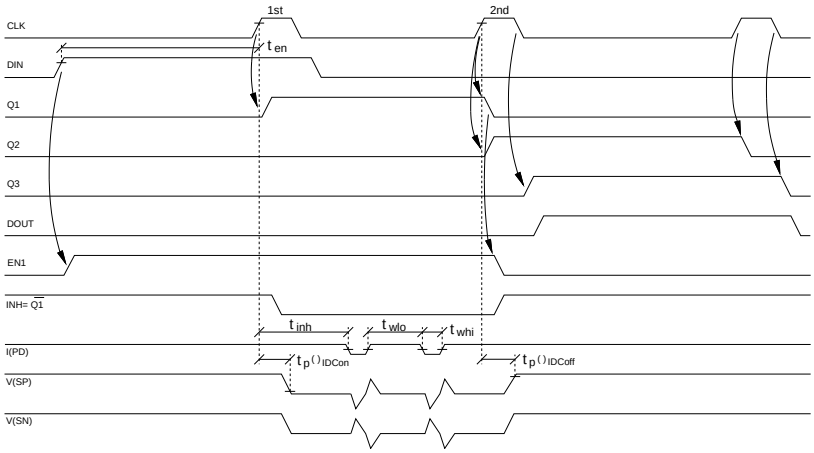


Figure 4: Timing characteristics (analogue section), outputs SP and SN with resistors to VDD

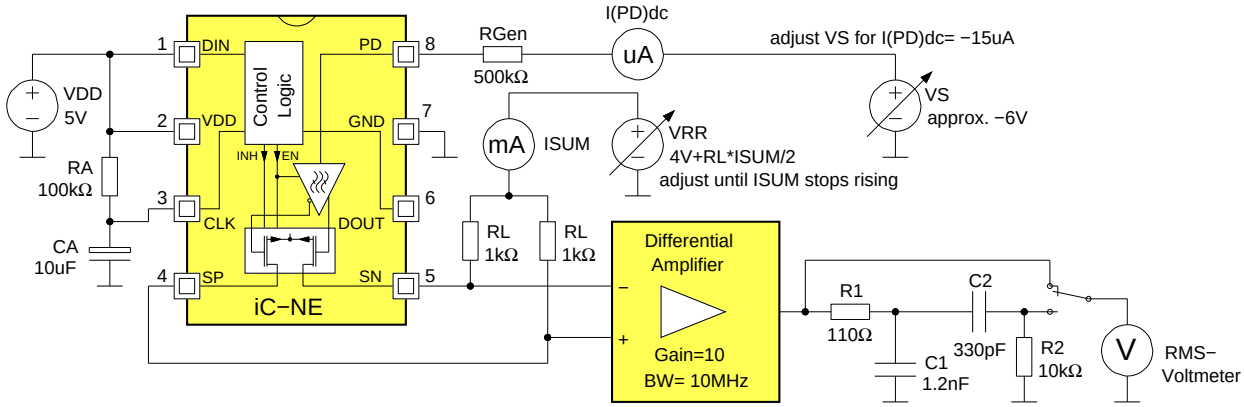


Figure 5: Noise measurement circuit

OPERATING REQUIREMENTS: Logic

Operating Conditions: VDD = 5 V ±10%, Ta = 0...70 °C, CL() = 50 pF,
input levels lo = 0...0.45 V, hi = VDD − 0.45 V...VDD, see Fig. 1 for reference levels and waveforms

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I001	ten	Activation Time: DIN lo → hi to CLK lo → hi	Standby to amplifier operation (see Fig. 4)	10		µs
I002	tinh	Output Activation Time: 1st CLK lo → hi until output ready to report	Sufficient decay of transient differential output current: |I(SN) − I(SP) − IO ∗ ISUM| ≤ 20 µA (see Fig. 4)	5		µs
I003	tset	Setup time: DIN stable before CLK lo → hi	(see Fig. 2)	50		ns
I004	thold	Hold time: DIN stable after CLK lo → hi	(see Fig. 2)	50		ns
I005	fo	Permissible Frequency at CLK			10	MHz

APPLICATIONS INFORMATION

Signal Processing

Figures 6 and 7 show output signal I(SP) – I(SN) in *normal* drive and in extreme overdrive (with the photodiode and input amplifier in saturation).

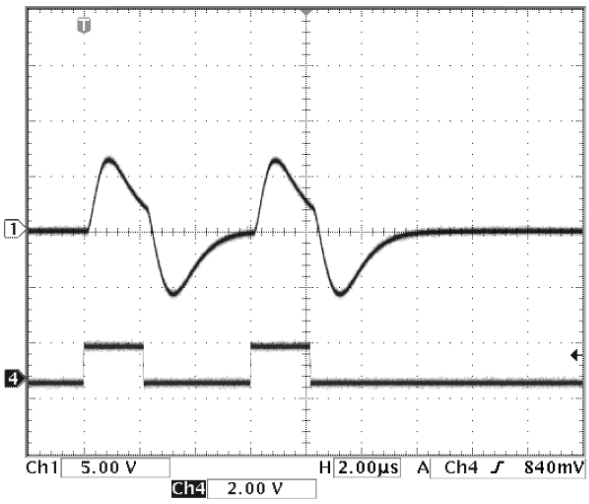


Figure 6: Regular input signals

It is clear from these diagrams that iC-NE, even when in overdrive, is not *blind* to a follow-on pulse. For evaluation purpose the response to the rising edge of the light pulse (i.e. the rising edge of the output signal) is to be used as it is this edge alone, even in the most extreme overdrive, which yields definite results. Evaluating the falling edge of the output signal or the level of the negative output signal half-wave (the recovery process at the end of a light pulse) is generally not advised.

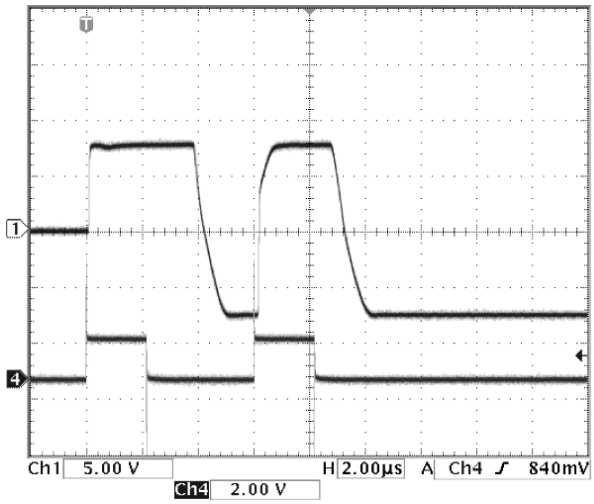


Figure 7: Excessive input signals

Light curtain

The circuit in Figure 8 shows iC-NE chained up to form a light curtain, where consecutive PIN diodes receive and evaluate clock-driven light pulses.

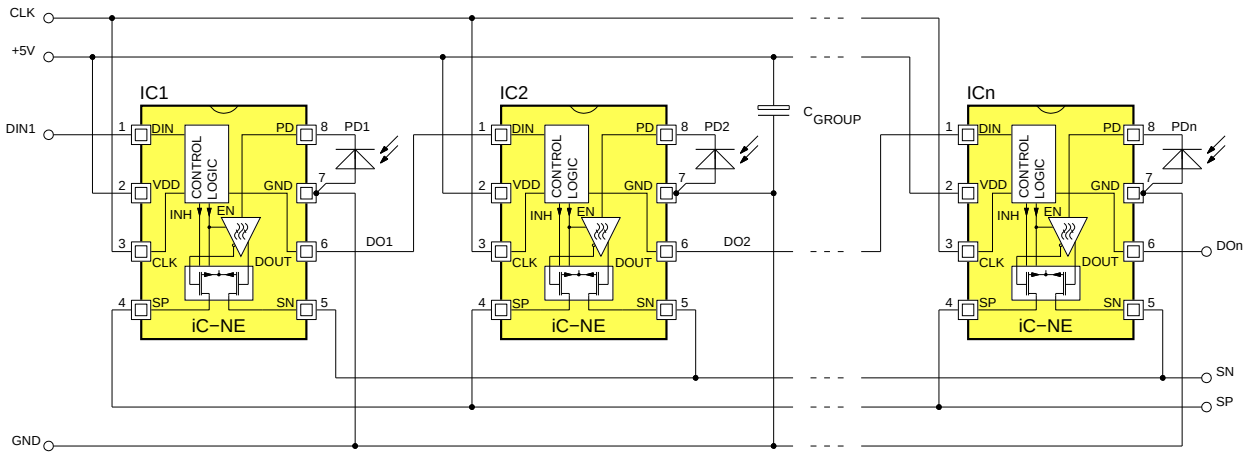


Figure 8: Schematic of a chain configuration

When discussing the function of iC-NE, it is assumed that all flip-flops in IC1...ICn have been reset, for example after the operating voltage has been switched on.

The signal DIN1 = hi activates the IC1 bandpass amplifier and the bias of the differential output stage. Outputs SP and SN remain tri-state until the rising CLK edge shifts in the input hi signal.

With no AC photocurrent fractions in the receiver photodiode, approximately equal currents are drawn in SP and SN. Within a time $t_{inh} \geq 5\,\mu s$, the transient differential currents in the output stage, caused by switching the chip on, have decayed, and iC-NE is ready to receive.

Current is drawn from PD (IC1) by a light pulse on the photodiode PD1, and the currents at outputs SP and SN react as shown in Figure 9: I(SP) rises and returns to the initial value with a time constant determined by the lower bandpass amplifier cut-off frequency, as long as the photodiode is constantly illuminated. When the light pulse decays, the current in SP first sinks and then ramps up to the standby value. The current in SN has a mirror-imaged time dependence, as the sum I(SP) + I(SN) is constant.

With DIN1 = 0, the next rising CLK edge resets FF1 and turns off the currents in the differential output stage. Simultaneously, FF1 sends the stored information to FF2. FF3 also accepts this information with the trailing CLK edge and activates the bandpass amplifier and the bias in the next device, IC2, via the output driver. The pulse diagram is also valid for the subsequent components in the chain, i.e. the ICs arranged as a light curtain form a clock-driven shift register which passes on the input information.

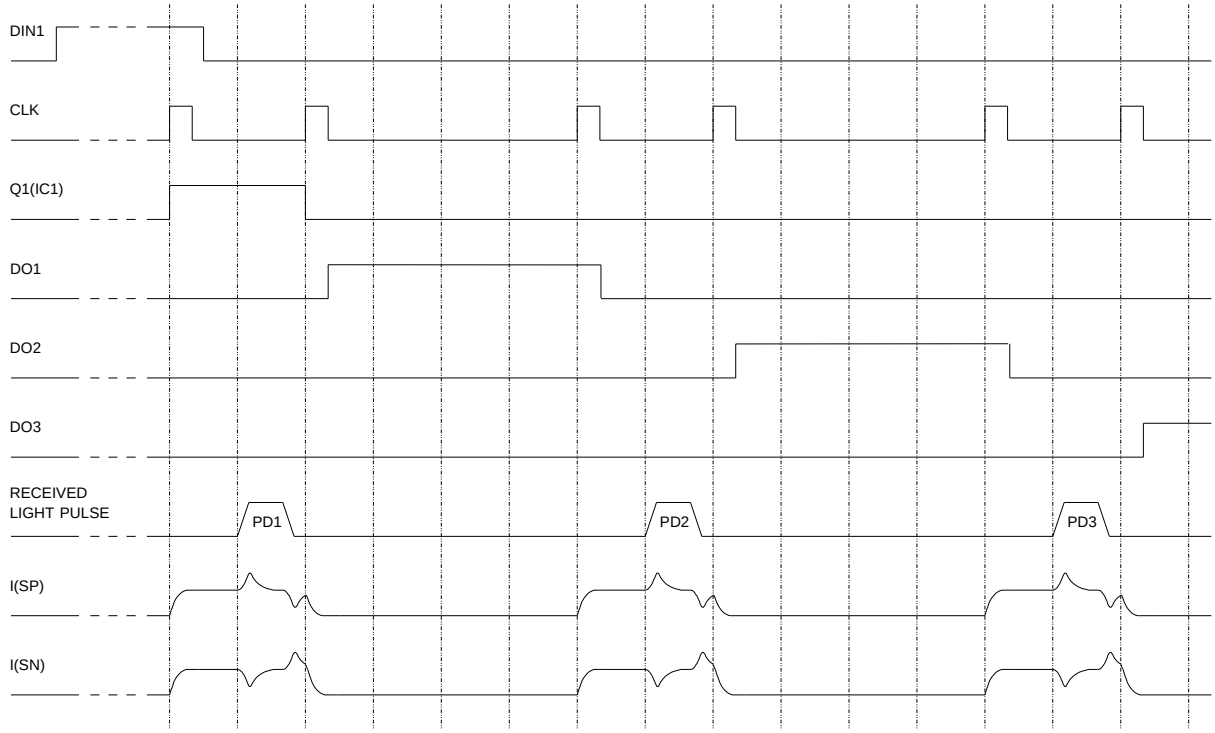


Figure 9: Signals for the chain configuration of Fig. 8

Light curtain PCB layout

The PCB layout for light curtain receivers is not critical. The photodiode anode should be directly connected to iC-NE's GND pin so that voltage drop caused by the chip's operating current is not coupled into the photocurrent signal.

As the power consumption is relatively small, only low-level back-up capacitors are required (typically 1 µF electrolytic capacitor in parallel to 47...100 nF ceramic capacitor). The ceramic capacitors should be placed at a distance of 7.5 cm apart, electrolytic capacitors at up to twice this distance. The number of receivers backed up as a group in this manner is irrelevant as only one device is activated and draws current at a time.

ORDERING INFORMATION

Type	Package	Order Designation
iC-NE	SO8 MSOP8	iC-NE SO8 iC-NE MSOP8

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (61 35) 92 92-0
Fax: +49 (61 35) 92 92-192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: http://www.ichaus.de/support_distributors.php