iC-LK
LIGHT-GRID PULSE RECEIVER

preliminary

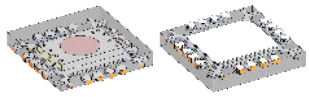
FEATURES

- Photoelectric amplifier with integrated photodiode
- Built-in bandpass filter with switchable centre frequency
- Differential current output with open-drain low-side drivers
- Nonlinear transfer function results in wide dynamic range for pulsed photocurrents
- Fast flash recovery time of max. 30 µs
- Recovery time below 10 µs even for excessive photocurrents within the input range
- Single 5 V supply
- Low standby current; circuit activation by input data
- ESD protection
- Function compatible to iC-NE (SEL = hi)

APPLICATIONS

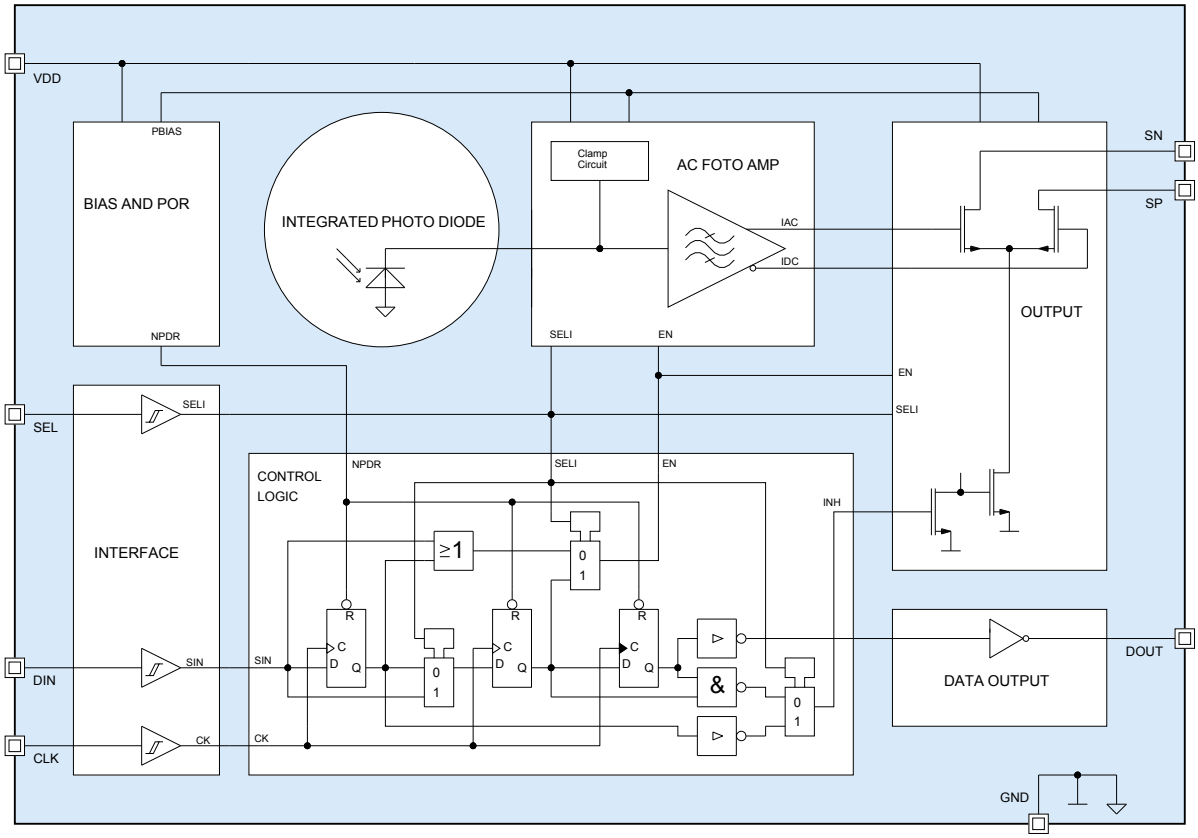
- Light curtains
- Light barriers
- Electro-sensitive protective equipment (ESPE)

PACKAGES



cQFN16 4 mm x 4 mm

BLOCK DIAGRAM



DESCRIPTION

The iC-LK is a light-grid receiver IC with integrated photo diode. Typical applications cover light curtains, light barriers and electro-sensitive protective equipment in general.

Integrated on a single silicon chip the iC-LK contains besides the photo diode a bandpass amplifier with a switchable centre frequency, a differential current output plus control logic to activate the amplifier and the output. Deactivated, the current consumption is very low and the current outputs SN and SP are switched to high impedance (zero current).

The control logic consists of a three-stage shift register in which the first two stages are triggered by the rising edge at the clock input CLK. The third flipflop is triggerred with the falling clock edge, which produces an artificial delay in order to avoid race conditions when shifting the input data via the serial output to the next device in the chain.

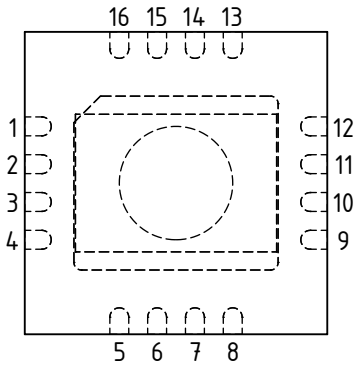
The rising edge of a received light pulse (which produces an increase of photocurrent), causes the output current at SP to increase and at SN to decrease by an equal value. The sum of I(SP) + I(SN) is kept constant. For light curtain applications in which only one device is activated at a time, the outputs SN and SP can be attached to a two-wire bus.

After processing the serial input data at DIN, the activated amplifier and output automatically return to standby mode, when the clock input receives the second rising edge. Therefore, a chain circuitry with multiple beams can be set up with just a single data bit within a shift cycle.

The IC contains protective diodes to prevent destruction by ESD. Logic input pins feature Schmitt trigger characteristics for high noise immunity. All pins are short-circuit proof.

PACKAGING INFORMATION cQFN16 4 mm x 4 mm

PIN CONFIGURATION cQFN16 4 mm x 4 mm

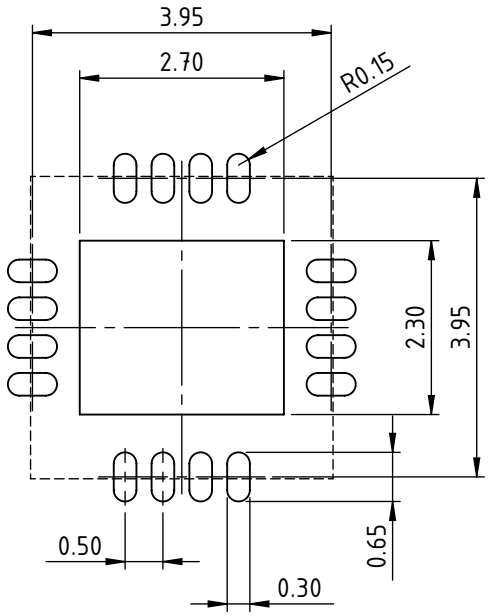


PIN FUNCTIONS

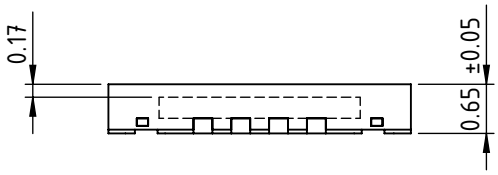
No.	Name	Function
1	VDD	+5 V Power Supply
2	GND	Ground
3	SN	Negative Differential Current Output
4	SP	Positive Differential Current Output
5		n/c
6		n/c
7		n/c
8		n/c
9	DOUT	Data Output
10	SEL	Mode Select (tie to GND or VDD)
11	CLK	Clock Input
12	DIN	Data Input
13		n/c
14		n/c
15		n/c
16		n/c

PACKAGE DIMENSIONS

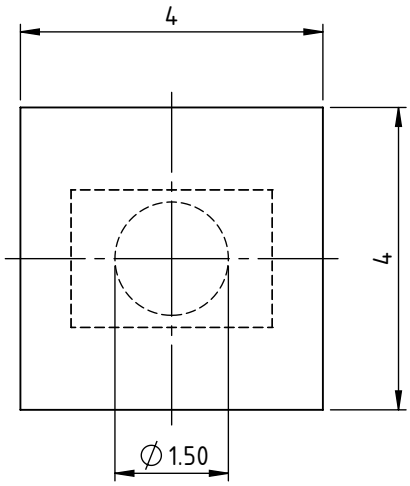
RECOMMENDED PCB-FOOTPRINT



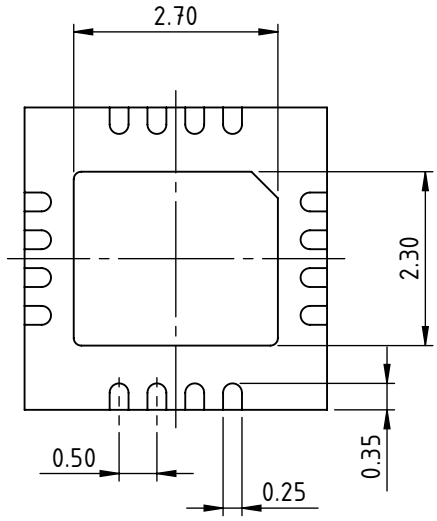
SIDE



TOP



BOTTOM



All dimensions given in mm.
Tolerance of sensor pattern: ±0.10mm (with respect to center of backside pad).

dra_cqfn164x4-2_lk_z_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.3	6	V
G002	V()	Voltage at DIN, CLK, SN, SP, SEL		-0.3	VDD + 0.3	V
G003	Vd()	ESD Susceptibility at DIN, CLK, SEL, DOUT, SN, SP	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G004	Tj	Junction Temperature		-40	150	°C
G005	Ts	Storage Temperature		-40	85	°C

THERMAL DATA

Operating Conditions: VDD = 5 V ±10%

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-25		75	°C
T02	Ts	Reflow Soldering Peak Temperature	tpk < 20 s, convection reflow MSL 4 according to J-STD 20 (max. floor life 72 h at 30 °C and 60% RH); please refer to Customer Information #7 for details			245	°C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 5 V ±10%, V(SN, SP) = 3.5 V...VDD, Tj = -25...85 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage Range		4.5		5.5	V
002	I(VDD)	Supply Current in VDD (Standby)	BP-amplifier and output stage disabled Tj = 27 °C		 40	60	µA µA
003	I(VDD)	Supply Current in VDD	BP-amplifier and output stage enabled Tj = 27 °C		 1.1	3.0	mA mA
004	VDDon	Turn-on Threshold VDD (Power-on Release)				4.2	V
005	VDDoff	Undervoltage Threshold VDD (Power-down Reset)	Decreasing voltage VDD	2.5			V
006	VDDhys	Hysteresis	VDDhys = VDDon − VDDoff	180		400	mV
007	Vc()hi	Clamp Voltage hi at DIN, CLK, SEL, DOUT, SN, SP	Vc()hi = V() − VDD, I() = 1 mA	0.4		1.25	V
008	Vc()lo	Clamp Voltage lo at DIN, CLK, SEL, DOUT, SN, SP		-1.25		-0.4	V
Photodiode							
101	Aph	Radiant Sensitive Area	⌀ 1.5 mm		1.767		mm^2
102	λ_{ar}	Spectral Application Range	$S(\lambda_{ar})$ = 0.25 × $S(\lambda)max$ (see Fig. 1)	400		950	nm
Bandpass Amplifier							
201	E()ccw	Permissible DC Irradiance	λ_{LED} für S(λ)max			675*	µW/cm²
202	twhi	Permissible Photocurrent Pulse Duration	SEL = lo (see Fig. 4) SEL = hi (see Fig. 5)	0.35 1.0			µs µs
203	twlo	Permissible Photocurrent Pause Duration	SEL = lo (see Fig. 4) SEL = hi (see Fig. 5)	0.4 2.0			µs µs
204	trec	Recovery Time	Φ(PD)pk = 5 mW; SEL = lo SEL = hi			 0.5* 10*	 µs µs
205	trec	Power Flash Recovery Time	Φ(PD)pk = 14 mW, radiant energy corresponds to 42 mWs; SEL = lo SEL = hi			 5* 30*	 µs µs
206	fl	Lower Cut-off Frequency (-3dB)	SEL = lo SEL = hi	90 30	290 80	390 110	kHz kHz
207	fh	Upper Cut-off Frequency (-3dB)	SEL = lo SEL = hi	600 100	1200 350	1800 650	kHz kHz
208	Δf	Bandwidth (-3dB)	SEL = lo SEL = hi	400 150	900 300	1400 500	kHz kHz
209	E()pk	Permissible Pulse Irradiance	I(OUT) increases or remains constant as E()pk increases			290*	mW/cm²
210	η_{pk}	Pulse Light Amplification	VDD = 5 V, P(PD)pk = 10 µW, λ_{pk} = 700 nm, tr = tf = 0.4 us, twpk = 1.5 µs; SEL = lo SEL = hi		 125 400		 A/W A/W
Output SN, SP							
301	V()out	Permissible Voltage at SN, SP		3.5		VDD	V
302	ISUM	Output Currents I(SN) + I(SP)	SEL = 0 SEL = 1	7.0 4.9	10.0 7.5	13.5 9.7	mA mA
303	IO	Relative Offset Current	IO = (I(SN) − I(SP)) / ISUM	-10		10	%
304	Ilk	Leakage Current I(SN) + I(SP)	Output disabled			4.0	µA
305	Idlk()	Differential Leakage Current	Idlk() = I(SN) − I(SP), twhi = 3 µs, output disabled	-0.1		0.1	µA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 5 V ±10%, V(SN, SP) = 3.5 V...VDD, Tj = -25...85 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
306	Ipn()	Differential Output Current	Ipn() = I(SN) − I(SP), E(PD)pk = 220 µW/cm²; SEL = 0 SEL = 1		 -0.5 -1.0		 mA mA
307	Ipn()	Differential Output Current	Ipn() = I(SN) − I(SP), E(PD)pk = 2.2 mW/cm²; SEL = 0 SEL = 1		 -4.0* -8.0*		 mA mA
308	INoise	Differential Output Current			5.0		µA
309	tp()IDCon	Output Stage Turn-on Delay: CLK hi → lo to 90% I(SN), I(SP)	SEL = lo: CLK hi → lo to 90% I(SN), I(SP) (see Fig. 4) SEL = hi: CLK lo → hi to 90% I(SN), I(SP) (see Fig. 5)			3.0 3.0	µs µs
310	tp()IDCoff	Output Stage Turn-off Delay: CLK lo → hi to 10% I(SN), I(SP)	SEL = lo: CLK lo → hi to 10% I(SN), I(SP) (see Fig. 4) SEL = hi: CLK lo → hi to 10% I(SN), I(SP) (see Fig. 5)			3.0 3.0	µs µs
Control Inputs DIN, CLK							
401	Vt()hi	Threshold Voltage hi	VDD = 5 V			2.0	V
402	Vt()lo	Threshold Voltage lo	VDD = 5 V	0.8			V
403	Vhys()	Input Hysteresis		450		700	mV
404	Ipd()	Pull-Down Current			30		µA
Output Buffer DOUT							
501	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(DOUT); I() = -4 mA			0.4	V
502	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	V
503	Isc()hi	Short-circuit Current hi	V() = 0 V	-100		-25	mA
504	Isc()lo	Short-circuit Current lo	V() = VDD	25		100	mA
Switching Characteristics							
601	tplh(CLK-DOUT)	Propagation Delay: CLK hi → lo until DOUT lo → hi	CL(DOUT) = 50 pF (see Fig. 3)			60	ns
602	tphl(CLK-DOUT)	Propagation Delay: CLK hi → lo until DOUT hi → lo	CL(DOUT) = 50 pF (see Fig. 3)			60	ns

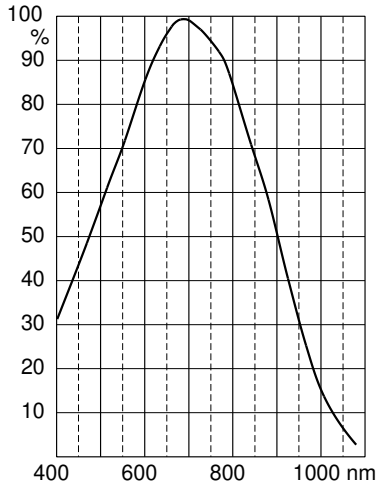


Figure 1: Typical relative spectral sensitivity

* Projected values by sample characterization

OPERATING REQUIREMENTS: Shift Register

Operating Conditions: VDD = 5 V ±10%, Ta = -25...75 °C, CL() = 50 pF
Input levels lo = 0...0.8 V, hi = 2 V...VDD, see fig. 2 and 3 for reference levels and waveforms

Item No.	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I001	tset	Setup Time: DIN stable before CLK lo → hi		3	50		ns
I002	thold	Hold Time: DIN stable after CLK lo → hi		3	50		ns
I003	f0	Permissible Frequency at CLK	Duty cycle 50%			10	MHz

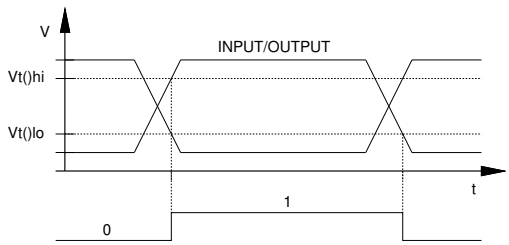


Figure 2: Reference levels

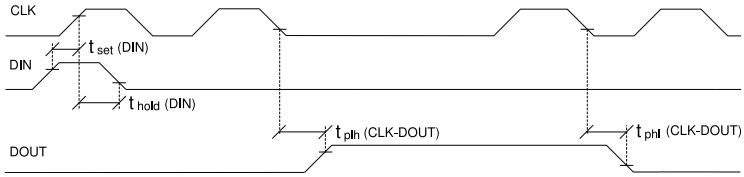


Figure 3: Timing characteristics

OPERATING REQUIREMENTS: SEL = lo

Operating Conditions: VDD = 5 V ±10%, Ta = -25...75 °C, CL() = 50 pF
Input levels lo = 0...0.8 V, hi = 2 V...VDD, see fig. 4 for reference levels and waveforms

Item No.	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I101	ten	Activation Time: CLK lo → hi to CLK hi → lo		4	2		µs
I102	tinh	Output Activation Time: CLK hi → lo until output ready to report		4	5		µs

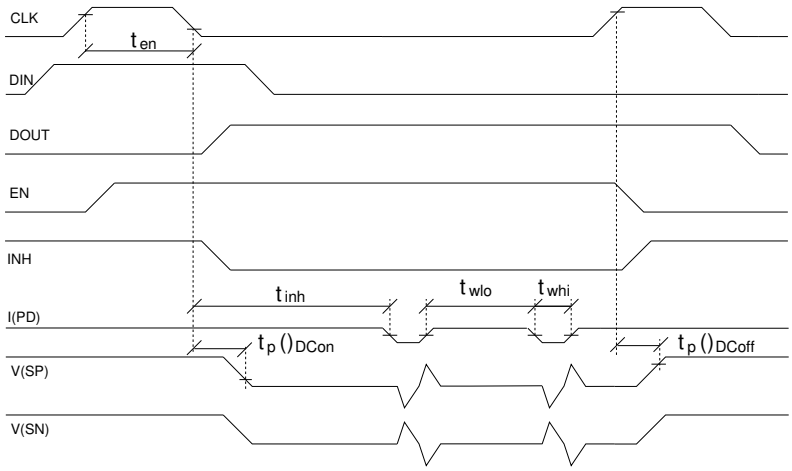


Figure 4: Timing characteristics (analogue section), outputs SN and SP with pull-up resistors to VDD

OPERATING REQUIREMENTS: SEL = hi

Operating Conditions: VDD = 5 V ±10%, Ta = -25...75 °C, CL() = 50 pF
Input levels lo = 0...0.8 V, hi = 2 V...VDD, see fig. 5 for reference levels and waveforms

Item No.	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I201	ten	Activation Time: DIN lo → hi to CLK lo → hi		5	10		µs
I202	tinh	Output Activation Time: CLK hi → lo until output ready to report		5	5		µs

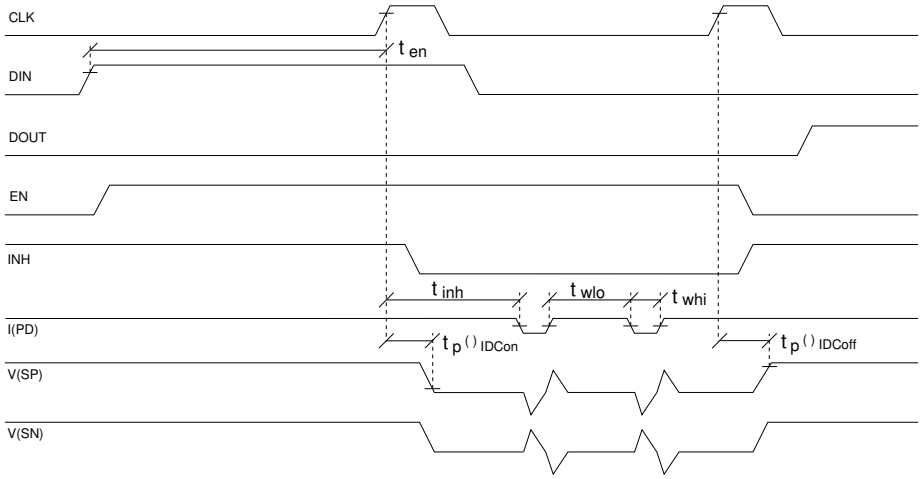


Figure 5: Timing characteristics (analogue section), outputs SN and SP with pull-up resistors to VDD

APPLICATIONS INFORMATION

Light curtains

The circuit in Figure 6 shows several iC-LKs connected as a light curtain, where consecutive ICs receive and evaluate clock-driven light pulses.

When discussing the function of iC-LK, it is assumed that all flip-flops have been reset, such as is the case, for example, after the supply voltage has been switched on. Signal DIN1 = high activates iC1's band-pass amplifier with the first rising edge of CLK. The current output stage of iC1 is activated when the second flip-flop also accepts the high signal with the falling CLK edge. Until this point, outputs SN and SP remain at high impedance.

With no AC fractions in the receiver photodiode, approximately equal currents are drawn in SN and SP. After a time of $t_{inh} \geq 5\,\mu s$, the transient differential currents in the current output stage caused when the device is switched on have decayed, and iC-LK is ready to receive.

With a light pulse being detected by IC1, the currents at outputs SP and SN react as shown in Figure 7; I(SP) rises and returns to its initial value within a time constant determined by the bottom cutoff frequency of the band-pass amplifier, as long as the photodiode is constantly illuminated. When the light pulse decays, the current in SP first sinks and then reaches its standby value within the same time constant. The current in SN has a mirror-image time dependence, meaning the sum of I(SN) + I(SP) is constant.

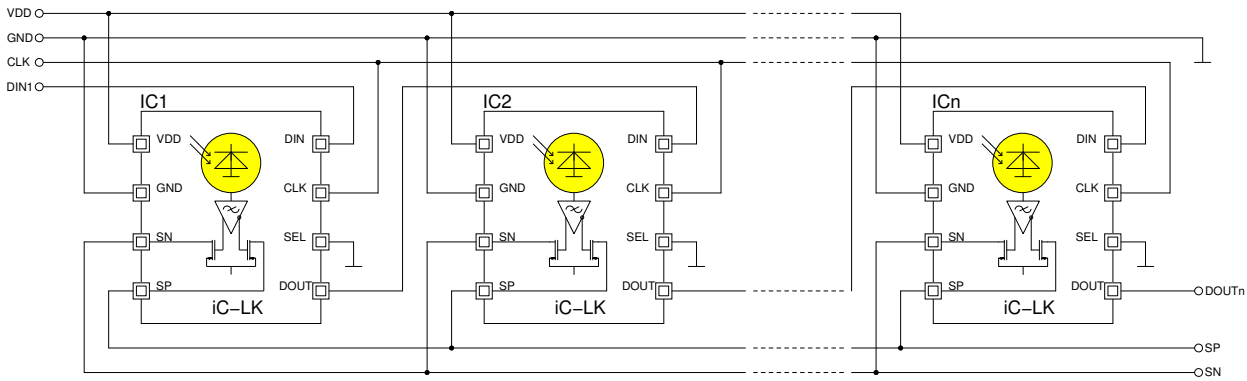


Figure 6: Schematic of a light curtain configuration

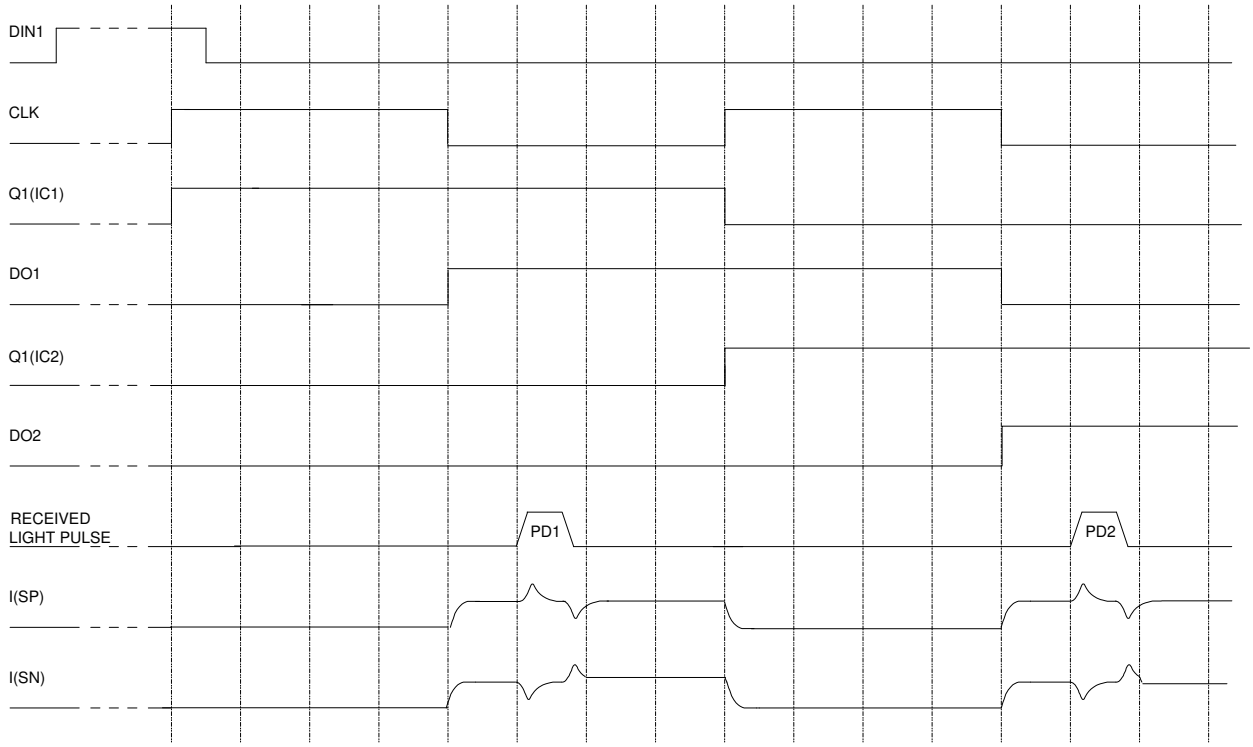


Figure 7: Signals for the chain configuration of Fig. 6

With DIN1 = 0, FF1 is reset at the next rising edge of CLK and the currents in the differential current output stage switched off. With the next falling edge, FF2 is reset. The pulse diagram is also valid for the subsequent components in the chain, i.e. the iCs configured as a light curtain make up a clock-driven shift register which passes on the input information.

Light curtain PCB layout

The PCB layout for light curtain receivers is not critical. As the power consumption is relatively small, only back-up capacitors with low capacitance values are required (typically 1 µF e-caps in parallel with 47...100 nF ceramic capacitors). The ceramic capacitors should be placed 7.5 cm apart and the e-caps at double this distance. The number of receivers blocked off as a group in this manner is irrelevant, as only one device is active and draws current at any one time.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2017-08-14	PACKAGES	Graphics updated	1
		BLOCK DIAGRAM	Graphics updated	1
		PACKAGING INFORMATION	Graphics updated	2
		PACKAGING INFORMATION	Function description of pin SEL complemented	2
		PACKAGING INFORMATION	Package dimensions graphics updated	3
		ABSOLUTE MAXIMUM RATINGS	G005: storage temperature corrected	4
		THERMAL DATA	T01: ambient temperature expanded	4
		ELECTRICAL CHARACTERISTICS	Operating conditions: junction temperature expanded	5-6
		ELECTRICAL CHARACTERISTICS	006: max. value corrected	5
		ELECTRICAL CHARACTERISTICS	102: spectral sensitivity dropped	5
		ELECTRICAL CHARACTERISTICS	207: upper cut-off frequency corrected	5
		ELECTRICAL CHARACTERISTICS	208: bandwidth corrected	5
		ELECTRICAL CHARACTERISTICS	210: pulse-light amplification conditions corrected	5
		ELECTRICAL CHARACTERISTICS	307: differential output current footnote added	6
		ELECTRICAL CHARACTERISTICS	401: threshold voltage hi min. value dropped, max. value corrected	6
		ELECTRICAL CHARACTERISTICS	402: threshold voltage low max. value dropped	6
		ELECTRICAL CHARACTERISTICS	3A01: added, selected profile only	6
		OPERATING REQUIREMENTS	Operating conditions: ambient temperature expanded	7-8

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-LK	clearQFN16 4 mm x 4 mm	iC-LK cQFN16-4x4

Please send your purchase orders to our order handling team:

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