iC-NL

LIGHT CHAIN PULSE DRIVER

FEATURES

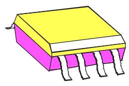
- Adjustable LED pulse operation, set range of 0.4..1.2A
- Short light pulses down to 300ns
- Preset of LED current through external resistor with low power requirement
- LED efficiency degradation compensated by positive current temperature coefficient
- Control logic with 2-step shift register
- Thermal shutdown and power-down reset
- Compatible to CMOS-levels
- Data output buffer optimized for open lines
- Single 5V supply
- Low standby current; circuit activation by input data
- ESD protection
- Small outline package SO8
- Suited for high-risk applications according to IEC 1496-1

◊ Option: extended temperature range of -20°C to 85°C

APPLICATIONS

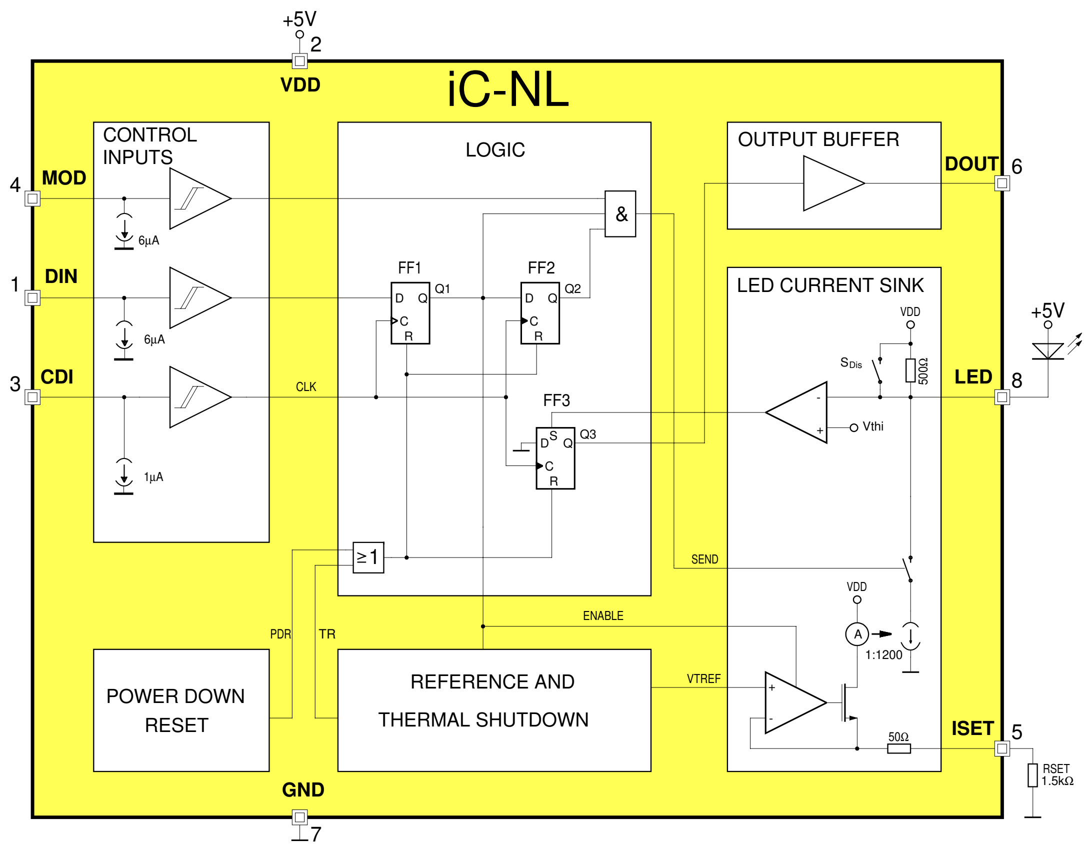
- Light curtain LED driver
- Light barrier LED driver
- Electro-sensitive protective equipment (ESPE)

PACKAGES



SO8

BLOCK DIAGRAM



Rev A0

iC-Haus GmbH
Integrated Circuits
Am Kuemmerling 18, D-55294 Bodenheim

Tel. +49/6135-9292-0
Fax +49/6135-9292-192
http://www.ichaus.com

DESCRIPTION

iC-NL is an LED pulse driver for light curtain systems and light barriers.

The device, which is controlled by a shift register, features an adjustable LED current sink with a set range of 0.4 to 1.2A (at room temperature). The two stages of the shift register cell enable data to be safely transported, free of race conditions, in order to activate pulse driver iC-NL connected in a chain with light curtain applications. The standby current draws a maximum of 60µA from 5V.

The positive temperature coefficient of the LED current sink largely compensates for the decrease in LED efficiency with a rise in temperature. Active discharge through short-circuiting the junction capacitance of the LED enables steep light pulses to be generated. The duration of this short circuit is determined by a monoflop which closes switch S_{DIS}. In the event of light pulses occurring in rapid succession, the monoflop is automatically reset to prevent cross currents.

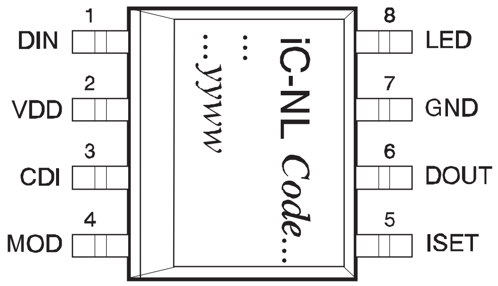
The driver stage of the LED current sink prepares for a light pulse with the rising edge of CDI when DIN reads a high signal (ENABLE= hi). With the consecutive falling edge, the high signal is passed on to output Q2 of the second flip-flop. The LED current sink can now be activated by a high at input MOD and deactivated by a low. Short current pulses with a width of 300ns or more or pulse sequences of 1.5MHz are possible. The voltage drop at the LED during a light pulse causes levels to drop below threshold voltage Vthi at pin LED. This results in a high level at the comparator output and at data output DOUT. An LED short circuit thus prevents an output via data output DOUT.
If DIN now reads a low, the driver stage is powered down with the next rising CLK edge; with the following falling edge, output DOUT also switches to low.

The flip-flops are reset and the LED current sink is turned off in the event of excessive temperature or low voltage. The device has protective diodes which prevent destruction by ESD. Driver and logic outputs are current-limited and short-circuit-proof, as the device is shut down with excessive temperature.

iC-NL fulfils safety requirements according to IEC 1496-1. An extended temperature range of -20°C..85°C is also available as an option.

PACKAGE SO8 to JEDEC Standard

PIN CONFIGURATION SO8
(top view)



PIN FUNCTIONS

No.	Name	Function
1	DIN	Data Input
2	VDD	+5V Supply Voltage
3	CDI	Clock Input
4	MOD	Modulation Input
5	ISET	Current Adjust, attachement RSET
6	DOUT	Data Output
7	GND	Ground
8	LED	Pulse Output, LED Cathode

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
G001	VDD	Supply Voltage			-0.5	7	V
G002	V()	Voltage at Inputs DIN, MOD			-0.5	VDD+0.5	V
G003	V()	Voltage at CDI, DOUT, ISET, LED			-0.5	VDD+0.5	V
E001	Vd()	ESD Susceptibility at VDD, ISET and digital Inputs/Outputs	MIL-STD-883, HBM 100pF discharged through 1.5kΩ			2	kV
E002	Vd(LED)	ESD Susceptibility at LED	with standard circuitry, HBM 100pF discharged through 1.5kΩ	5		2	kV
TG1	Tj	Junction Temperature			-40	150	°C
TG2	Ts	Storage Temperature			-40	150	°C

THERMAL DATA

Operating Conditions: VDD= 4.75..5.5V

Item	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
T1	Ta	Operating Ambient Temperature Range (extended temperature range of -20..85°C on request)			0		70	°C
T2	Rthja	Thermal Resistance Junction to Ambient	surface mounted without special cooling areas				170	K/W

All voltages are referenced to ground unless otherwise noted.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions:
VDD= 4.75..5.5V, RSET= 1.5kΩ, Tj= -20..85°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VDD	Permissible Supply Voltage Range				4.75		5.5	V
002	Toff	Shutdown Temperature				110		150	°C
003	I(VDD)	Supply Current in VDD	LED current sink off (flipflops reset); DIN, MOD, CDI= hi or lo, logic levels: lo= 0V..0.45V, hi= VDD-0.45V..VDD					60	µA
004	I(VDD)	Supply Current in VDD	LED current sink off (flipflops reset); DIN, MOD, CDI= hi or lo logic levels: lo= 22%VDD, hi= 78%VDD					1.0	mA
005	I(VDD)	Supply Current in VDD	analog section enabled, RSET≥ 1.5kΩ; internal signal SEND= lo	-20 27 85 125				7.5 7.5 8.5 1.0	mA mA mA mA
006	I(VDD)	Supply Current in VDD	analog section enabled, RSET≥ 1.5kΩ; internal signal SEND= hi	 125				25 1.0	mA mA
007	VDDon	Turn-on Threshold VDD (Power-on Release)						4.3	V
008	VDDoff	Undervoltage Threshold at VDD (Power-down Reset)	decreasing voltage VDD			2.7			V
009	VDDhys	Hysteresis	VDDhys= VDDon-VDDoff			100			mV
010	Vc()hi	Clamp Voltage hi at DIN, CDI, MOD, DOUT, ISET, LED	Vc()hi= V()-VDD, I()= 10mA			0.4		1.25	V
011	Vc()lo	Clamp Voltage lo at DIN, CDI, MOD, DOUT, ISET, LED	I()= -10mA, VDD= 0V other pins open			-1.25		-0.4	V
LED Current Sink LED, ISET									
101	V(ISET)	Reference Voltage at ISET	RSET= 1.5..4.5kΩ	-20 27 85 125			1.27 1.50 1.79 0		V V V V
102	TC(ISET)	Temperature Coefficient of Reference Voltage at ISET	RSET= 1.5..4.5kΩ	27		0.30	0.33	0.36	%/K
103	CR1	Current Ratio I(LED) / -I(ISET)	RSET= 1.5..4.5kΩ, V(LED)= 1.0V..VDD				1200		
104	I(LED)	LED Pulse Current	duty cycle I(LED)≤ 1%, RSET= 1.5kΩ, V(LED)= 1.0V..VDD	-20 27 85 125		0.78 0.98 1.11	1.02 1.20 1.44 0	1.27 1.42 1.78	A A A A
105	I(LED)	LED Pulse current	duty cycle I(LED)≤ 1%, RSET= 4.5kΩ, V(LED)= 0.85V..VDD	-20 27 85 125		0.26 0.33 0.37	0.34 0.40 0.48 0	0.44 0.48 0.61	A A A A
106	tr(LED)	LED Current Rise Time			3			150	ns
107	tf(LED)	LED Current Fall Time			3			150	ns
108	tdis(LED)	LED Discharge Duration	LED shutdown, switch Sdis closed					400	ns

ELECTRICAL CHARACTERISTICS

Operating Conditions:
VDD= 4.75..5.5V, RSET= 1.5kΩ, Tj= -20..85°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
LED Current Sink (continued)									
109	Ir(LED)	LED Discharge Current	V(VDD/LED)= 1.5V				200		mA
110	Rpu(LED	Pull-up Resistor at LED				300	500	850	Ω
111	Vt(LED)hi	LED Short-circuit Check	Vt(LED)hi= VDD -V(LED)			0.5		1	V
Control Inputs DIN, CDI, MOD									
201	Vt()hi	Threshold Voltage hi						78	%VDD
202	Vt()lo	Threshold Voltage lo				22			%VDD
203	Vhys()	Schmitt-Trigger Input Hysteresis				400			mV
204	Ipd()	Pull-Down Current in DIN, MOD	V()= 5.0V			3	6	12	µA
205	Ipd(CDI)	Pull-Down Current in CDI	V(CDI)= 5V, internal signal Q1= lo			0.4	1	2	µA
Output Buffer DOUT									
301	Vs()hi	Saturation Voltage hi	Vs()hi= VDD -V(DOUT), I(DOUT)= -4mA					0.4	V
302	Vs()lo	Saturation Voltage lo	I(DOUT)= 4mA					0.4	V
303	Isc()hi	Short-Circuit Current hi	V(DOUT)= 0V			-80	-40	-20	mA
304	Isc()lo	Short-Circuit Current lo	V(DOUT)= VDD			20	40	80	mA
305	Rout()	Source Resistance	VDD= 5V, V(DOUT)= 2.5V			80	120	190	Ω
306	tr()	Rise Time	CL(DOUT)≤ 50pF				20	60	ns
307	tf()	Fall Time	CL(DOUT)≤ 50pF				20	60	ns
Switching Characteristics									
401	tphl(MOD -LED)	LED Pulse Turn-on Delay	MOD lo→hi until I(LED)= 10% set value		4			100	ns
402	tplh(MOD -LED)	LED Pulse Turn-off Delay	MOD hi→lo until I(LED)= 90% set value		4			80	ns
403	tplh (MOD-DOUT)	Delay Time: MOD lo→hi until DOUT lo→hi	CL(DOUT)≤ 50pF, Q1, Q2= hi		2		60	120	ns
404	tphl (CDI-DOUT)	Delay Time: CDI hi→lo until DOUT hi→lo	CL(DOUT)≤ 50pF		2		25	60	ns

OPERATING REQUIREMENTS: Logic

Operating Conditions: VDD= 4.75..5.5V, Ta= 0..70°C, CL()= 50pF,
input levels lo= 0..0.45V, hi= VDD-0.45V..VDD, see Fig. 1 for reference levels and waveforms

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I1	ten	LED-Current Source Activation Time: CDI lo→hi until MOD hi for LED on		4	5		µs
I2	tset	Setup time: DIN stable before CDI lo→hi		2	50		ns
I3	thold	Hold time: DIN stable after CDI lo→hi		2	50		ns

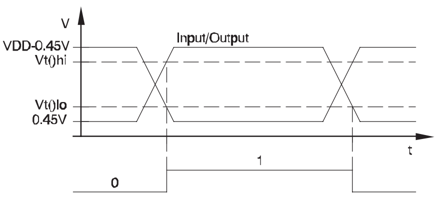


Fig. 1: reference levels

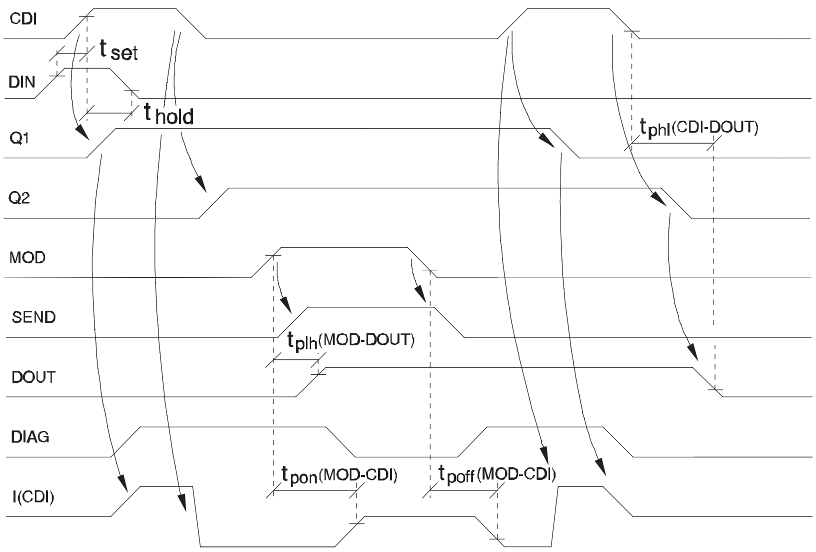


Fig. 2: timing characteristics

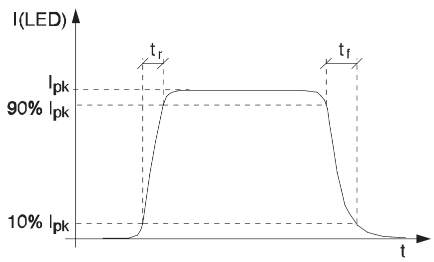


Fig. 3: LED current pulse

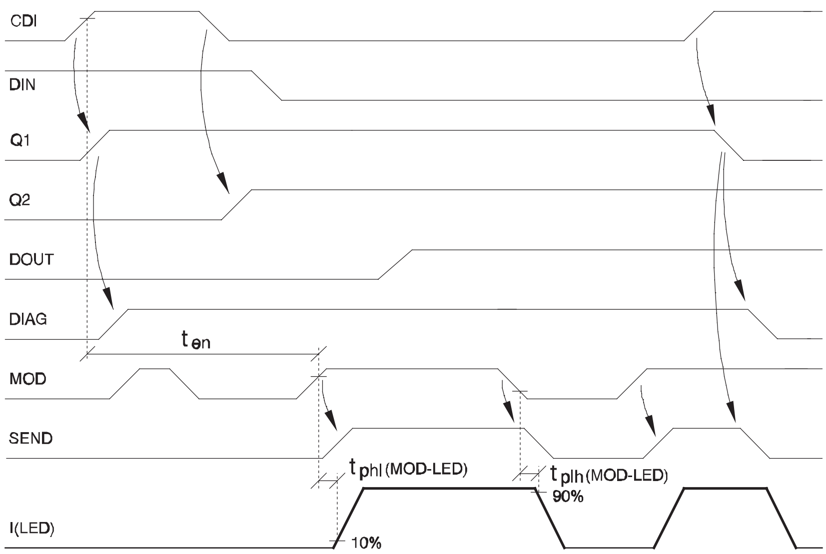


Fig. 4: chain configuration,
LED current pulse generated by MOD signal

APPLICATIONS INFORMATION

Light curtains
The circuit in Figure 5 shows several iC-NLs connected as a light curtain, where consecutive LEDs emit clock-driven light pulses.

When discussing the function of iC-NL, it is assumed that all flip-flops in iC1..iCn have been reset, such as is the case, for example, after the supply voltage has been switched on. Signal DIN= high activates iC1's current sink with the first rising edge of CLK; this current sink can be switched in following the falling CLK edge with MOD = high of LED1. When the driver current is reached, set with RSET, a high is sent to output DOUT by FF3.

With DIN1= low, the next rising CLK edge resets FF1 and deactivates the current sink in iC1. With the falling edge, output DOUT is again set to low. The pulse diagram in Figure 6 is also valid for the subsequent components in the chain, i.e. the iCs configured as a light curtain make up a clock-driven shift register which passes on the input information.

The length of a light pulse can be stipulated with the aid of modulation input MOD. In general, the pulse duration is determined by the activation time required by the receiver or by requirements set by the system.

As the LED pulse currents are high, the PCB layout must be designed so as to avoid large voltage drops on the supply lines. The high, short-term pulse current is provided by back-up capacitors C1..Cn; these should have a low inductance due to the high increase rate of the current. The leads to the LED anode and to iC-NL's GND pin should be as short as possible. The capacitors selected should ensure that the voltage drop caused by a light pulse is less than 1V, i.e. that C1..Cn= 1µF for a light pulse of 1A x 1µs, for example. In practice, the voltage at the iC drops much less during a pulse, as charge from the back-up capacitors of neighboring iCs also flows into the active device. Low-inductance capacitance can be achieved most economically by placing several capacitors of low capacitance in parallel.

Since only one device is activated at any one time within a section of the light curtain, several iC-NLs can share external resistor RSET to set the coil current. This parallel circuit should be limited to ca. 5 iCs due to the increasing capacitive load at pin ISET.

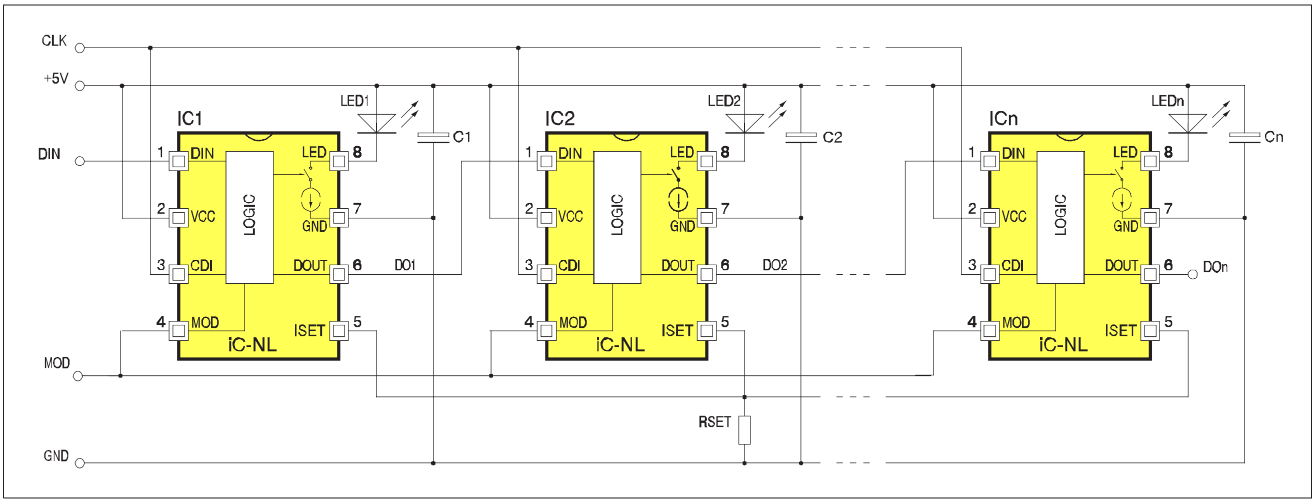


Fig. 5: schematic of a chain configuration

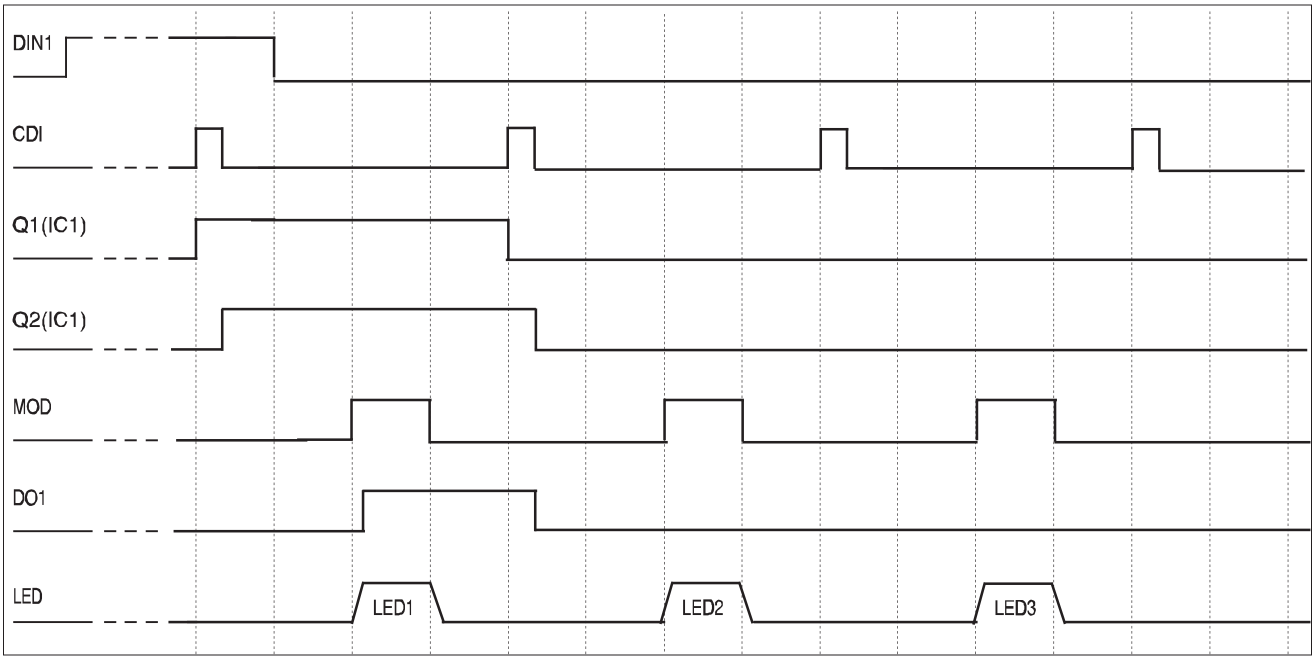


Fig. 6: signals of the chain configuration of figure 5

ORDERING INFORMATION

Type	Package	Order designation
iC-NL	SO8	iC-NL SO8

For information about prices, terms of delivery, options for other case types, etc., please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim

Tel. +49-6135-9292-0
Fax +49-6135-9292-192
www.ichaus.com