iC-MCB EVAL MCB1D
EVALUATION BOARD DESCRIPTION

FUNCTIONAL MODEL; EVAL-BOARD:
This device is for laboratory use only. Due to limited testing and lack of qualification for use under all conditions, long-term performance is not guaranteed. Malfunctions and operating errors may damage the device and the connected circuit; such damage may result in personal injury to the user. Safety goggles are mandatory. All liability and option of return are terminated upon activation of the device.

ORDERING INFORMATION

The evaluation kit includes the evaluation board of iC-MCB. For BiSS/SSI communication with iC-MCB, iC-Haus recommends the BiSS/SSI to PC-USB MBxU-Adapter family. Please refer to the following table for further information.

Type	Order Designation	Description
Evaluation board	iC-MCB EVAL MCB1D	iC-MCB evaluation board Ready-to-operate, accessible by GUI using PC adapter (not included)
Related parts	(to be sold separately)	
PC adapter	iC-MB3 iCSY MB3U-I2C	PC-USB Adapter for BiSS/SSI w. I2C/SPI extension cable
	iC-MB5 iCSY MB5U	High Perf. Galv. Isolated BiSS(SSI)-to-PC USB Adapter For further information check DOCUMENTATION AND SOFTWARE

BOARD MCB1D

(size 100 mm x 80 mm)

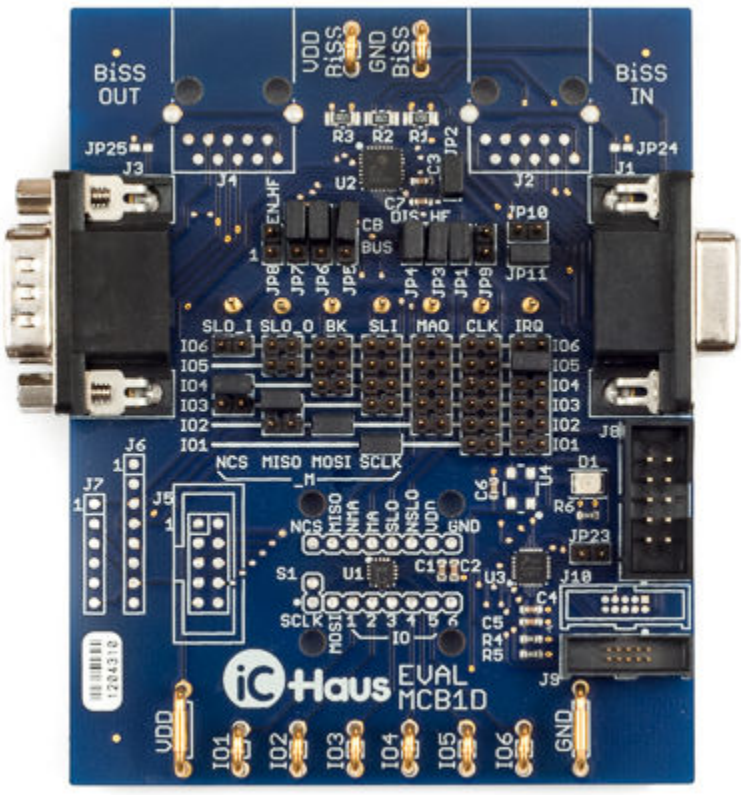

Figure 1: Evaluation board MCB1D

DOCUMENTATION AND SOFTWARE

- IC Documentation → www.ichaus.de/MCB

- IC Software GUI (BiSS device configuration via BiSS adapter)
  - with LabVIEW™ RTE → www.ichaus.de/MCB_gui_rte
  - without LabVIEW™ RTE → www.ichaus.de/MCB_gui

- BiSS-to-PC Adapter Descriptions
  - MB3U-I2C → www.ichaus.de/MB3U_datasheet_en
  - MB5U → www.ichaus.de/MB5U_datasheet_en

- BiSS Protocol Description → www.biss-interface.com/biss_c_en

- BiSS Safety Concept → www.biss-interface.com/biss_safety_concept_en

CONNECTORS AND TERMINALS

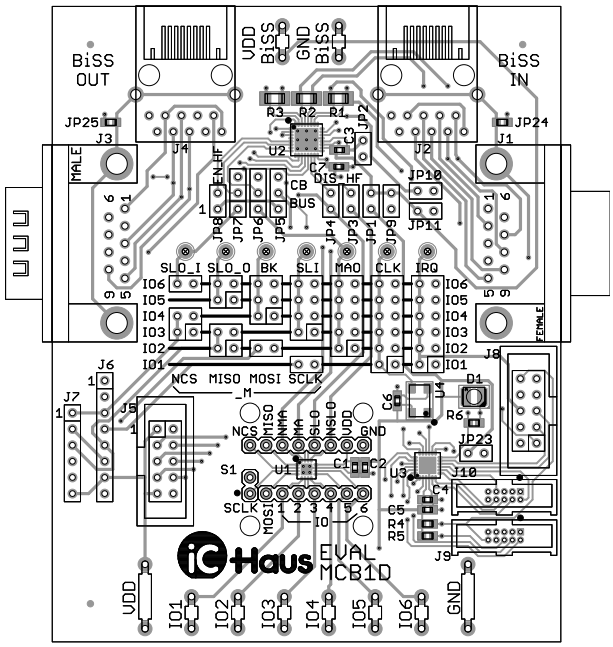

Figure 2: Component side

TERMINALS

Upper side (from left to right)

VDD BiSS	+5 V Supply Voltage for iC-HF
GND BiSS	Ground

Center area (from left to right)

SLO_I	BiSS Data Input to internal SLO_I
SLO_O	BiSS Data Output from internal SLO_O
BK	BiSS Bus Coupler Control Signal
SLI	BiSS Data Input
MAO	BiSS Clock Internal Output
CLK	Oscillator Clock Input
IRQ	Interrupt Request Output for MCU

Availability of the aforementioned signals depends on jumper settings and iC-MCB's I/O crossbar configuration.

Lower side (from left to right)

VDD	3.0 V . . . +5 V Supply Voltage for iC-MCB
IO1	I/O Crossbar Port 1 (iC-MCB)
IO2	I/O Crossbar Port 2 (iC-MCB)
IO3	I/O Crossbar Port 3 (iC-MCB)
IO4	I/O Crossbar Port 4 (iC-MCB)
IO5	I/O Crossbar Port 5 (iC-MCB)
IO6	I/O Crossbar Port 6 (iC-MCB)
GND	Ground

LEDS

LED D1	Power LED (green)

CONNECTORS

J1	BiSS Interface to master (to PC adapter) (9-pin D-Sub, female)
J2	BiSS Interface to master (RJ45) (not assembled)
J3	BiSS Interface to slaves (optional) (9-pin D-Sub, male)
J4	BiSS Interface to slaves (RJ45, optional) (not assembled)
J5	I/O Crossbar Interface (10-pin, iC-MCB) (not assembled)
J6	Fast Sensor Interface: SPI Master (8-pin) (not assembled, suitable to connect sensors with serial interface)
J7	Fast Sensor Interface: SPI Master (6-pin) (not assembled, suitable to connect sensors with serial interface)
J8	Host Interface: SPI Slave (suitable to connect offboard MCU)
J9	Programming Interface for onboard MCU
J10	MCU I/O Interface (not assembled)

PINOUT OF CONNECTORS

BiSS Interface to master (to PC adapter)
9-pin D-Sub connector J1 - female

PIN	Name	Function
1	VB_IN	+12 V Supply Voltage (line in)
2	MA +	Master Clock Input
3	MA -	Master Clock Input (inverted)
4	VDD_IN	+5 V Supply Voltage (line in)
5	SLI -	Slave Data Input (inverted)
6	GND_BiSS	0 V Ground (line in)
7	SL +	Slave Data
8	SL -	Slave Data (inverted)
9	SLI +	Slave Data Input

BiSS Interface to slaves (RJ45, optional)
10-pin RJ45-Sub connector J4 - female

PIN	Name	Function
1	SL +	Slave Data
2	SL -	Slave Data (inverted)
3	MAO +	Master Clock Output
4	SLO +	Slave Data Output
5	SLO -	Slave Data Output (inverted)
6	MAO -	Master Clock Output (inverted)
7	VB_OUT	+12 V Supply Voltage
8	GND_BiSS	0 V Ground
A	VDD_OUT	+5 V Supply Voltage
B	GND_BiSS	0 V Ground
SHLD	SHIELD_OUT	Shield_Out

BiSS Interface to master (RJ45)
10-pin RJ45 connector J2 - female

PIN	Name	Function
1	SL +	Slave Data
2	SL -	Slave Data (inverted)
3	MA +	Master Clock Input
4	SLI +	Slave Data Input
5	SLI -	Slave Data Input (inverted)
6	MA -	Master Clock Input (inverted)
7	VB_IN	+12 V Supply Voltage (line in)
8	GND_BiSS	0 V Ground (line in)
B	GND_BiSS	0 V Ground (line in)
A	VDD_IN	+5 V Supply Voltage (line in)
SHLD	SHIELD_IN	Shield_In

I/O Crossbar Interface (10-pin, iC-MCB)
10-pin connector J5

PIN	Name	Function
1	VDD	Supply Voltage (3.0 V . . . 5.5 V)
2	GND	Ground
3	IO1	Digital Port Input/Output
4	IO2	Digital Port Input/Output
5	IO3	Digital Port Input/Output
6	IO4	Digital Port Input/Output
7	IO5	Digital Port Input/Output
8	IO6	Digital Port Input/Output
9	VDD	Supply Voltage (3.0 . . . 5.5 V)
10	GND	Ground

BiSS Interface to slaves (optional)
9-pin D-Sub connector J3 - male

PIN	Name	Function
1	VB_OUT	+12 V Supply Voltage
2	MAO +	Master Clock Output
3	MAO -	Master Clock Output (inverted)
4	VDD_OUT	+5 V Supply Voltage
5	SLO -	Slave Data Output (inverted)
6	GND_BiSS	0 V Ground
7	SL +	Slave Data
8	SL -	Slave Data (inverted)
9	SLO +	Slave Data Output

Sensor Interface
8-pin connector J6

PIN	Name	Function
1	n.c.	
2	n.c.	
3	NCS_M	SPI Chip Select Output (low active, I/O Crossbar)
4	SCLK_M	SPI Clock Output (I/O Crossbar)
5	MISO_M	SPI MISO Input (I/O Crossbar)
6	MOSI_M	SPI MOSI Output (I/O Crossbar)
7	VDD	Supply Voltage (3.0 V . . . 5.5 V)
8	GND	Ground

Sensor Interface
6-pin connector J7

PIN	Name	Function
1	NCS_M	SPI Chip Select Output (low active, I/O Crossbar)
2	MOSI_M	SPI MOSI Output (I/O Crossbar)
3	MISO_M	SPI MISO Input (I/O Crossbar)
4	SCLK_M	SPI Clock Output (I/O Crossbar)
5	GND	Ground
6	VDD	Supply Voltage (3.0 V . . . 5.5 V)

SPI Host Interface
10-pin connector J8

PIN	Name	Function
1	SCLK	SPI Clock Input (iC-MCB)
2	GND	Ground
3	PTC1	Analog/Digital Port (MCU)
4	VDD	Supply Voltage (3.0 V . . . 5.5 V)
5	PTC2	Analog/Digital Port (MCU)
6	IRQ	Interrupt Request Output (I/O Crossbar)
7	MOSI	SPI MOSI Input (iC-MCB)
8	NCS	SPI Chip Select Input (low active, iC-MCB)
9	MISO	SPI MISO Output (iC-MCB)
10	NRES	Disable MCU by pin 10 with 0V, open pin = enable MCU

DESCRIPTION OF JUMPERS

Default setting: FSI and IRQ at I/O Crossbar, powered via J1, single-board connection, iC-HF disabled

I/O Crossbar (iC-MCB)

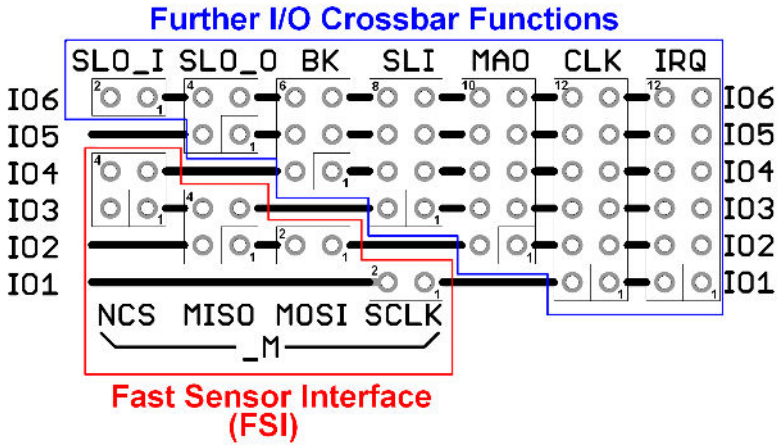

Figure 3: Jumper for I/O Crossbar Configuration

	SCLK_M JP15	MOSI_M JP14	MISO_M JP13	NCS_M JP12	Condition
IO1	1-2 bridged	N/A	N/A	N/A	CB_FSI = 1, 2, 3, 5, 6, 7
IO2	N/A	1-2 bridged	open	N/A	CB_FSI = 1, 2, 5, 6
IO2	N/A	open	1-2 bridged	N/A	CB_FSI = 3, 7
IO3	N/A	N/A	3-4 bridged	open	CB_FSI = 1, 5
IO3	N/A	N/A	open	1-2 bridged	CB_FSI = 6, 7
IO4	N/A	N/A	N/A	3-4 bridged	CB_FSI = 5

CLK	JP21	Condition: CB_CLK = 1
IO1	1-2 bridged	IO1 free
IO3	5-6 bridged	IO1 . . . 2 used, IO3 free
IO4	7-8 bridged	IO1 . . . 3 used, IO4 free
IO5	9-10 bridged	IO1 . . . 4 used, IO5 free
IO6	11-12 bridged	IO1 . . . 5 used, IO6 free

IRQ	JP22	Condition: CB_IRQ = 1
IO1	1-2 bridged	IO1 free
IO2	3-4 bridged	IO1 used, IO2 free
IO3	5-6 bridged	IO1 . . . 2 used, IO3 free
IO4	7-8 bridged	IO1 . . . 3 used, IO4 free
IO5	9-10 bridged	IO1 . . . 4 used, IO5 free

MAO	JP20	Condition: CB_MAO = 1
IO2	1-2 bridged	IO2 free
IO3	3-4 bridged	IO2 used, IO3 free
IO4	5-6 bridged	IO2 . . . 3 used, IO4 free
IO5	7-8 bridged	IO2 . . . 4 used, IO5 free
IO6	9-10 bridged	IO2 . . . 5 used, IO6 free

SLI	JP19	Condition: CB_SLI = 1
IO3	1-2 bridged	IO3 free
IO4	3-4 bridged	IO3 used, IO4 free
IO5	5-6 bridged	IO3 . . . 4 used, IO5 free
IO6	7-8 bridged	IO3 . . . 5 used, IO6 free

BK	JP18	Condition: ENCMD2 = 1
IO4	1-2 bridged	IO4 free
IO5	3-4 bridged	IO4 used, IO5 free
IO6	5-6 bridged	IO4 . . . 5 used, IO6 free

SLO_O	JP17	Condition: CB_SLO = 1
IO5	1-2 bridged	IO5 free
IO6	3-4 bridged	IO5 used, IO6 free

SLO_I	JP16	Condition: CB_SLO = 1
IO6	1-2 bridged	IO6 free

Besides jumper settings the following iC-MCB parameters have to be considered: CB_FSI, CB_IRQ, CB_CLK, CB_MAO, CB_SLI, CB_BK, CB_SLO.

Voltage Supply

Power Supply	JP1 / JP2	JP11	JP23	Comment
via board terminals	bridged	open	open	VDD and VDD_BiSS connected
via J1 (BiSS Master)				
- Bypassed iC-HF	bridged	bridged	open	VDD and VDD_BiSS connected
- Through iC-HF	open	bridged	open	With reverse polarity protection
via J8 (SPI-HOST)	bridged	open	bridged	VDD and VDD_BiSS connected

Line driver

Line Driver	JP3 / JP4	JP8	Comment
iC-HF used	open	bridged	
iC-MCB used	bridged	open	No communication chain via J3, iC-HF disabled

Communication chain

Communication chain	Board 1 . . . n-1 JP5	Board n (leftmost) JP5	Comment
Single-Board connection	2-3 bridged	N/A	
Board-to-Board connection			
- Manually	1-2 bridged	2-3 bridged	
- Programmable via BiSS	open	open	uses BK (I/O Crossbar)

Source for MAO (J3, J4)	JP6
iC-HF	2-3 bridged
iC-MCB (MAO, I/O Crossbar)	1-2 bridged

Source for SLO (J1 . . . J4)	JP7
iC-MCB (SLO)	2-3 bridged
iC-MCB (SLO_I, I/O Crossbar)	1-2 bridged

VDD_OUT (J3)	JP9
Connected to VDD_BiSS	bridged
VDD_OUT left open	open

VB_OUT (J3, J4)	JP10
Connected to VB_IN	bridged
VB_OUT left open	open

SHIELD_IN (J1, J2)	JP24
Connected to GND_BiSS	bridged
SHIELD_IN left open	open

SHIELD_OUT (J3, J4)	JP25
Connected to GND_BiSS	bridged
SHIELD_OUT left open	open

Note:
JP24 and JP25 are not assembled upon delivery.

CIRCUIT SCHEMATIC

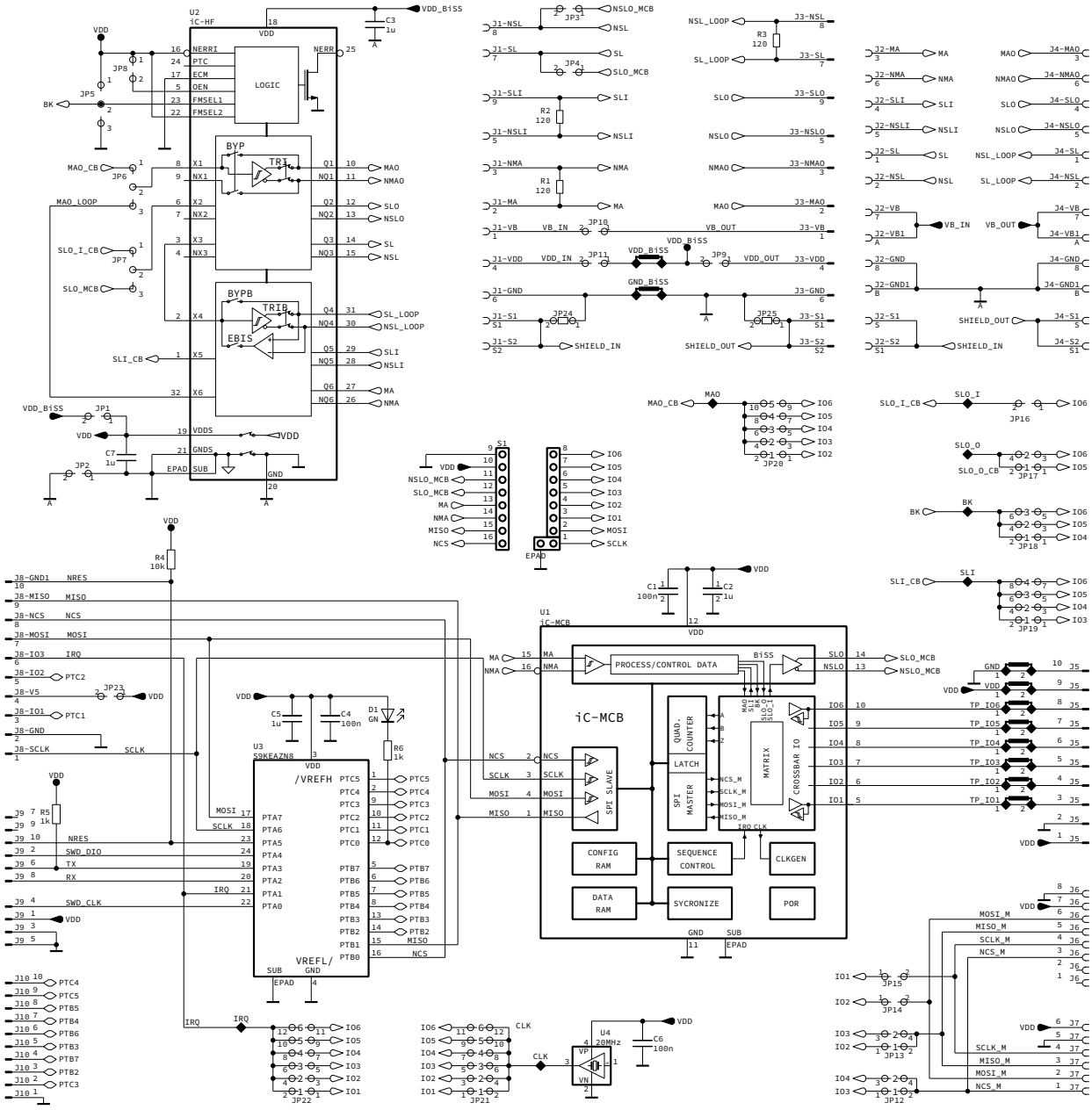

Figure 4: Circuit schematic

BOARD LAYOUT

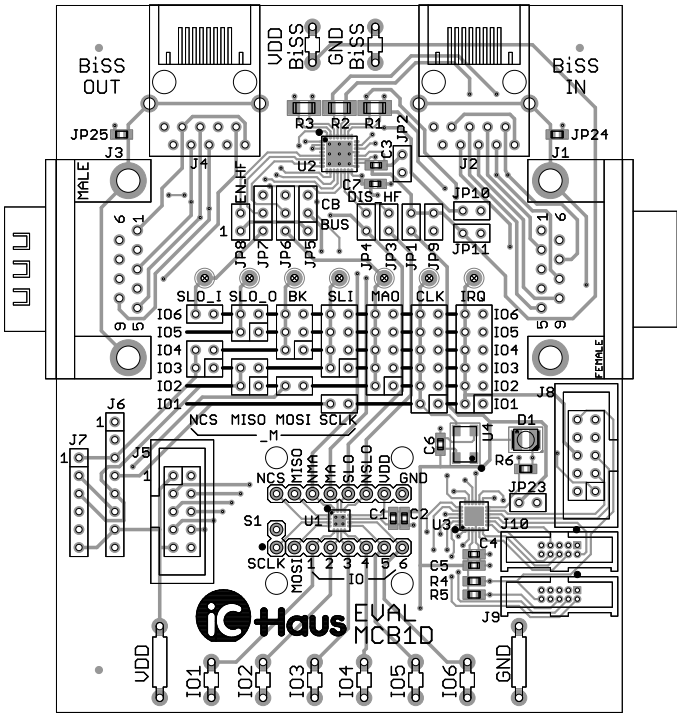

Figure 5: iC-MCB EVAL MCB1D (top side)

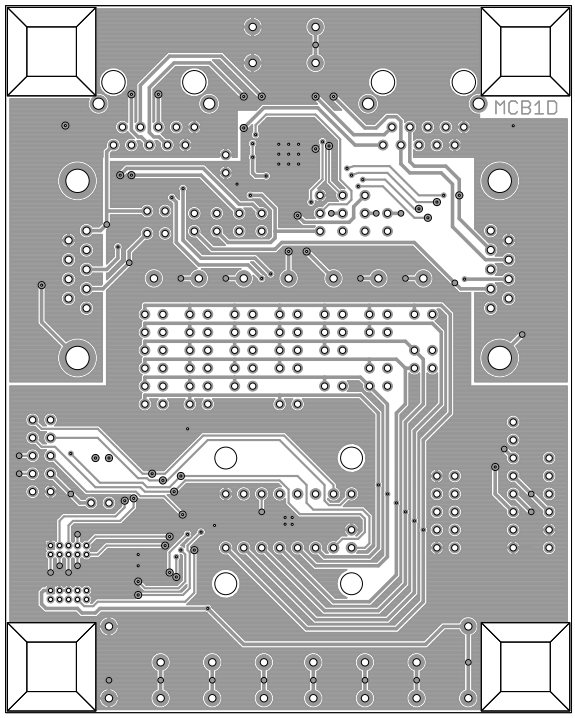

Figure 6: iC-MCB EVAL MCB1D (bottom side)

ASSEMBLY PART LIST

Device	Value (typical)	Comment
D1	LED green	Power LED
J1	D-SUB9 FEMALE	
J2, J4	RJ45 10	Y-CONJACK-21 (not assembled)
J3	D-SUB9 MALE	
J5	WSL10	not assembled
J6	W8X1	not assembled
J7	W6X1	not assembled
J8	WSL10	
J9	ESHF-105-01-L-D-TH	not assembled
J10	ESHF-105-01-L-D-TH	not assembled
BK, CLK, IRQ, MAO, SLI, SLO_I, SLO_O	S1-F	Test pins
GND, VDD	LBS04	Test clamp 40
GND_BISS, VDD_BISS, TP_IO1-6	LBS02	Test clamp 20
JP1, JP2, JP3, JP4, JP8, JP9, JP10, JP11, JP14, JP15, JP16, JP23	W2X1	Jumper
JP5, JP6, JP7	W3X1	Jumper
JP12, JP13, JP17	W2X2	Jumper
JP18	W3X2	Jumper
JP19	W4X2	Jumper
JP20	W5X2	Jumper
JP21, JP22	W6X2	Jumper
JP24, JP25	0 Ω, 5%	RSMD0603 (not assembled)
R1, R2, R3	120 Ω, 1%	RSMD1206
R4	10k Ω, 1%	RSMD0603
R5, R6	1k Ω, 1%	RSMD0603
U1	iC-MCB QFN16 3X3	
U2	iC-HF QFN32 5X5	Differential line driver
U3	S9KEAZN8AMFK QFN24 4X4	Onboard MCU
U4	20MHz OSC4 SMD 5X3.2	Oscillator
S1_1	MK012G Socket	not assembled
S1_2	MK017G Socket	not assembled
S1_3	MK018G Socket	not assembled

ONBOARD HOST MCU

To enable a convenient evaluation of iC-MCB, the evaluation board is delivered with an onboard host microcontroller. At start-up the MCU configures iC-MCB via SPI. Therefor a dedicated set of configuration parameters is stored in the microcontroller's flash memory. After successful configuration the microcontroller provides single-cycle data (e.g. a counter value) to iC-MCB which is then accessible by a connected BiSS master. By using BiSS C register communication iC-MCB's configuration can be adjusted and a dedicated set of the MCU's registers accessed (e.g. in order to adjust the single-cycle data's content). Figure 3 shows the interface diagram between iC-MCB and the MCU.

To provide single-cycle data periodically the MCU is triggered externally by iC-MCB with an interrupt request (IRQ).

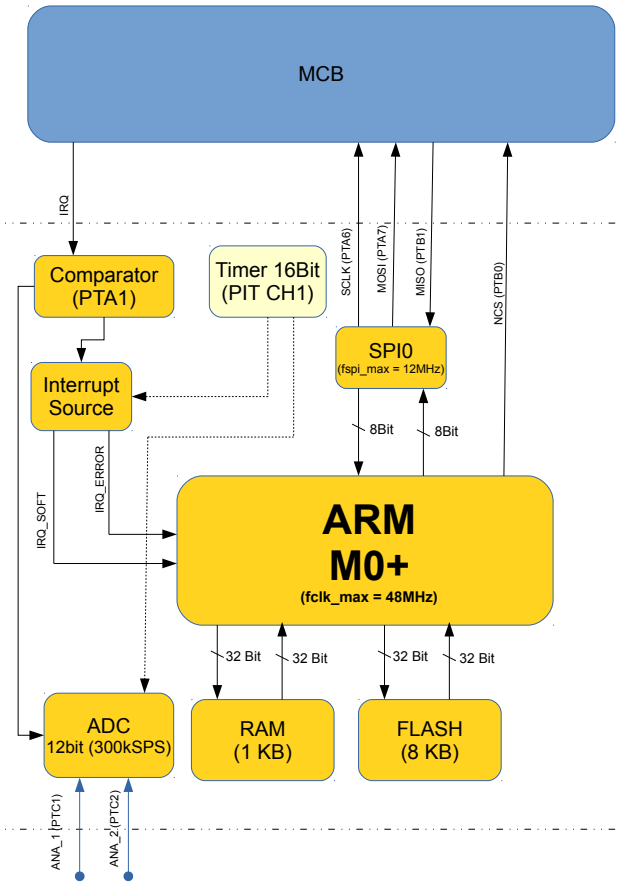

Figure 7: Interface diagram between iC-MCB and host MCU (Freescale® S9KEAZN8AMFK)

For further information about the onboard host MCU Freescale® S9KEAZN8AMFK, please check www.freescale.com.

BiSS REGISTER MAP AND CONFIGURATION

Configuration of iC-MCB (addr. 0x60 ...0x6F) and a dedicated set of the host MCU's registers (other registers) can be accessed via BiSS. Table 1 shows the content of the accessible registers.

Addr.	Name	Value (Default)	Comment
0x00 ...0x3F	Registers of selected bank	Depends on bank "Not implemented"	For highest slave ID For lower slave ID(s)
0x40	Bank selection	0x00	-
0x41	EDS bank	0x00	No EDS available
0x42 ...0x43	Profile ID	0x01 02 0x03 04	For highest slave ID For lower slave ID(s)
0x44 ...0x47	Serial number	0x22 33 44 55	-
0x48 ...0x4D	Host MCU functions	0x00 00 00 1B 01 01	See HOST MCU FUNCTIONS
0x4E ...0x4F	Reserved	0x00 00	-
0x50 ...0x5F	Host MCU flash memory	0x59 02 00 00 00 30 01 00 0x00 00 00 00 15 84 00 00	Loaded into MCU and iC-MCB configuration RAM at startup.
0x60 ...0x6F	iC-MCB configuration RAM	0x59 02 00 00 00 30 01 00 0x00 00 00 00 15 84 00 00	According to iC-MCB datasheet. Write access via BiSS.
0x70	Host MCU configuration status	MCU_STAT	See Table 6
0x71 ...0x73	Reserved	0x00 00 00 00	-
0x74	Host MCU commands	MCU_CMD	See Table 7
0x75 ...0x77	Reserved	"Not implemented"	-
0x78 ...0x7D	Device ID	0x4D 43 42 02 01 00	ASCII code for 'MCB'. Includes host firmware version at addr. 0x7B and 0x7C
0x7E ...0x7F	Manufacturer ID	0x69 43	ASCII code for 'iC'
Notes	Registers 0x7B and 0x7C contain the implemented firmware version: - Firmware Version 1.04: Compatible to GUI Software Version A1 - Firmware Version 2.01: Compatible to GUI Software Version B1		

Table 1: Table of registers accessible by BiSS Master

BiSS register accesses to address range 0x60...0x6F are purely managed by iC-MCB. Accesses to other registers are managed by the host MCU. This includes confirmation of the read or write access, providing register data from its memory to iC-MCB (BiSS register read access) and collecting data from iC-MCB (BiSS register write access).

HOST MCU FUNCTIONS

The onboard Host MCU provides a dedicated set of functions that enable a fast and simple getting started for evaluating iC-MCB. Using a BiSS adapter (e.g. MB5U) and the iC-MCB Evaluation Software GUI access to the host MCU functions as well as iC-MCB's configuration registers is enabled. At startup and after adjusting the host MCU functions the host MCU configures iC-MCB accordingly. For instance when another "Predefined Function" is selected the host MCU adjusts the data length configuration (parameters DLEN1 and DLEN2) in iC-MCB.

The following functions are provided by the onboard host MCU and can be adjusted in the iC-MCB evaluation software GUI in tab "Host MCU Functions". After selecting the desired MCU function, click "Write to MCU RAM" to execute function a shown in Figure 8.

Default configuration of host MCU

PREDEFINED FUNCTION	Addr. 0x48; bit 7:0	R/W
Code	Function	
0x00	24 bit Counter	
0x01	12 bit Analog-to-Digital Converter (ADC) Channel ANA_1 on pin PTC1 of MCU.	
0x02	12 bit Analog-to-Digital Converter (ADC) Channel ANA_2 on pin PTC2 of MCU.	
0x03	12 bit Analog-to-Digital Converter (ADC) on Channels ANA_1 & ANA_2 of MCU	
0x04	24 bit Counter & 12 bit ADC Channel ANA_1 on pin PTC1 of MCU	
0x05	24 bit Counter & 12 bit ADC Channel ANA_2 on pin PTC2 of MCU	
0x06	BiSS Safety Encoder Emulation (24 bit SPW Safety-Counter & 28 bit CPW Control-Counter)	
0xFF	No Single-Cycle Data provided by Host MCU (suitable for using the Fast Sensor Interface).	
other	Reserved	
Notes	ADC sampling has to be deactivated (ADCMODE = 0x02) for FUNCTION = 0x06.	

Table 2: Predefined Function Selection

ADCMODE	Addr. 0x49; bit 7:0	R/W
Code	Function	
0x00	Internal ADC IRQ of host MCU used for sampling of analog signal at pin PTC1 & PTC2 (with start bit delay, longer SCD cycle)	
0x01	Internal ADC timer of host MCU used for sampling of analog signal at PTC1 & PTC2 (without start bit delay, shorter SCD cycle)	
0x02	ADC sampling of analog signal at PTC1 & PTC2 turned off (must be set for Predefined Function 0x06)	
other	Reserved	
Notes	ADCMODE takes effect on FUNCTION = 0x01...0x05. ADC sampling has to be deactivated (ADCMODE = 0x02) for FUNCTION = 0x06.	

Table 3: ADC Sample Mode

INTERFACE	Addr. 0x4A; bit 7:0	R/W
Code	Function	
0x00	BiSS (iC-MCB's IRQ signal used, BANKSW=0, ACQMODE=1)	
0x01	SSI (iC-MCB's IRQ signal used, BANKSW=1, ACQMODE=0)	
0x02	SSI (MCU IRQ Timer instead of iC-MCB's IRQ signal used, BANKSW=1, ACQMODE=0)	
0x03	BiSS (MCU IRQ Timer instead of iC-MCB's IRQ signal used, BANKSW=1, ACQMODE=0)	
other	Reserved	

Table 4: Interface Mode

TIMER	Addr. 0x4B; bit 7:0	R/W
Code	MCU IRQ Timer Value in µs	
0x00...0x1A	reserved	
0x1B	18 (recommended)	
0x1C...0xFF	2/3*Code	
Notes	MCU IRQ Timer Value is only used for INTERFACE=0x02 and INTERFACE=0x03.	

Table 5: MCU IRQ Timer Value

MCU_STAT	Addr. 0x70; bit 7:0	R
Code	Function	
0x00	Flash Configuration loaded into MCU and iC-MCB RAM. MCU RAM Configuration not changed.	
0x11	MCU RAM Configuration changed but not activated (missing CMD = 0xBE)	
0x10	MCU RAM Configuration changed and activated with CMD = 0xBE but not in Flash (CMD = 0xFF)	
other	reserved	

Table 6: Status of MCU Configuration

MCU_CMD	Addr. 0x74; bit 7:0	W
Code	Function	
0xBE	Activate new Configuration entered in MCU RAM (0x48...0x4D)	
0xDA	Load iC-MCB Configuration from Flash to RAM.	
0xDF	Load MCU and iC-MCB Configuration from Flash memory to RAM.	
0xFF	Writes MCU and iC-MCB Configuration from RAM to Flash memory.	
other	reserved	

Table 7: Commands for MCU Configuration

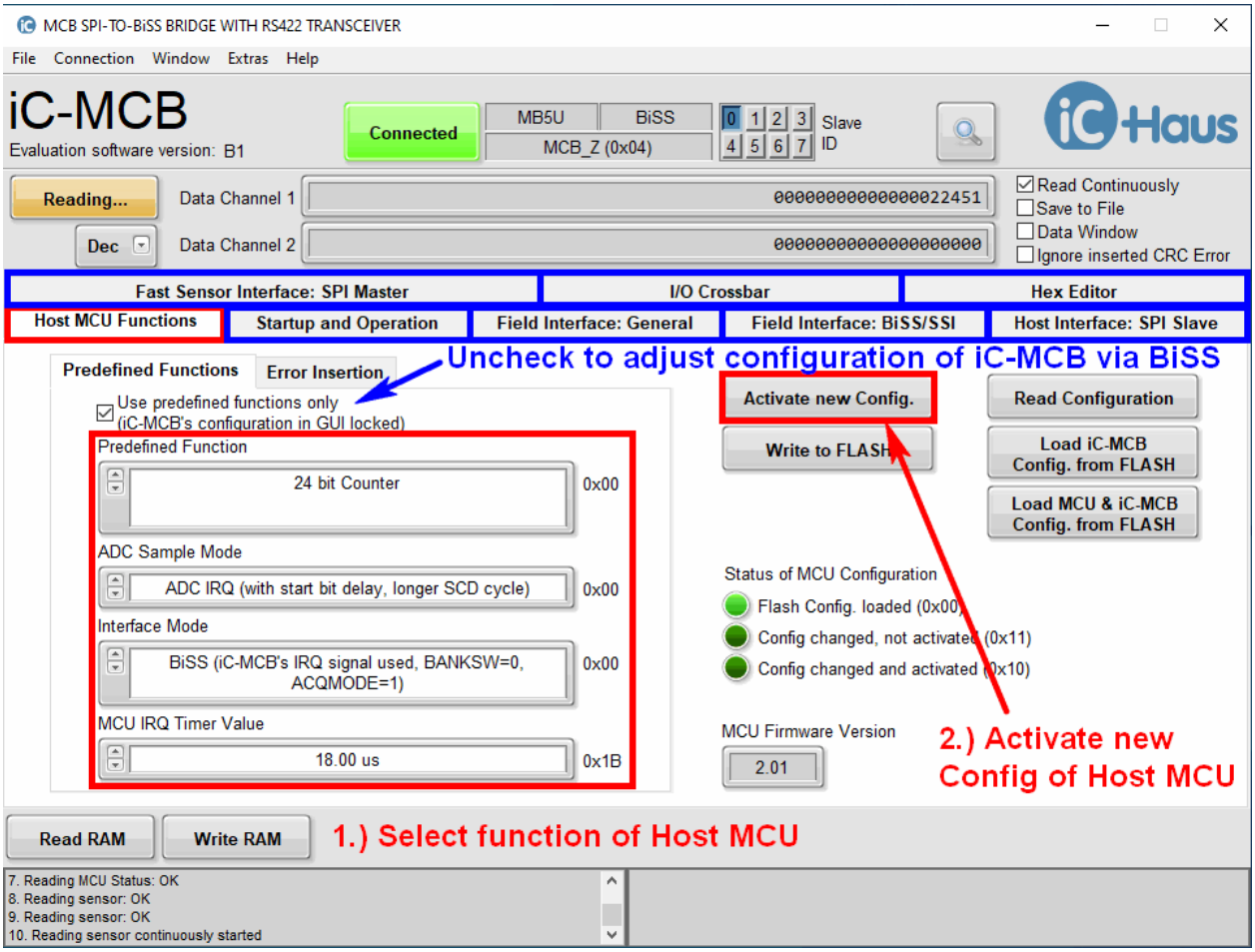

Figure 8: Configuration of Host MCU in iC-MCB Evaluation Software GUI

PREDEFINED FUNCTION 0x00: 24 bit Counter

The predefined function 0x00 configures the MCU to provide a 24 bit counter value to iC-MCB that is incremented with each BiSS frame. A single data channel is configured and one BiSS slave ID is occupied. The single-cycle data (SCD) consists of the 24 bit counter value and 2 bits status information that is protected by a 6 bit CRC (transmitted inversely). The status bits contain an error bit (nE) and a warning bit (nW) which are active low (A "1" indicates "no error"/ "no warning").

When entering the predefined function 0x00 mode, iC-MCB's data channel parameters such as number of data channels, data length and CRC are adjusted by the MCU to ensure proper configuration for this operating mode.

Predefined Function 0x00: 24 Bit Counter		
Data Channel	Single-Cycle Data (SCD)	CRC
1	24 bit Counter + 1 Error bit + 1 Warning bit	6 bit (polynomial 0x43, start value 0x00)

Table 8: BiSS Master Configuration for Predefined Function 0x00

PREDEFINED FUNCTION 0x01: 12 bit MCU ADC Channel 1

The predefined function 0x01 configures the MCU to provide a digital 12 bit value to iC-MCB that is converted from an analog source at the MCU's pin PTC1 in every BiSS frame. A single data channel is configured and one BiSS slave ID is occupied. The single-cycle data (SCD) consists of the 12 bit ADC value and 2 bits status information that is protected by a 5 bit CRC (transmitted inversely). The status bits contain an error bit (nE) and a warning bit (nW) which are active low (A "1" indicates "no error"/ "no warning").

When entering the predefined function 0x01 mode, iC-MCB's data channel parameters such as number of data channels, data length and CRC are adjusted by the MCU to ensure proper configuration for this operating mode.

Predefined Function 0x01: 12 bit MCU ADC Channel 1		
Data Channel	Single-Cycle Data (SCD)	CRC
1	12 bit Counter + 1 Error bit + 1 Warning bit	5 bit (polynomial 0x25, start value 0x00)

Table 9: BiSS Master Configuration for Predefined Function 0x01

The permitted input voltage range for the analog input pins of the MCU is 0 V . . . VDD.

PREDEFINED FUNCTION 0x02: 12 bit MCU ADC Channel 2

The predefined function 0x02 configures the MCU to provide a digital 12 bit value to iC-MCB that is converted from an analog source at the MCU's pin PTC2 in every BiSS frame. A single data channel is configured and one BiSS slave ID is occupied. The single-cycle data (SCD) consists of the 12 bit ADC value and 2 bits status information that is protected by a 5 bit CRC (transmitted inversely). The status bits contain an error bit (nE) and a warning bit (nW) which are active low (A "1" indicates "no error"/ "no warning").

When entering the predefined function 0x02 mode, iC-MCB's data channel parameters such as number of data channels, data length and CRC are adjusted by the MCU to ensure proper configuration for this operating mode.

Predefined Function 0x02: 12 bit MCU ADC Channel 2		
Data Channel	Single-Cycle Data (SCD)	CRC
1	12 bit Counter + 1 Error bit + 1 Warning bit	5 bit (polynomial 0x25, start value 0x00)

Table 10: BiSS Master Configuration for Predefined Function 0x02

The permitted input voltage range for the analog input pins of the MCU is 0 V . . . VDD.

PREDEFINED FUNCTION 0x03: 12 bit MCU ADC Channel 1 + 2

The predefined function 0x03 configures the MCU to provide two digital 12 bit value to iC-MCB that are converted from an analog source at the MCU's pins PTC1 and PTC2 in every BiSS frame. Two data channels are configured and two BiSS slave IDs are occupied. For each data channel the single-cycle data (SCD) consists of the 12 bit ADC value and 2 bits status information that is protected by a 5 bit CRC (transmitted inversely). The status bits contain an error bit (nE) and a warning bit (nW) which are active low (A "1" indicates "no error"/ "no warning").

When entering the predefined function 0x03 mode, iC-MCB's data channel parameters such as number of data channels, data length and CRC are adjusted by the MCU to ensure proper configuration for this operating mode.

Predefined Function 0x03: 12 bit MCU ADC Channel 1 + 2		
Data Channel	Single-Cycle Data (SCD)	CRC
1	12 bit Counter + 1 Error bit + 1 Warning bit	5 bit (polynomial 0x25, start value 0x00)
2	12 bit Counter + 1 Error bit + 1 Warning bit	5 bit (polynomial 0x25, start value 0x00)

Table 11: BiSS Master Configuration for Predefined Function 0x03

The permitted input voltage range for the analog input pins of the MCU is 0 V . . . VDD.

PREDEFINED FUNCTION 0x04: 24 bit Counter + 12 bit MCU ADC Channel 1

The predefined function 0x04 configures the MCU to provide a 24 bit counter value and a digital 12 bit value to iC-MCB that is converted from an analog source at the MCU's pin PTC1 in every BiSS frame. Two data channels are configured and two BiSS slave IDs are occupied. Besides the 24 bit counter value and 12 bit ADC value each data channel contains 2 bits status information. The single-cycle data (SCD) is protected by a 6 bit respectively 5 bit CRC that is transmitted inversely. The status bits consist of an error bit (nE) and a warning bit (nW) which are active low (A "1" indicates "no error"/ "no warning").

When entering the predefined function 0x04 mode, iC-MCB's data channel parameters such as number of data channels, data length and CRC are adjusted by the MCU to ensure proper configuration for this operating mode.

Predefined Function 0x04: 24 bit Counter + 12 bit MCU ADC Channel 1		
Data Channel	Single-Cycle Data (SCD)	CRC
1	24 bit Counter + 1 Error bit + 1 Warning bit	6 bit (polynomial 0x43, start value 0x00)
2	12 bit Counter + 1 Error bit + 1 Warning bit	5 bit (polynomial 0x25, start value 0x00)

Table 12: BiSS Master Configuration for Predefined Function 0x04

The permitted input voltage range for the analog input pins of the MCU is 0 V . . . VDD.

PREDEFINED FUNCTION 0x05: 24 bit Counter + 12 bit MCU ADC Channel 2

The predefined function 0x05 configures the MCU to provide a 24 bit counter value and a digital 12 bit value to iC-MCB that is converted from an analog source at the MCU's pin PTC2 in every BiSS frame. Two data channels are configured and two BiSS slave IDs are occupied. Besides the 24 bit counter value and 12 bit ADC value each data channel contains 2 bits status information. The single-cycle data (SCD) is protected by a 6 bit respectively 5 bit CRC that is transmitted inversely. The status bits consist of an error bit (nE) and a warning bit (nW) which are active low (A "1" indicates "no error"/ "no warning").

When entering the predefined function 0x05 mode, iC-MCB's data channel parameters such as number of data channels, data length and CRC are adjusted by the MCU to ensure proper configuration for this operating mode.

Predefined Function 0x05: 24 bit Counter + 12 bit MCU ADC Channel 2		
Data Channel	Single-Cycle Data (SCD)	CRC
1	24 bit Counter + 1 Error bit + 1 Warning bit	6 bit (polynomial 0x43, start value 0x00)
2	12 bit Counter + 1 Error bit + 1 Warning bit	5 bit (polynomial 0x25, start value 0x00)

Table 13: BiSS Master Configuration for Predefined Function 0x05

The permitted input voltage range for the analog input pins of the MCU is 0 V . . . VDD.

PREDEFINED FUNCTION 0x06: BiSS Safety Encoder Emulation (24 bit Counter + 28 bit Counter)

The predefined function 0x06 configures the MCU to provide a 24 bit counter value (Safety Position Word) and a 28 bit value (Control Position Word) to iC-MCB in every BiSS frame. Two data channels are configured to emulate a BiSS Safety Encoder Type RSM and two BiSS slave IDs are occupied.

Safety Position Word
Besides the 24 bit counter value data channel 1 contains 2 bits status information and a 6 bit Sign-of-Life counter. Its single-cycle data (SCD) is protected by a 16 bit CRC that is transmitted inversely. In safety applications the Safety Position Word (SPW) is used to verify validity of the transmitted Control Position Word.

Control Position Word
Data channel 2 contains a 28 bit counter value and 2 bits status information. Its SCD is protected by a 6 bit CRC that is transmitted inversely. In encoder (including safety) applications the Control Position Word is used for motor feedback and motion control.

The status bits of both data channels consist of an error bit (nE) and a warning bit (nW) which are active low (A "1" indicates "no error"/ "no warning"). Note, in BiSS Safety an inaccuracy is tolerated. For BiSS Safety Encoder Type RSM only the 21 MSB of both counter values are compared to each other and may deviate by +/-1 LSB.

When entering the predefined function 0x06 mode, iC-MCB's data channel parameters such as number of data channels, data length and CRC are adjusted by the MCU to ensure proper configuration for this operating mode.

Predefined Function 0x06: BiSS Safety Encoder Emulation (24 bit Counter + 28 bit Counter)		
Data Channel	Single-Cycle Data (SCD)	CRC
1	24 bit Counter + 1 Error bit + 1 Warning bit + 6 bit Sign-of-Life Counter	16 bit (polynomial 0x190D9, start value 0x00)
2	28 bit Counter + 1 Error bit + 1 Warning bit	6 bit (polynomial 0x43, start value 0x00)
Notes	Only the 21 MSB of both Counter values are compared in BiSS Safety Encoder Type RSM.	

Table 14: BiSS Master Configuration for Predefined Function 0x06

For predefined function 0x06 the ADC sampling has to be turned off (ADCMODE=0x02).

Error Insertion

ERR	Addr. 0x4C; bit 7:0	R/W
Code	Function	
0x00	Error Configuration is deactivated	
0x01	Error Configuration is activated by a low voltage level at pin PTC1 (Note: Due to a pull-up resistor at PTC1, error configuration is disabled on default)	
0x10	Error Configuration is activated (independent of voltage level at pin PTC1)	
other	reserved	

Table 15: Activation of Error Configuration

ERR_LSB	Addr. 0x4D; bit 0	R/W
Code	Function	
0	No error	
1	+/-2 LSB Error activated (occurs periodically). Note: The CPW's and SPW's 21 MSB are compared.	
ERR_CRC_S	Addr. 0x4D; bit 1	R/W
Code	Function	
0	No error	
1	CRC of Safety Position Word is calculated and corrupted by MCU. CRC calculation of iC-MCB is deactivated.	
ERR_CRC_C	Addr. 0x4D; bit 2	R/W
Code	Function	
0	No error	
1	CRC of Control Position Word is calculated and corrupted by MCU. CRC calculation of iC-MCB is deactivated.	
ERR_LC	Addr. 0x4D; bit 3	R/W
Code	Function	
0	No error	
1	Sign-of-Life Counter (SPW) is corrupted by MCU (+/-2 per frame).	
ERR_nE_S	Addr. 0x4D; bit 4	R/W
Code	Function	
0	No error	
1	Error flag of Safety Position Word is indicated (nE = 0).	
ERR_nE_C	Addr. 0x4D; bit 5	R/W
Code	Function	
0	No error	
1	Error flag of Control Position Word is indicated (nE = 0).	
ERR_nW_S	Addr. 0x4D; bit 6	R/W
Code	Function	
0	No error	
1	Warning flag of Safety Position Word is indicated (nW = 0).	
ERR_nW_C	Addr. 0x4D; bit 7	R/W
Code	Function	
0	No error	
1	Warning flag of Control Position Word is indicated (nW = 0).	

Table 16: Error Configuration

For predefined function 0x06 the ADC sampling has to be turned off (ADCMODE=0x02).

PREDEFINED FUNCTION 0xFF: No Single-Cycle Data provided by Host MCU

The predefined function 0xFF configures the MCU to provide no single-cycle data (SCD) to iC-MCB. This function is suitable for using iC-MCB's Fast Sensor Interface (e.g. as an SPI Master). In this mode iC-MCB's parameters have to be adjusted manually with respect to the connected sensor.

Predefined Function 0xFF: No Single-Cycle Data provided by Host MCU		
Data Channel	Single-Cycle Data (SCD)	CRC
Configuration depends on connected sensor		

Table 17: BiSS Master Configuration for Predefined Function 0xFF

For manual configuration of iC-MCB, disable "Use predefined functions only" as shown in Figure 8.

OFFBOARD EMBEDDED MCU USE

Pin NRES at J8 has a pull-up resistor which is used to enable operation of the onboard MCU on default.
The onboard MCU can be disabled in order to use an external/ offboard MCU with the MCB1D evaluation board.

To disable the onboard MCU pin NRES at J8 has to be pulled down to ground level.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2018-04-18	All	Initial release	All

Rel.	Rel. Date*	Chapter	Modification	Page
A2	2020-03-26	All	Overall update and reorganization for Host MCU firmware version 1.04 and software GUI	All
		DESCRIPTION OF JUMPERS	Renamed CB_SER → CB_FSI Added picture for I/O Crossbar Jumpers Added colored default jumper configuration CLK not available at IO2 IRQ not available at IO6	6f
		CIRCUIT SCHEMATIC	Schematic mirrored (according to iC-MCB and iC-HF block diagram) Schematic can now be searched for text (e.g. jumpers)	8
		ASSEMBLY PART LIST	Minor updates	10
		BiSS REGISTER MAP AND CONFIGURATION	Updated BiSS Register Map	12
		HOST MCU FUNCTIONS	Updated description of MCU functions	13ff
		OFFBOARD EMBEDDED MCU USE	Minor update	25

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2022-08-08	All	Overall update according to host MCU firmware version 2.01 and new software.	All
		ASSEMBLY PART LIST	Added details about onboard MCU.	10
		BiSS REGISTER MAP AND CONFIGURATION	Added firmware and GUI compatibility. Updated default configuration according to host MCU firmware version 2.01.	12
		HOST MCU FUNCTIONS	Updated Figure 8.	15
		PREDEFINED FUNCTION 0x00 ... 0xFF	Updated chapters according to new host MCU firmware version 2.01.	16ff
		PREDEFINED FUNCTION 0x06: BiSS Safety Encoder Emulation (24 bit Counter + 28 bit Counter)	Added functions to insert failure modes.	22f

* Release Date format: *YYYY-MM-DD*