iC-NK
LIGHT-GRID PULSE RECEIVER

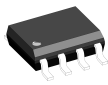
FEATURES

- Photoelectric amplifier with integrated bandpass
- Processing of light pulses up to 1 MHz
- Differential current-signal output with open drain low-side drivers
- Non-linear transfer function results in wide dynamic range of 0.3 µA to 1.8 mA for pulsed photo currents
- Fast recovery time of 0.5 µs within dynamic range
- System function tolerant versus flash lights
- 2-step shift register and control logic
- Compatible to CMOS levels
- Single 5 V supply
- Low standby current; circuit activation by input data
- Power-down reset
- ESD protection
- Option: extended temperature range of -40 to 85 °C

APPLICATIONS

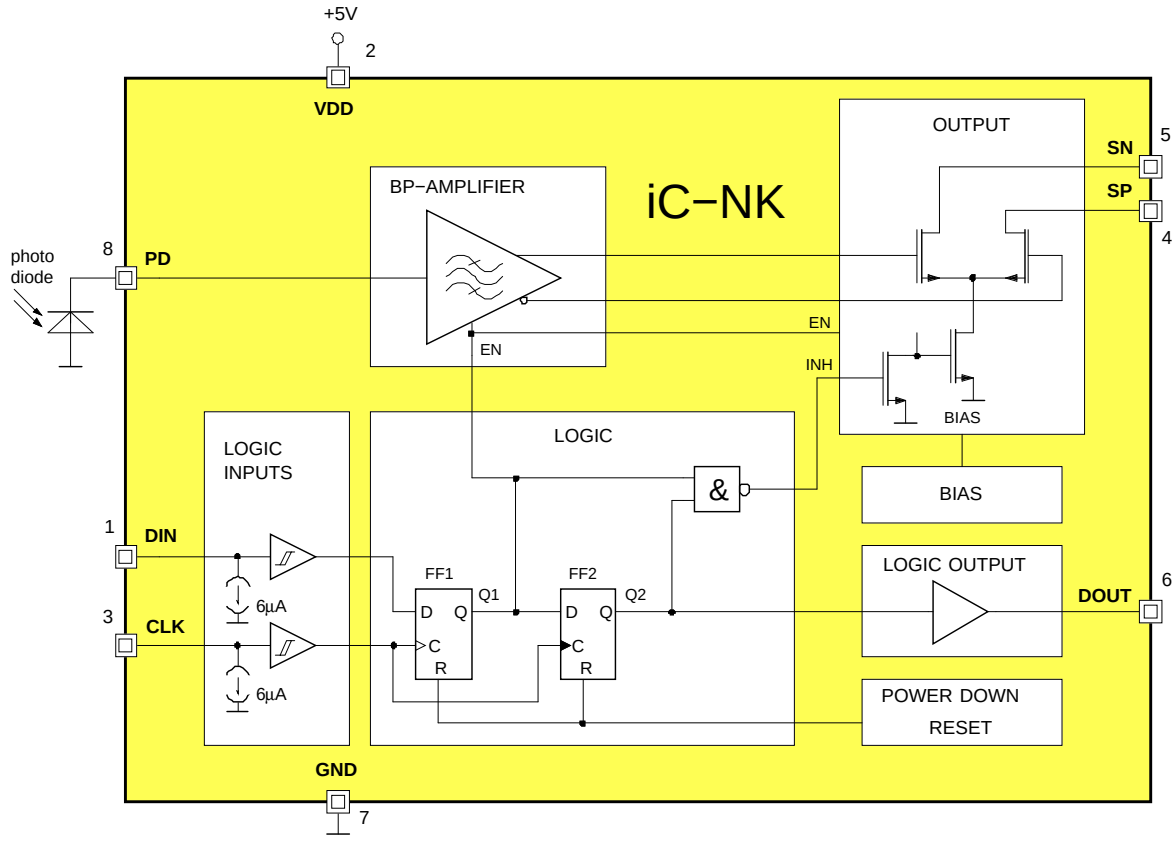
- Light curtains
- Light barriers
- Electro-sensitive protective equipment (ESPE)

PACKAGES



SO8

BLOCK DIAGRAM



DESCRIPTION

iC-NK is a detector iC for light curtains or light barrier applications.

Integrated on a single chip, iC-NK has a band-pass amplifier, a differential current output and a logic to activate the amplifier and differential current output. In its deactivated state, current consumption is extremely low and current outputs SN and SP are switched to high impedance (zero current).

The logic consists of a two-stage shift register where the first stage is triggered by the rising edge of CLK. The second flip-flop is triggered with the falling edge of CLK, producing an artificial delay. This prevents race conditions when data is transferred via the serial output to the next device in the chain.

A high at DIN is passed on to output Q1 of the first flip-flop with the first rising edge of CLK, activating the band-pass amplifier. The current output stage is activated when the second flip-flop also accepts the high signal with the falling CLK edge. Outputs SN and SP now both have a current of equal strength, providing the connected photo diode does not detect a change in illumination.

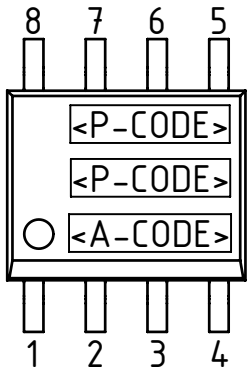
The rising edge of a received light pulse (which gives rise to an increase in the photo current) causes the output current at SN to decrease and that at SP to increase by an equal value. The sum of I(SN) + I(SP) remains constant. For light curtain applications where only one device is active at a time, outputs SN and SP can be connected to a two-wire bus.

After processing the serial input data at DIN, the amplifier and current output stage automatically return to standby mode when CLK reaches its second rising edge. It is thus advisable to set up chain circuitries with multiple beams using only a single data bit per run.

The device is protected against destruction by ESD. The logic inputs feature Schmitt trigger characteristics for high noise immunity. A voltage monitor deactivates the device with low voltage and resets the flip-flops. All pins are short-circuit-proof.

PACKAGING INFORMATION SO8 to JEDEC Standard

PIN CONFIGURATION SO8

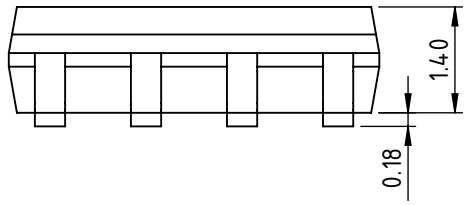


PIN FUNCTIONS

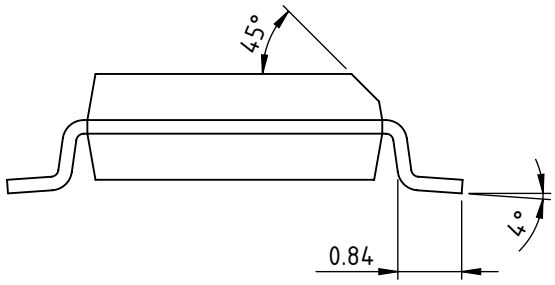
No.	Name	Function
1	DIN	Data Input
2	VDD	+5 V Supply Voltage
3	CLK	Clock Input
4	SP	Positive Differential Current Output
5	SN	Negative Differential Current Output
6	DOUT	Data Output
7	GND	Ground
8	PD	Photocurrent Input, Cathode of Photodiode

PACKAGE DIMENSIONS

SIDE



FRONT



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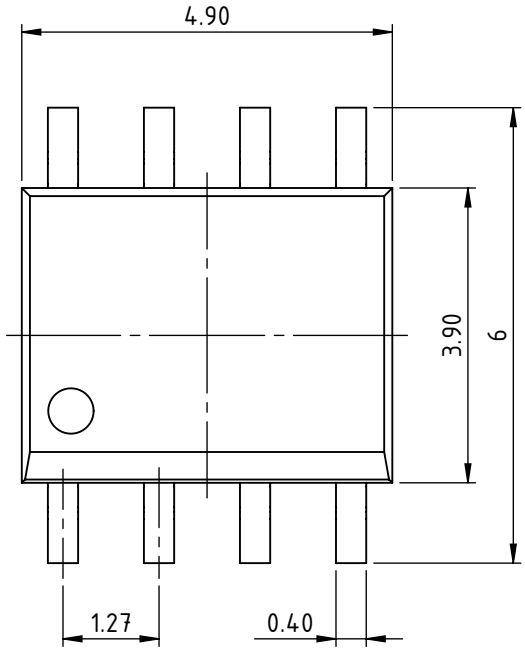
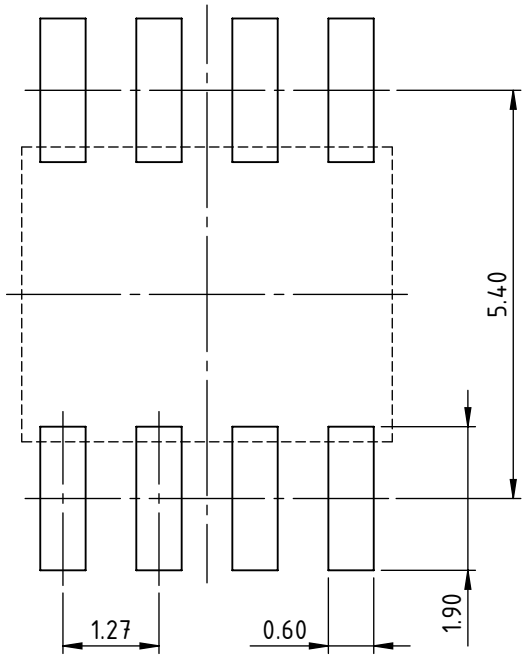


RECOMMENDED PCB-FOOTPRINT



All dimensions given in mm. Tolerances of form and position according to JEDEC MS-012.

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ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.5	7	V
G002	V()	Voltage at DIN, CLK, DOUT, SN, SP, PD		-0.5	VDD + 0.5	V
G003	Vd()	ESD Susceptibility at DIN, CLK, DOUT, PD, SN, SP	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G004	Tj	Junction Temperature		-40	150	°C
G005	Ts	Storage Temperature		-40	150	°C

THERMAL DATA

Operating Conditions: VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended temperature range of -40 to 85 °C on request)		0		70	°C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 5 V ±10 %, V(SN, SP) = 3.5 V...VDD, Tj = -40...85 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage Range		4.5		5.5	V
002	VDD	Required Supply Voltage Range for Logic Function	decreasing voltage VDD	1.7			V
003	I(VDD)	Supply Current in VDD (Standby)	DIN = CLK = hi or lo: BP amplifier and output disabled, logic levels: lo = 0...0.45 V, hi = VDD − 0.45 V...VDD Tj = 27 °C		 40	60	µA µA
004	I(VDD)	Supply Current in VDD	EN = hi: BP amplifier active, INH = hi: output disabled, I(PD) = -33...0 µA Tj = 27 °C		 0.3	0.5	mA mA
005	I(VDD)	Supply Current in VDD	EN = hi, INH = lo: BP amplifier and output activated Tj = 27 °C		 1.1	3	mA mA
006	VDDon	Turn-on Threshold VDD (Power-on Release)	 Tj = -40 °C			4.0 4.1	V V
007	VDDoff	Undervoltage Threshold VDD (Power-down Reset)	decreasing voltage VDD	2.6			V
008	VDDhys	Hysteresis	VDDhys = VDDon − VDDoff	200		500	mV
009	Vc()hi	Clamp Voltage hi at DIN, CLK, DOUT, PD, SN, SP	Vc()hi = V() − VDD, I() = 10 mA	0.4		1.25	V
010	Vc()lo	Clamp Voltage lo at DIN, CLK, DOUT, PD, SN, SP	VDD = 0 V, I() = -10 mA, other pins open	-1.25		-0.4	V
Bandpass Amplifier and Output PD, SN, SP							
101	C(PD)	Permissible Capacitance at PD				30	pF
102	V(PD)	Voltage at PD	Tj = 27 °C		0.9		V
103	Idc(PD)	Permissible DC Photocurrent in PD (Ambient Light Supression)		-15		0	µA
104	I(PD)mg	Monotone Gain Range of I(PD)pk	differential output current increases or remains constant when I(PD)pk increases (see Fig. 3)	-1.8		0	mA
105	twhi	Permissible Photocurrent Pulse Duration	see Fig. 3, 4	0.35			µs
106	twlo	Permissible Photocurrent Pause Duration	2^{nd} Gpk ≥ 90% 1^{st}Gpk, resp. of single pulse (see Fig. 4)	0.4			µs
107	trec	Power Flash Recovery Time	I(PD)pk = -5 mA, magnitude of photocurrent integral equal to 15 mAs			5	µs
108	Gpk	Pulse Current Gain	Gpk = (Ipnpk − IO ∗ ISUM) / I(PD)pk; I(PD)dc = -33...0 µA, I(PD)pk = -3 µA...-300 nA, tr = tf = 0.1 µs, twpk = 0.5 µs (see Fig. 3)	150		350	
109	Gac	AC Current Gain	I(PD)dc = -33...-2.5 µA, I(PD)ac = 5 µApp sinusoidal waveform, frequency for max. gain	280		500	
110	fl	Lower Cut-off Frequency (-3 dB)	I(PD)dc = -33...-2.5 µA, I(PD)ac = 5 µApp sinusoidal waveform Tj = 27 °C	0.32	 0.42	0.67	MHz MHz
111	fh	Upper Cut-off Frequency (-3 dB)	I(PD)dc = -33...-2.5 µA, I(PD)ac = 5 µApp sinusoidal waveform Tj = 27 °C	1.4	 2.0	2.65	MHz MHz
112	fΔ	Bandwidth (-3 dB)	fΔ = fh − fl Tj = 27 °C	1.0	 1.6	2.0	MHz MHz
113	V(SN,SP)	Permissible Voltage at SN, SP		3.5		VDD	V
114	ISUM	Output Currents I(SN) + I(SP)	 Tj = 27 °C	7.0	 10.0	13.5	mA mA
115	IO	Relative Offset Current	IO = (I(SN) − I(SP)) / ISUM; I(PD) = 0	-10		10	%
116	Ilk	Leakage Current I(SN) + I(SP)	output stage disabled			5.0	µA
117	Idlk()	Differential Leakage Current	Idlk() = I(SN) − I(SP); I(PD)pk = -1.8 mA, twhi = 0.5 µs, output disabled (see Fig 3)	-0.1		0.1	µA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 5 V ±10 %, V(SN, SP) = 3.5 V...VDD, Tj = -40...85 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
118	Ipn()	Differential Output Current	Ipn() = I(SN) − I(SP); I(PD)pk = -30 µA (see Fig. 3)	-9.0		-5.0	mA
119	Ipn()	Differential Output Current	Ipn() = I(SN) − I(SP); I(PD)pk = -300 µA (see Fig. 3)	-14.0		-5.0	mA
120	INoise	Differential Output Current Noise (RMS)	I(PD)dc = -33 µA, RGen = 500 kΩ, no additional filter , Tj = 27 °C (see Fig. 5)		4.0		µA
121	INoise	Differential Output Current Noise (RMS)	I(PD)dc = -33 µA, RGen = 500 kΩ, with BP filter 300 kHz...3.6 MHz, Tj = 27 °C (see Fig. 5)		2.5		µA
122	tp()IDCon	Output Stage Turn-on Delay: CLK hi → lo to 90% I(SN), I(SP)	I(PD)dc = -33 µA...0, I(PD)ac = 0 (see Fig. 4)			3.0	µs
123	tp()IDCoff	Output Stage Turn-off Delay: CLK lo → hi to 10% I(SN), I(SP)	I(PD)dc = -33 µA...0, I(PD)ac = 0 (see Fig. 4)			3.0	µs
Control Inputs DIN, CLK							
201	Vt()hi	Threshold Voltage hi				66	%VDD
202	Vt()lo	Threshold Voltage lo		33			%VDD
203	Vhys()	Schmitt-Trigger Input Hysteresis		400			mV
204	Ipd()	Pull-Down Current	V() = 5.0 V Tj = 27 °C	3	 6	12	µA µA
Output Buffer DOUT							
301	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(DOUT); I() = -4 mA			0.4	V
302	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	V
303	Isc()hi	Short-circuit Current hi	V() = 0 V Tj = 27 °C	-100	 -50	-25	mA mA
304	Isc()lo	Short-circuit Current lo	V() = VDD Tj = 27 °C	25	 50	100	mA mA
305	tr()	Rise Time	CL() = 50 pF Tj = 27 °C		 20	60	ns ns
306	tf()	Fall Time	CL() = 50 pF Tj = 27 °C		 20	60	ns ns
Switching Characteristics							
401	tplh(CLK − DOUT)	Propagation Delay: CLK hi → lo until DOUT lo → hi	CL(DOUT) = 50 pF (see Fig. 4) Tj = 27 °C		 25	60	ns ns
402	tphl(CLK − DOUT)	Propagation Delay: CLK hi → lo until DOUT hi → lo	CL(DOUT) = 50 pF (see Fig. 4) Tj = 27 °C		 25	60	ns ns

OPERATING REQUIREMENTS: Control Logic

Operating Conditions: VDD = 5 V ±10 %, Ta = 0...70 °C, CL() = 50 pF,
lo = 0...0.45 V, hi = VDD − 0.45 V...VDD, see Fig. 1 for reference levels and waveforms

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I001	ten	Activation Time: CLK lo → hi to CLK hi → lo	standby to amplifier operation (see Fig. 4)	2		µs
I002	tinh	Output Activation Time: CLK hi → lo until output ready to report	sufficient decay of transient differential output current: |I(SN) − I(SP) − IO ∗ ISUM| ≤ 30 µA (see Fig. 4)	5		µs
I003	tset	Setup Time: DIN stable before CLK lo → hi	see Fig. 2	50		ns
I004	thold	Hold Time: DIN stable after CLK lo → hi	see Fig. 2	50		ns
I005	f0	Permissible Frequency at CLK	duty cycle 50%		10	MHz

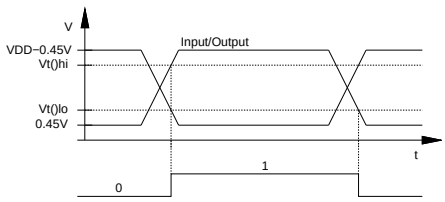

Figure 1: Reference levels

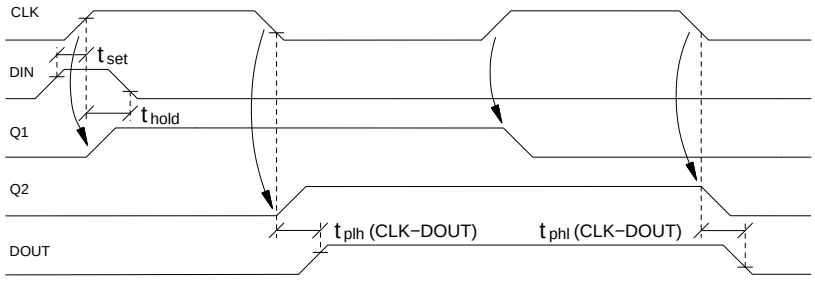

Figure 2: Timing characteristics

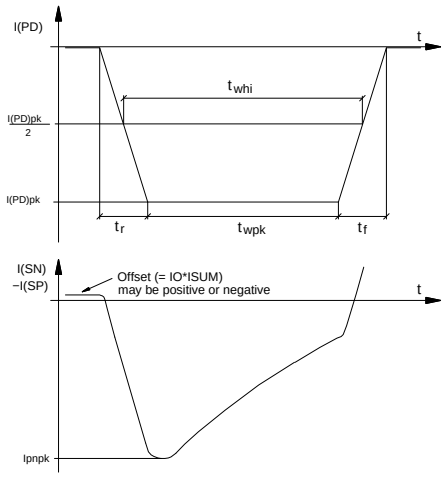

Figure 3: Differential output current pulse at SP and SN versus input current pulse at PD

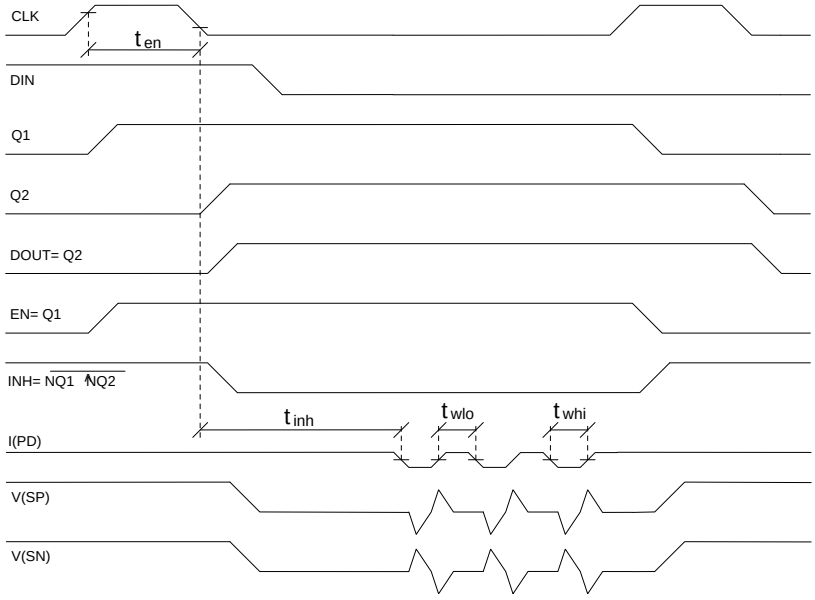

Figure 4: Timing characteristics (analogue section), outputs SP and SN with resistors to VDD

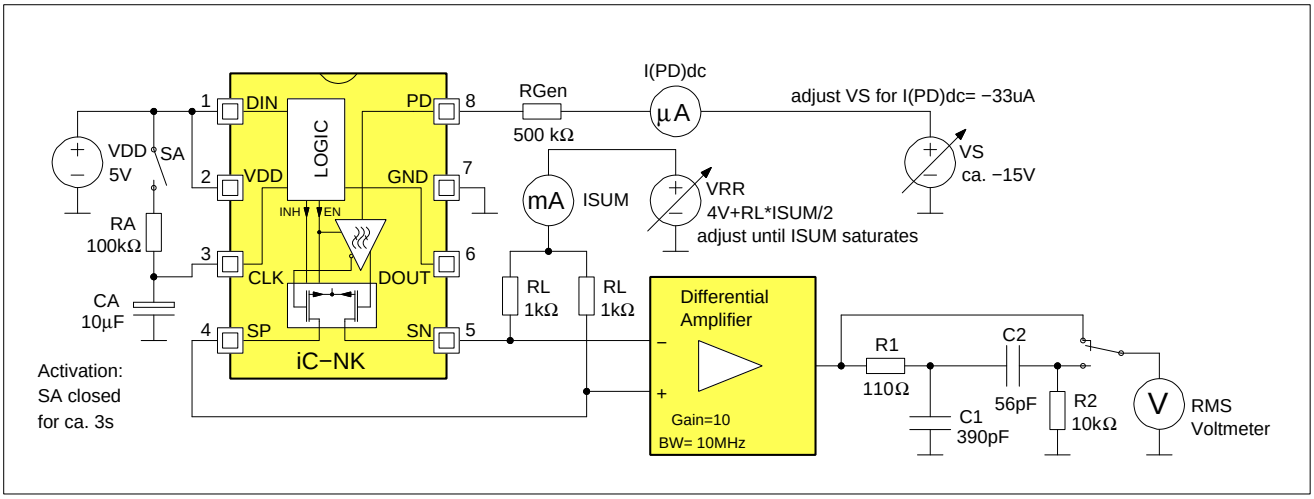

Figure 5: Noise measurement circuit

APPLICATIONS INFORMATION

Signal Processing

Figures 6 and 7 show output signal I(SP) – I(SN) in *normal* drive and in extreme overdrive (with the photo diode and input amplifier in saturation).

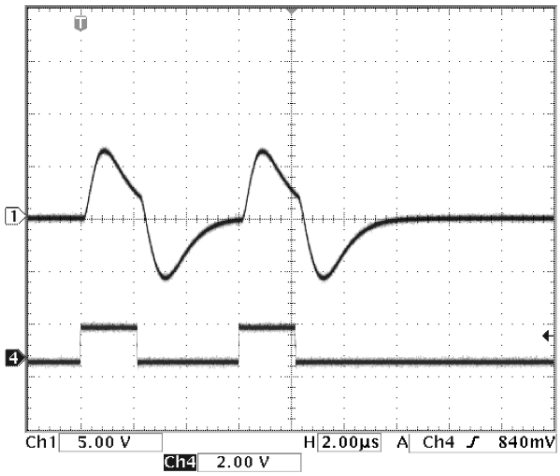

Figure 6: Regular input signals

It is clear from these diagrams that iC-NK, even when in overdrive, is not *blind* to a follow-on pulse. For evaluation purposes the response to the rising edge of the light pulse (i.e. the rising edge of the output signal) is to be used as it is this edge alone, even in the most extreme overdrive, which yields definite results. Evaluating the falling edge of the output signal or the level of the negative output signal half-wave (the recovery process at the end of a light pulse) is generally not advised.

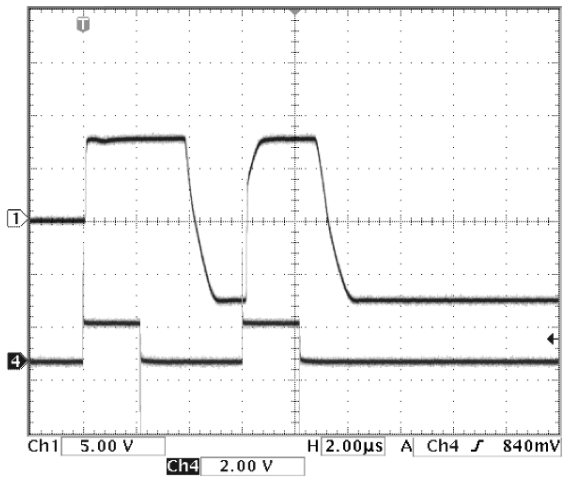

Figure 7: Excessive input signals

Light curtain

The circuit in Figure 8 shows several iC-NKs connected as a light curtain, where consecutive PIN diodes receive and evaluate clock-driven light pulses.

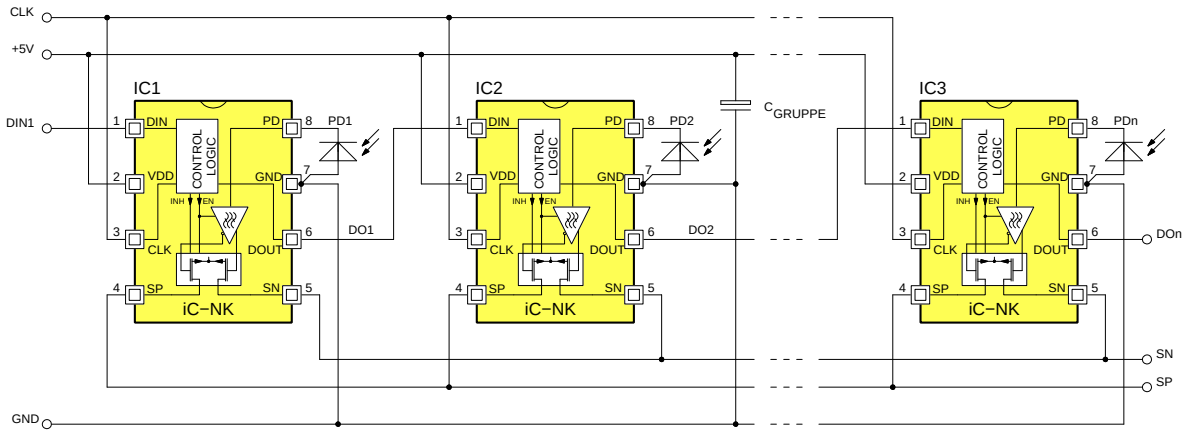

Figure 8: Schematic of a chain configuration

When discussing the function of iC-NK, it is assumed that all flip-flops have been reset, such as is the case, for example, after the supply voltage has been switched on.

Signal DIN1 = high activates iC1's band-pass amplifier with the first rising edge of CLK. The current output stage of iC1 is activated when the second flip-flop also accepts the high signal with the falling CLK edge. Until this point, outputs SN and SP remain at high impedance.

With no AC fractions in the receiver photo diode, approximately equal currents are drawn in SN and SP. After a time of tinh $\geq$ 5 µs, the transient differential currents in the current output stage caused when the device

is switched on have decayed, and iC-NK is ready to receive.

If current is drawn from PD (iC1) through a light pulse being detected by photo diode PD1, the currents at outputs SP and SN react as shown in Figure 9; I(SP) rises and returns to its initial value within a time constant determined by the bottom cut-off frequency of the band-pass amplifier, as long as the photo diode is constantly illuminated. When the light pulse decays, the current in SP first sinks and then reaches its standby value within the same time constant. The current in SN has a mirror-image time dependence, meaning the sum of I(SN) + I(SP) is constant.

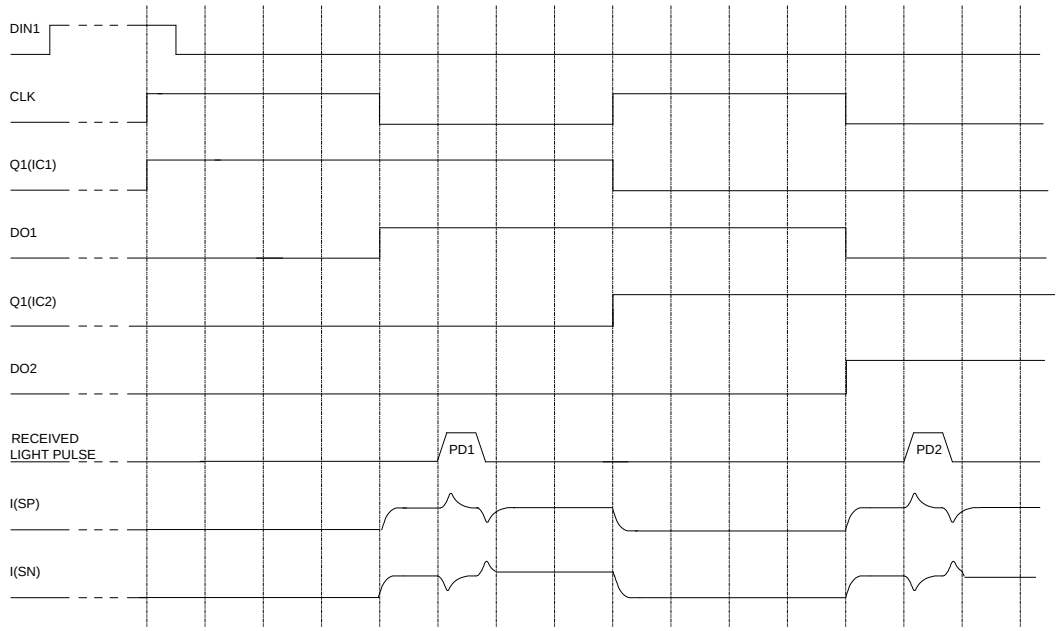

Figure 9: Signals for the chain configuration of Fig. 8

With DIN1 = 0, FF1 is reset at the next rising edge of CLK and the currents in the differential current output switched off. With the next falling edge, FF2 is reset. The pulse diagram is also valid for the subsequent components in the chain, i.e. the iCs configured as a light curtain make up a clock-driven shift register which passes on the input information.

Light curtain PCB layout

The PCB layout for light curtain receivers is not critical. The photodiode anode should be directly connected to iC-NK's GND pin so that voltage drops caused by the device's supply current are not coupled into the photo current signal.

As the power consumption is relatively small, only back-up capacitors with low capacitance values are required (typically 1 µF Elkos in parallel with 47 to 100 nF ceramic capacitors). The ceramic capacitors should be placed 7.5 cm apart and the Elkos at double this distance. The number of receivers blocked off as a group in this manner is irrelevant, as only one device is active and draws current at any one time.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2015-10-22	APPLICATIONS	Image updated	1
		PACKAGES	MSOP8 option dropped	1
		FEATURES	Optional extended temperature decreased to -40 °C	1
		PACKAGING INFORMATION	MSOP8 option dropped	2
		PACKAGING INFORMATION	Package dimensions added	3
		THERMAL DATA	Optional extended temperature decreased to -40 °C	4
		ELECTRICAL CHARACTERISTICS	Operating conditions: Junction temperature decreased to -40 °C	5-6
		ELECTRICAL CHARACTERISTICS	006: Max. value for -40 °C added	5
		ORDERING INFORMATION	MSOP8 option dropped	11

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-NK	SO8		iC-NK SO8

Please send your purchase orders to our order handling team:

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