iC-MCB

SPI-TO-BiSS BRIDGE WITH RS422 TRANSCEIVER

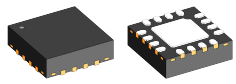
FEATURES

- BiSS Interface slave
- Full BiSS protocol support
- Two data channel configurable
- Three slave IDs occupiable
- Single-cycle data buffer of 64 byte organized in multiple banks for simultaneous access
- Built-in control communication
- RS422 line driver/receiver for BiSS/SSI point-to-point network
- BiSS bus structure capable
- SPI slave interface for sensor data provided by microcontroller
- Fast Sensor interface for direct sensor data provided by an SPI slave device
- BiSS safety related features: Two data channels for Control and Safety Position Word, 6/16 bit CRC + CRC start value
- BiSS timeout: adaptive, 2 µs, 20 µs
- SSI protocol support
- Operation from 3.0 V to 5.5 V
- Operating temperature range of -40° C to +125° C
- Space-saving 16-pin QFN package

APPLICATIONS

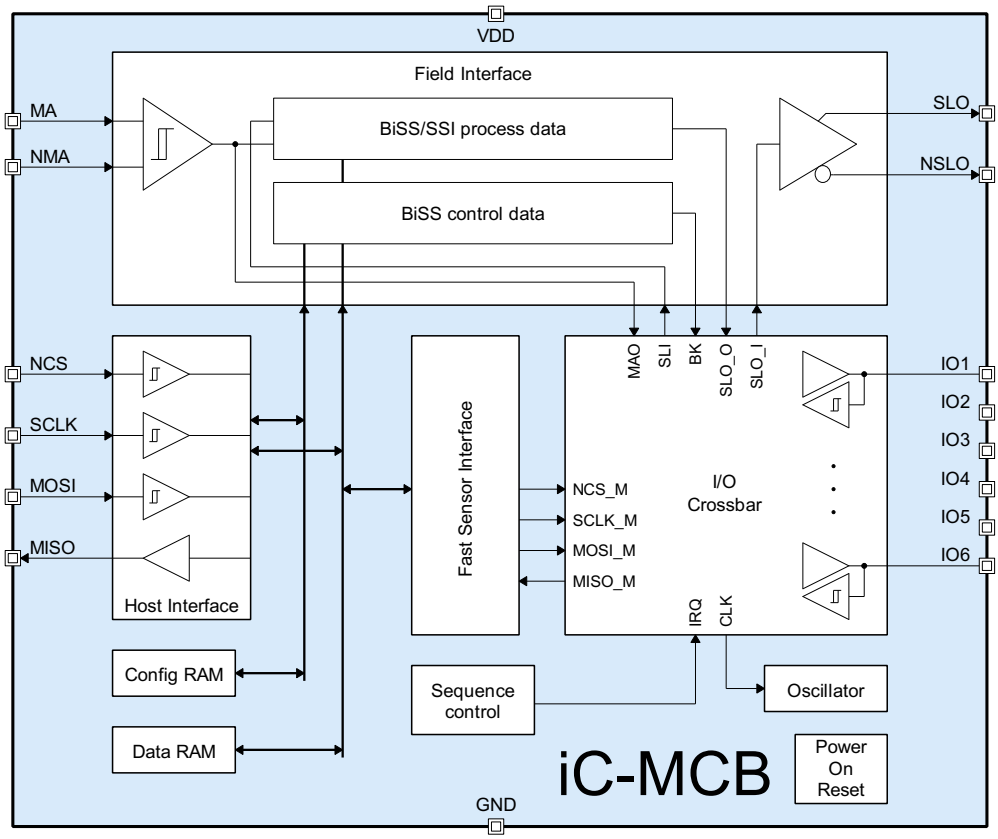
- BiSS slave implementation
- Multiple sensor devices
- Encoder
- Condition monitoring extension
- Diagnosis extension
- Torque sensor
- Acceleration sensor
- Inclinometer
- Safety light curtain

PACKAGES



16-pin QFN
3 mm x 3 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-MCB is a BiSS slave bridge component suitable to implement BiSS slave functionality into any device and platform.

It is designed for BiSS sensor implementations and also enables downgrading to SSI operation. Full BiSS C protocol functionality including single-cycle data (SCD) for sensors (SCDS) and control communication (e.g. for register accesses). Time-critical protocol specific actions are handled directly by the iC-MCB.

Besides the BiSS/SSI field interface, iC-MCB provides

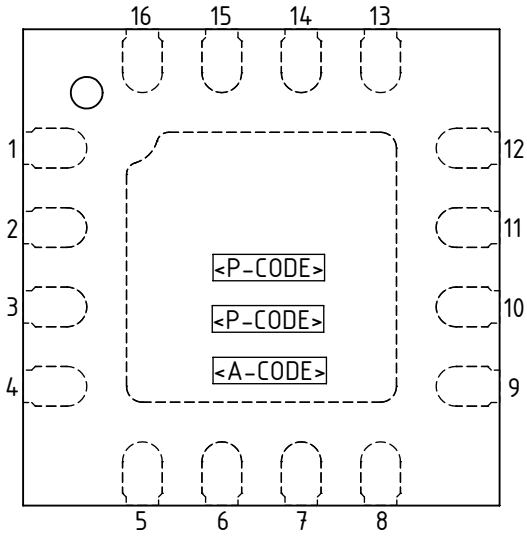
- a Host Interface (SPI Slave Interface)
- a Fast Sensor Interface (e.g. SPI Master Interface)

Typically, the host interface is used to configure iC-MCB on start-up, support iC-MCB during BiSS control communication and provide sensor data. However, iC-MCB can also operate as a master to automatically access various sensors (e.g. SPI sensors) directly by its Fast Sensor Interface at the I/O crossbar. To this end, the Fast Sensor Interface is fully configurable including signals, phase, polarity, clock frequency, data lengths and header.

With the integrated RS422 transceiver iC-MCB is perfectly equipped for BiSS point-to-point encoder applications with a maximum clock rate of 10 MHz. BiSS bus structures are also supported by enabling data input pin SLI and clock output pin MAO at the I/O crossbar.

PACKAGING INFORMATION

PIN CONFIGURATION
QFN16-3x3 (3 mm x 3 mm x 0.9 mm)
(according to JEDEC Standard MO-220)

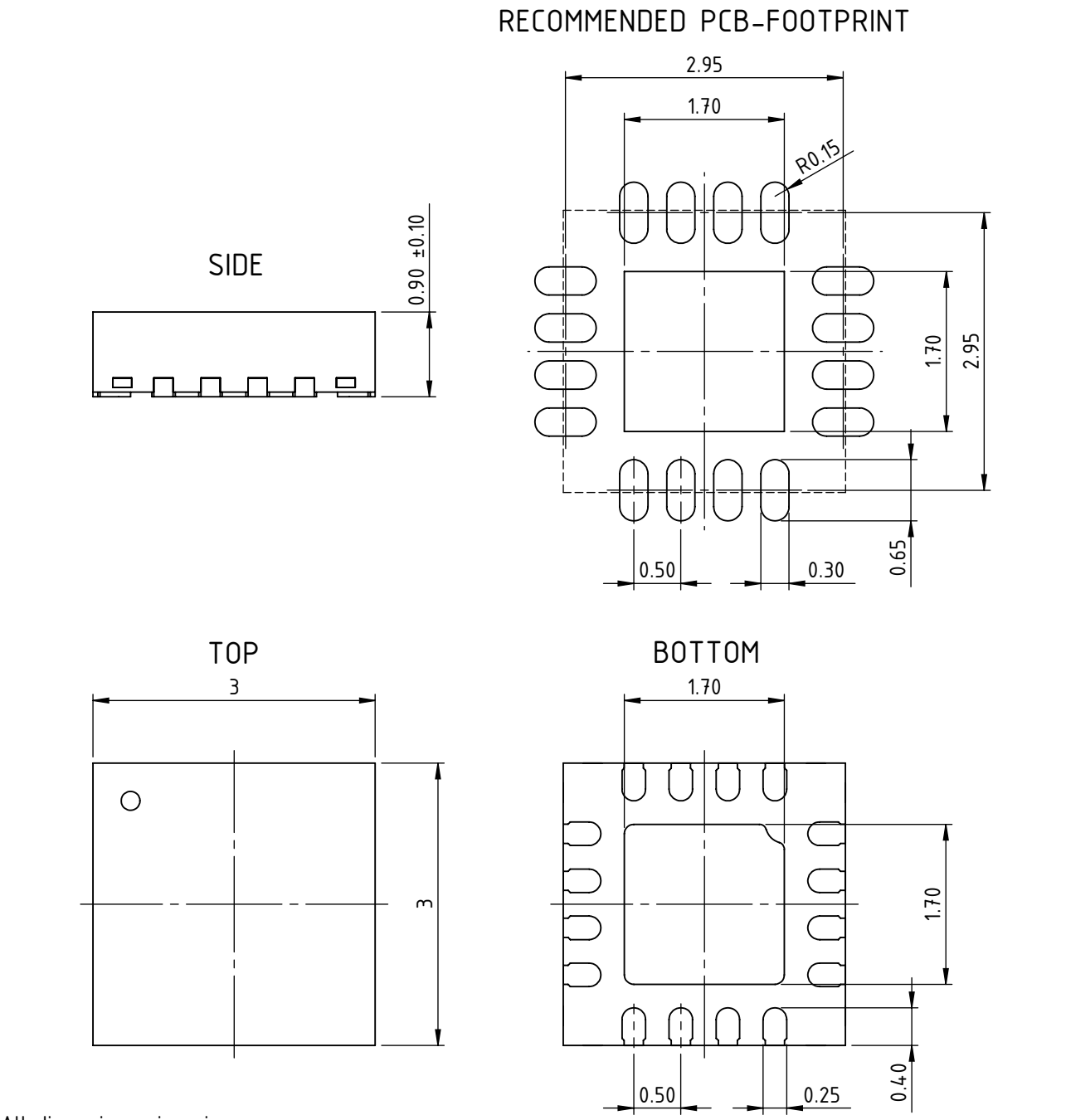


PIN FUNCTIONS

No.	Name	Function
1	MISO	SPI Serial Data Output
2	NCS	SPI Chip Select Input
3	SCLK	SPI Clock Input
4	MOSI	SPI Serial Data Input
5	IO1	Digital Port Input/Output
6	IO2	Digital Port Input/Output
7	IO3	Digital Port Input/Output
8	IO4	Digital Port Input/Output
9	IO5	Digital Port Input/Output
10	IO6	Digital Port Input/Output
11	GND	Ground
12	VDD	+3.0 V to +5.5 V Supply Voltage
13	NSLO	BiSS Data Line Output (inverted)
14	SLO	BiSS Data Line Output
15	MA	BiSS Clock Line Input
16	NMA	BiSS Clock Line Input (inverted)
	BP	Backside Paddle [1)]

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
1) Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS QFN16 3 mm x 3 mm x 0.9 mm



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

drb_qfn16-3x3-1_pack_1, 15:1

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V(VDD)	Voltage at VDD		-0.3	6	V
G002	V()	Voltage at MISO, NCS, SCLK, MOSI, IO1, IO2, IO3, IO4, IO5, IO6	V() < V(VDD) + 0.3 V	-0.3	6	V
G003	V()	Voltage at SLO, NSLO		-0.3	6	V
G004	V()	Voltage at MA, NMA		-10	10	V
G005	I(VDD)	Current in VDD		-100	150	mA
G006	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G007	Tj	Junction Temperature		-40	150	°C
G008	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	package QFN16-3x3	-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	QFN16-3x3 surface mounted to PCB according to JEDEC 51 thermal measurement standards		45		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 . . . 5.5 V, T_j = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VDD	Permissible Supply Voltage		3.0		5.5	V
002	I(VDD)	Supply Current	without load		5	8	mA
003	Vc()hi	Clamp Voltage hi at MISO, NCS, SCLK, MOSI, IO1, IO2, IO3, IO4, IO5, IO6	Vc()hi = V() - VDD; I() = 1 mA	0.4		1.5	V
004	Vc()lo	Clamp Voltage lo at MISO, NCS, SCLK, MOSI, IO1, IO2, IO3, IO4, IO5, IO6	I() = -1 mA	-1.5		-0.3	V
Field Interface: BiSS/SSI RS422 Line Driver Outputs SLO, NSLO							
201	Vs()hi	Saturation Voltage hi	Vs() = VDD - V(); I() = -20 mA			500	mV
202	Vs()lo	Saturation Voltage lo	I() = 20 mA			400	mV
203	Isc()hi	Short-circuit Current hi	V() = 0 V	-60	-30	-20	mA
204	Isc()lo	Short-circuit Current lo	V() = VDD	20	45	90	mA
Field Interface: BiSS/SSI RS422 Line Receiver MA, NMA							
210	Vin()	Permissible Input Voltage		-10		10	V
211	Vcm()	Input Common Mode Voltage		-7		7	V
212	Vdiff()	Differential Input Voltage	Vdiff() = V(MA) - V(NMA)	-12		12	V
213	Rin()	Input Resistance	MA vs. GND, NMA vs. GND	4			kΩ
214	Vt()diff	Differential Input Threshold	Vt(MA)diff = V(MA) - V(NMA) t_C = 334 ns (f_C = 3 MHz) t_C = 100 ns (f_C = 10 MHz)	 -200 -400		 200 400	 mV mV
215	Vt()hys	Differential Input Hysteresis	Vt()hys = V(MA) - V(NMA)	5	60	200	mV
216	Vt()hi	Input Threshold Voltage hi at MA	ESE = 1			70	%VDD
217	Vt()lo	Input Threshold Voltage lo at MA	ESE = 1	30			%VDD
Field Interface: BiSS/SSI Timing							
220	fclk()	Permissible Clock Frequency at MA	SSI protocol BiSS C protocol			4 10	MHz MHz
221	tr()	Rise Time hi at SLO, NSLO	RL = 100 Ω to GND, rise 10 % to 90 %			20	ns
222	tf()	Fall Time lo at SLO, NSLO	RL = 100 Ω to VDD, fall 90 % to 10 %			20	ns

223	t_P()	Output Propagation Delay at SLO	versus clock edge MA, ESE = 1;
			versus clock edge MA, ESE = 0;
			versus clock edge MAO via IOx;
			refers to timing Figure 1
				0
				0
				-10
						40
						75
						10
							ns
							ns
							ns

224	t_{out}()	Slave Timeout at SLO	adaptive (NTOA = 0);
			
			short (NTOA = 1, TOS = 1);
			
			long (NTOA = 1, TOS = 0);
				2/fosc	
					
					30/fosc
					
					375 /fosc
						375 /fosc	

225	T_{CLK}	Period of BiSS Timeout Sampling Clock	refers to Characteristics in BiSS C Protocol Description		1.33 /f_{OSC}		

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 . . . 5.5 V, T_j = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Host Interface SPI Slave NCS, SCLK, MOSI, MISO							
301	Vs()hi	Saturation Voltage hi at MISO	Vs() = VDD - V(); I() = -1.6 mA			0.4	V
302	Vs()lo	Saturation Voltage lo at MISO	I() = -1.6 mA			0.4	V
303	tr()	Rise Time at MISO	CL = 50pf VDD = 3.0 . . . 3.6 V, rise 10 % to 70 % VDD = 4.5 . . . 5.5 V, rise 10 % to 70 %			 35 25	 ns ns
304	tf()	Fall Time at MISO	CL = 50pf VDD = 3.0 . . . 3.6 V, fall 90 % to 0.8 V VDD = 4.5 . . . 5.5 V, fall 10 % to 0,8 V			 45 35	 ns ns
305	Vt()hi	Threshold Voltage hi at NCS, SCLK, MOSI				70	%VDD
306	Vt()lo	Threshold Voltage lo at NCS, SCLK, MOSI		30			%VDD
307	Vt()hys	Threshold Hysteresis at NCS, SCLK, MOSI		200			mV
308	Ipu()	Pull-up Current at NCS	V() = 0 V...VDD − 1 V	-70		-2	µA
309	Ipd()	Pull-down Current at SCLK, MOSI	V() = 1 V...VDD	2		80	µA
310	t_{P1}()	Output Propagation Delay at MISO	CL = 50pf, MISO = 0.5*VDD after SCLK hi → lo refers to timing Figure 3 VDD = 3.0 . . . 3.6 V VDD = 4.5 . . . 5.5 V			 40 25	 ns ns
Oscillator							
401	f_{osc}	Internal Oscillator Frequency		12	20	28	MHz
402	f_{osc_in}	External Oscillator Frequency	Input at I/O Crossbar (CB_CLK = 1)	12		18	MHz
Power-On Reset							
501	VDDon	VDD Turn-on Threshold	increasing voltage at VDD vs. GND	1.5		2.9	V
502	VDDoff	VDD Turn-off Threshold (undervoltage reset)	decreasing voltage at VDD vs. GND	1.2		2.7	V
503	VDDhys	VDD Hysteresis	VDDhys = VDDon - VDDoff	200			mV
I/O Crossbar: IO1, IO2, IO3, IO4, IO5, IO6							
601	Vs()hi	Saturation Voltage hi	Vs() = VDD - V(); I() = -1.6 mA			0.4	V
602	Vs()lo	Saturation Voltage lo	I() = -1.6 mA			0.4	V
603	tr()	Rise Time	CL = 50pf VDD = 3.0 . . . 3.6 V, rise 10 % to 70 % VDD = 4.5 . . . 5.5 V, rise 10 % to 70 %			 35 25	 ns ns
604	tf()	Fall Time	CL = 50pf VDD = 3.0 . . . 3.6 V, fall 90 % to 0.8 V VDD = 4.5 . . . 5.5 V, fall 10 % to 0,8 V			 45 35	 ns ns
605	Vt()hi	Threshold Voltage hi				70	%VDD
606	Vt()lo	Threshold Voltage lo		30			%VDD
607	Vt()hys	Threshold Hysteresis		200			mV
608	Ipd()	Pull-down Current	V() = 1 V...VDD	2		80	µA

OPERATING REQUIREMENTS: Field Interface BiSS

Operating Conditions: VDD = 3.0 . . . 5.5 V, T_j = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I001	t_{Cycle}	Permissible Frame Repetition		*	indefinite	
I002	t_{busy}	Processing Time	data available (asynchronous operation); Note, other modes delay data availability time (refer to Table 10)	2·t_C	500 ns	
I003	busy_s	Additional Start Bit Delay	ACQMODE = 1 or ENFSI = 1		1	t_C
I004	t_C	Permissible Clock Period		90		ns
I005	t_{L1}	Clock Signal hi Level Duration		45	t_{out}	ns
I006	t_{L2}	Clock Signal lo Level Duration		45	t_{out}	ns
I007	t_P	Output Propagation Delay		refer to Elec. Char. 223		
I008	t_{TO}	Slave Timeout at SLO	depending on NTOA and TOS	refer to Elec. Char. 224		
I009	t_{Wait}	Wait Time		500		ns

*Allow t_{out} to elapse.

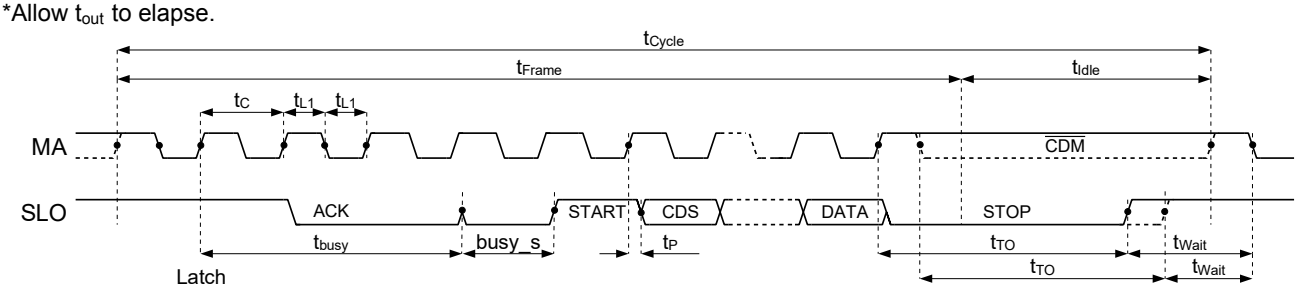


Figure 1: BiSS Protocol Timing

OPERATING REQUIREMENTS: Field Interface SSI

Operating Conditions: VDD = 3.0 . . . 5.5 V, T_j = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I101	t_{Cycle}	Permissible Frame Repetition		*	indefinite	
I102	t_C	Permissible Clock Period		250		ns
I103	t_{L1}	Clock Signal hi Level Duration		45	t_{out}	ns
I104	t_{L2}	Clock Signal lo Level Duration		45	t_{out}	ns
I105	t_{RQ}	REQ Signal lo Level Duration	ACQMODE = 0, ENFSI = 0	45	t_{out}	ns
I106	t_P	Output Propagation Delay		refer to Elec. Char. 223		
I107	t_{TO}	Slave Timeout at SLO	depending on TOS	refer to Elec. Char. 224		
I108	t_{Wait}	Wait Time		500		ns

*Allow t_{out} to elapse.

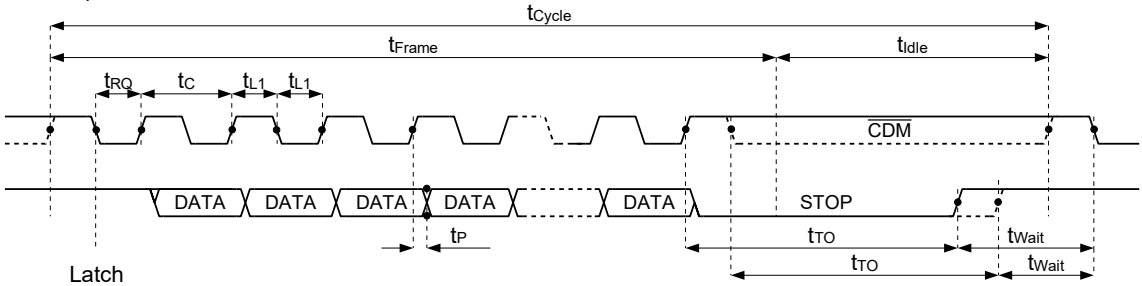


Figure 2: SSI Protocol Timing

OPERATING REQUIREMENTS: Host Interface SPI Slave

Operating Conditions: VDD = 3.0 . . . 5.5 V, T_j = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I201	t_C	Permissible Clock Period		50		ns
I202	t_{L1}	Clock Signal lo Level Duration		25		ns
I203	t_{L2}	Clock Signal hi Level Duration		25		ns
I204	t_{H1}	Hold Time: NCS lo after SCLK lo → hi		50		ns
I205	t_{H2}	Hold Time: MOSI stable after SCLK lo → hi		20		ns
I206	t_{S1}	Setup Time: NCS lo before SCLK lo → hi		25		ns
I207	t_{S2}	Setup Time: MOSI stable before SCLK lo → hi		20		ns
I208	t_{P1}	Propagation Delay: MISO stable after SCLK hi → lo		refer to Elec. Char. 310		
I209	t_{P2}	Propagation Delay: MISO hi impedance after NCS lo → hi			50	ns
I210	t_W	Wait Time: between NCS lo → hi and NCS hi → lo		250		ns

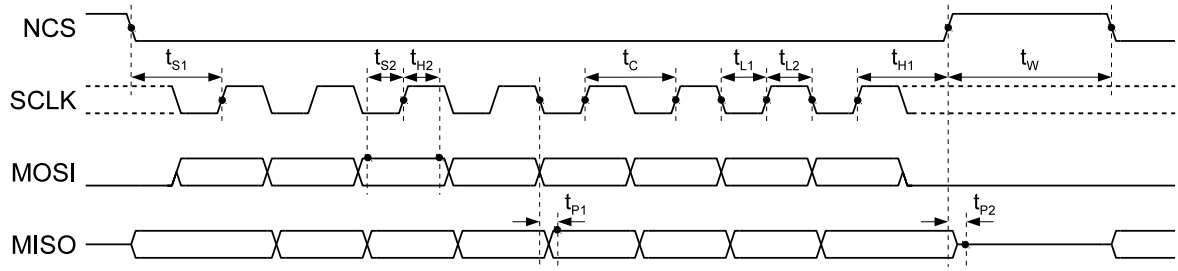


Figure 3: SPI Protocol Timing

CONFIGURATION PARAMETERS

REGISTER MAP (HOST INTERFACE)

DATA RAM								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00 ... 0x3F	Single-Cycle Data for data channels 1 and 2 (The Data RAM is separated into 4 memory banks of equal size, if BANKSW=1)							

Table 1: Data RAM (Access via SPI)

CONFIGURATION RAM								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIELD INTERFACE: BiSS/SSI								
0x40	GRAY1	ENDC1	DLEN1(5:0)					
0x41	CSTART1(5:0)						CPOLY1(1:0)	
0x42	0	ENDC2	DLEN2(5:0)					
0x43	CSTART2(5:0)						CPOLY2(1:0)	
0x44	BUSY(7:0)							
0x45	RSSI	ENSSI	CMD2EN	CMD01DI	ASID	TOS	NTOA	REGPROT
OPERATION								
0x46	0	0	0	0	0	USDST [1)]	BANKSW	ACQMODE
FAST SENSOR INTERFACE: SPI MASTER								
0x47	OSCDIV2 [2)]	ENFSI	DLFSI(5:0)					
0x48	0	IDLE	STAFSI(1:0)		HEADL(3:0)			
0x49	CLKDIV(3:0)				G2B	REQ_FT	CPHA	CPOL
0x4A	HEADER(7:0)							
RESERVED								
0x4B	0	0	0	0	0	0	0	0
I/O CROSSBAR								
0x4C	CB_SLO	CB_SLI	CB_MAO	CB_IRQ	CB_CLK	CB_FSI(2:0)		
STARTUP								
0x4D	CFGOK	0	ESE	0	CHPREL(3:0)			
BiSS CONTROL COMMUNICATION								
0x4E	RDATA(7:0)							
0x4F	0	0	0	CONFIRM [1)]	IVALID [1)]	CVALID(2:0)		
Notes								
[1)] Not implemented before chip revision Z. Must be zero if not implemented.								
[2)] Not implemented from chip revision Z. Must be zero if not implemented.								

Table 2: Configuration RAM (Access via SPI)

REGISTER MAP (BiSS)

CONFIGURATION RAM								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIELD INTERFACE: BiSS/SSI								
0x60	GRAY1	ENDC1	DLEN1(5:0)					
0x61	CSTART1(5:0)						CPOLY1(1:0)	
0x62	0	ENDC2	DLEN2(5:0)					
0x63	CSTART2(5:0)						CPOLY2(1:0)	
0x64	BUSY(7:0)							
0x65	RSSI	ENSSI	CMD2EN	CMD01DI	ASID	TOS	NTOA	REGPROT
OPERATION								
0x66	0	0	0	0	0	USDST [1)]	BANKSW	ACQMODE
FAST SENSOR INTERFACE: SPI MASTER								
0x67	OSCDIV2 [2)]	ENFSI	DLFSI(5:0)					
0x68	0	IDLE	STAFSI(1:0)		HEADL(3:0)			
0x69	CLKDIV(3:0)				G2B	REQ_FT	CPHA	CPOL
0x6A	HEADER(7:0)							
RESERVED								
0x6B	0	0	0	0	0	0	0	0
I/O CROSSBAR								
0x6C	CB_SLO	CB_SLI	CB_MAO	CB_IRQ	CB_CLK	CB_FSI(2:0)		
STARTUP								
0x6D	CFGOK	0	ESE	0	CHPREL(3:0)			
BiSS CONTROL COMMUNICATION								
0x6E	RDATA(7:0)							
0x6F	0	0	0	CONFIRM [1)]	IVALID [1)]	CVALID(2:0)		
Notes								
Other registers can only be accessed via BiSS, if implemented by the Host MCU as described in chapter BiSS Control Communication. [1)] Not implemented before chip revision Z. Must be zero if not implemented. [2)] Not implemented from chip revision Z. Must be zero if not implemented.								

Table 3: Configuration RAM (Access via BiSS)

STARTUP AND OPERATION

Startup

After power on the configuration RAM is automatically initialized with zeros and must then be programmed through the host (SPI) or the field (BiSS) interface. If the host (SPI) interface is used, it is recommended to set REGPROT to avoid access to iC-MCB's configuration via BiSS.

The chip release can be verified with the ROM value CHPREL.

CHPREL	Addr. 0x4D (SPI);	bit 3:0	R
	Addr. 0x6D (BiSS);	bit 3:0	R
0x0	iC-MCB		
0x1	Reserved		
0x2	iC-MCB 2		
0x3	iC-MCB 3		
0x4	iC-MCB Z		
0x5	Reserved		
0x6	iC-MCB Z2		
0x7 ... 0xF	Reserved		

Table 4: Chip release

After the configuration phase, which will end by setting the parameter CFGOK, the device is ready for BiSS respectively SSI access. While CFGOK is zero, the data output SLO remains high to allow error detection in the SSI output format; the device listens to a write access via BiSS.

CFGOK	Addr. 0x4D (SPI);	bit 7	R/W 0
	Addr. 0x6D (BiSS);	bit 7	R/W 0
0	Configuration data invalid, SLO remains high		
1	Configuration data valid		

Table 5: Tag configuration data as valid

Operation

The iC-MCB provides sensor data after receiving the request from the BiSS Interface. Therefore, two interfaces are implemented to import sensor data to the Data RAM.

- SPI master: The iC-MCB is active and uses a SPI master as a Fast Sensor Interface (FSI) to load sensor data from an external serial sensor. The interface is enabled with ENFSI. Detailed information can be found in chapter FAST SENSOR INTERFACE: SPI MASTER on page 29.
- SPI slave: The iC-MCB is passive and receives sensor data from a microprocessor using the host interface. Further details are described in chapter HOST INTERFACE: SPI SLAVE on page 19.

The operating sequence is shown in Figure 4. After a BiSS request the sensor data must be placed in the Data RAM. The following data transmission starts after a configurable delay to allow subsequent BiSS slaves to calculate their sensor data (see parameter BUSY). Unlike to the loading of sensor data via the Fast Sensor Interface, which starts always isochronic to the BiSS request, the microprocessors has two acquisition options.

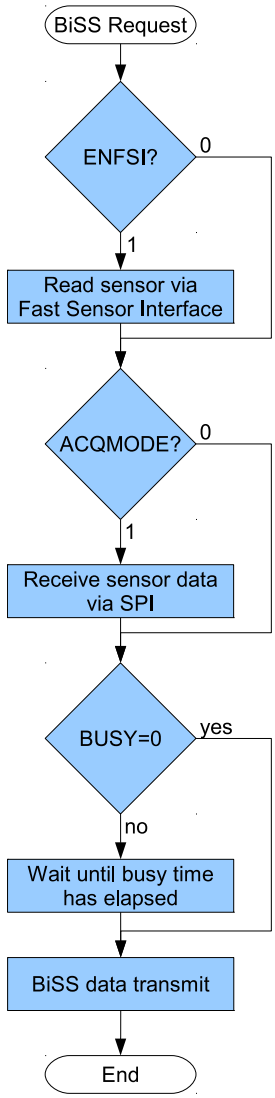


Figure 4: Sequence diagram

If ACQMODE = 1, the iC-MCB waits after signalizing the request with IRQ until sensor data is written with a particular SPI command (Transmit SDAD) into the 64 byte Data RAM. In the meantime the incomming data at SLI will be stored in the Data RAM. The host must

finish operation Transmit SDAD before the temporary buffer overflows to prevent data loss.

If ACQMODE = 0, the iC-MCB does not wait for Transmit SDAD. Instead sensor data are either written into the Data RAM independently and asynchronously to the BiSS/SSI frames via the host interface or automatically requested by iC-MCB's Fast Sensor Interface. In the first case the last stored sensor data is transmitted in the next BiSS/SSI frame without any additional delay. In the latter case iC-MCB delays the start bit of the BiSS frame until the sensor data has been completely received via the Fast Sensor Interface.

ACQMODE	Addr. 0x46 (SPI); bit 0 R/W 0 Addr. 0x66 (BiSS); bit 0 R/W 0
0	Independent of Transmit SDAD (SSI or BiSS)
1	Waiting for Transmit SDAD (BiSS only)
Notes	See Table 10 for application details.

Table 6: Acquisition mode

If sensor data is provided via the host interface and ACQMODE = 0, it is necessary to enable bank switching with parameter BANKSW, which separates the Data RAM into three banks and a temporary buffer with 16 bytes each.

BANKSW	Addr. 0x46 (SPI); bit 1 R/W 0 Addr. 0x66 (BiSS); bit 1 R/W 0
0	Bank switch disabled (one bank, see Table 35)
1	Bank switch enabled (three banks, see Table 9)
Notes	[1] See Table 10 for application details.

Table 7: Bank switch

Three banks are written alternately by the microcontroller (iC-MCB manages the bank selection automatically) and the fourth bank is used to temporarily store the last sent data. If no new sensor data has been written to iC-MCB by the microcontroller since the last BiSS frame, the parameter USDST configures, if the last sent sensor data is repeated (available in BiSS and mandatory in SSI), or if the sensor data is marked as invalid by sending zero data (available only in BiSS). In order to output proper data when using USDST = 1, the Data RAM needs to be initialized after power-on.

USDST	Addr. 0x46 (SPI); bit 2 R/W 0 Addr. 0x66 (BiSS); bit 2 R/W 0
0	Send zero data (BiSS only)
1	Use sensor data several times (mandatory in SSI)
Notes	[1] USDST is not implemented before chip revision Z. [2] See Table 10 for application details. [3] If USDST = 1, the Data RAM needs to be initialized with proper data before setting CFGOK = 1.

Table 8: Activity on missing sensor data

Note: The activity on missing sensordata is not defined before chip revision Z.

Table 9 shows the arrangement in the Data RAM if BANKSW is set.

Data RAM	Addr. 0x00...0x3F (SPI); bit 7:0 R/W 0
0x00 ... 0x0F	Bank 0
0x10 ... 0x1F	Bank 1
0x20 ... 0x2F	Bank 2
0x30 ... 0x3F	Temporary buffer for data received at SLI.

Table 9: Data RAM arrangement (BANKSW=1)

Application			Start Bit Delay at	Recommended Configuration		
Field Interface	**Sensor Data**	**SPI Operation[1]**	**Field Interface[2]**	**ACQMODE**	**BANKSW**	**USDST**
BiSS (ENSSI=0)	Input via Host	Synchronous	Waiting for Transmit SDAD	1	0	0
SSI (ENSSI=1)	Input via Host	Asynchronous	No delay	0	1	1
BiSS (ENSSI=0)	Input via FSI	Synchronous	Waiting for FSI	0	0	0
BiSS (ENSSI=0)	Input via Host	Asynchronous	No delay	0	1	0 or 1

Notes:

[1] Synchronous operation at the host interface is enabled with IRQ.

[2] Only in BiSS a sensor's processing time can be considered. iC-MCB delays the start bit of the BiSS frame while waiting for sensor data (until the rising edge of signal NCS at host interface or FSI respectively). The minimum start bit delay (BUSY) is considered and the start bit is additionally delayed as defined in I002 and I003.

Table 10: Typical applications and required configurations

FIELD INTERFACE: General

iC-MCB provides one RS422 line receiver for the clock input MA and one current limited RS422 driver for the data output SLO. The line receiver includes internal resistors to allow a common mode voltage range of -7 V to +7 V. A single ended TTL mode for MA can be selected with the parameter ESE.

ESE	Addr. 0x4D (SPI);	bit 5	R/W 0
	Addr. 0x6D (BiSS);	bit 5	R/W 0
0	Differential ended operation at MA, NMA		
1	Single-ended operation at MA		

Table 11: Enable single ended operation

FIELD INTERFACE: BiSS

The BiSS Interface is a serial, bidirectional interface which is suitable to transmit process data isochronously and to access memory registers (e.g. an electronic datasheet) of the slave device. For a detailed description of the protocol refer to the BiSS C Protocol Description.

BiSS Frame

A BiSS frame is used to interchange process data between master and slave and to transmit one bit in each direction for the control communication. Process data is distinguished into sensor data, which is transferred from slave to master, and actuator data for the opposite direction. The iC-MCB signalizes the start of each frame with IRQ at the first rising edge of MA. This first rising edge signals the slave to capture its sensor data and is in BiSS defined as the 'latch point'. Now the iC-MCB waits for sensor data (ACQMODE = 1), which must be provided via SPI with the command Transmit SDAD. The start bit is then generated when both the SPI command Transmit SDAD has been completed and the busy counter (configured by BUSY and measured from the latch point) has expired.

BUSY	Addr. 0x44 (SPI);	bit 7:0	R/W 0
	Addr. 0x64 (BiSS);	bit 7:0	R/W 0
Code	Minimum start bit delay		
	before chip release Z		from chip release Z	
	In clocks f_{OSC}	Time period	In clocks f_{OSC}	Time period
0x00	0	0 ns	0	0 ns
0x01	1	50 ns	4	200 ns
0x02 ... 0xFE	2 ... 254	100 ns ... 12.7 µs	8 ... 1016	400 ns ... 50.8 µs
0xFF	255	12.75 µs	1020	51 µs

Table 12: Minimum start bit delay

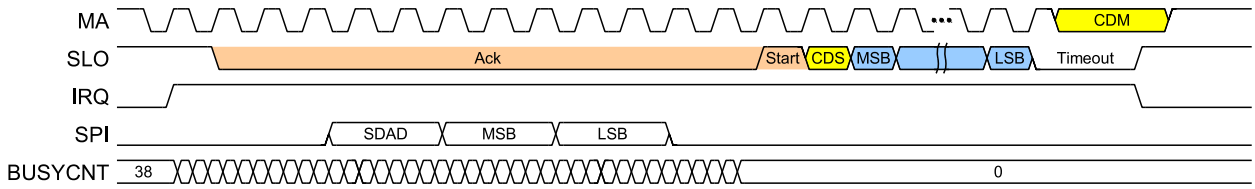


Figure 5: Start bit delay in BiSS frame

The process data is contained in logical data channels. Each data channel has a programmable data length (DLEN1, DLEN2) and CRC to increase the transmission safety. The generator polynomial (CPOLY1, CPOLY2) and the start value for CRC calculation (CSTART1, CSTART2) is programmable too. ENDC1 and ENDC2 enable the corresponding data channel. With the BiSS protocol two channels can be configured in iC-MCB. Process data contained in data channel 1 is received by the BiSS master first, followed by the process data in data channel 2.

DLEN1	Addr. 0x40 (SPI);	bit 5:0	R/W 0
	Addr. 0x60 (BiSS);	bit 5:0	R/W 0
0x00	1 bit		
...	(DLEN1 + 1) bit		
0x3F	64 bit		
Notes	If DLEN1 < 8, a CRC must be enabled (CPOLY1 > 0).		

Table 13: Data length channel 1

ENDC1	Addr. 0x40 (SPI); bit 6 R/W 0 Addr. 0x60 (BiSS); bit 6 R/W 0
0	Data channel 1 disabled
1	Data channel 1 enabled

Table 14: Enable data channel 1

CPOLY1	Addr. 0x41 (SPI); bit 1:0 R/W 0 Addr. 0x61 (BiSS); bit 1:0 R/W 0
0x0	no CRC generated (0 bit CRC)
0x1	CRC polynomial = 0x25 (5 bit CRC)
0x2	CRC polynomial = 0x43 (6 bit CRC)
0x3	CRC polynomial = 0x190D9 (16 bit CRC)

Table 15: CRC polynomial data channel 1

CSTART1	Addr. 0x41 (SPI); bit 7:2 R/W 0 Addr. 0x61 (BiSS); bit 7:2 R/W 0
0x00 . . . 0x3F	Start value for CRC calculation

Table 16: CRC start value for data channel 1

DLEN2	Addr. 0x42 (SPI); bit 5:0 R/W 0 Addr. 0x62 (BiSS); bit 5:0 R/W 0
0x00 ... 0x3F	1 bit (DLEN2 + 1) bit 64 bit
Notes	If DLEN2 < 8, a CRC must be enabled (CPOLY2 > 0).

Table 17: Data length channel 2

ENDC2	Addr. 0x42 (SPI); bit 6 R/W 0 Addr. 0x62 (BiSS); bit 6 R/W 0
0	Data channel 2 disabled: data channel length 0 bit
1	Data channel 2 enabled (condition: ENDC1 = 1)

Table 18: Enable data channel 2

CPOLY2	Addr. 0x43 (SPI); bit 1:0 R/W 0 Addr. 0x63 (BiSS); bit 1:0 R/W 0
0x0	no CRC2 generated (0 bit CRC)
0x1	CRC2 polynomial = 0x25 (5 bit CRC)
0x2	CRC2 polynomial = 0x43 (6 bit CRC)
0x3	CRC2 polynomial = 0x190D9 (16 bit CRC)

Table 19: CRC polynomial data channel 2

CSTART2	Addr. 0x43 (SPI); bit 7:2 R/W 0 Addr. 0x63 (BiSS); bit 7:2 R/W 0
0x00 . . . 0x3F	Start value for CRC calculation

Table 20: CRC start value for data channel 2

The (automatic) BiSS timeout adaption (refer to www.biss-interface.com) is based on the BiSS MA clock period T_{MA} and the device specific internal sampling frequency $1/T_{CLK}$.

The iC-MCB measures the 1.5 periods (from the first falling to the second rising edge) of MA each frame and calculates an adaptive timeout with $T_{CLK} = \frac{1.33}{f_{OSC}}$ (see El. Char. 225).

Symbol	**Condition**	**Min.**	**Max.**
timeout	$T_{CLK} \leq 1.5 * T_{MA}$	$1.5 * T_{MA}$	$1.5 * T_{MA} + 3.0 * T_{CLK}$
	$T_{CLK} \geq 1.5 * T_{MA}$	$1.0 * T_{CLK}$	$1.5 * T_{MA} + 3.0 * T_{CLK}$

Table 21: Adaptive BiSS timeout

Parameters NTOA and TOS (described in chapter FIELD INTERFACE: SSI) may be considered to enable a constant long BiSS timeout (approx. 20 µs) or constant short BiSS timeout (approx. 2 µs) as well.

BiSS Control Data Frame

The iC-MCB manages a dedicated set of BiSS commands and registers automatically. The number of occupied slave IDs is equal to the number of enabled data channels, but can be increased by one using ASID.

If CFGOK is not set or if the SSI protocol is enabled, the control frame will be executed without evaluating the slave ID. A register overview is shown in Table 22.

Addr. [2]	Name	Size	Managed by
0x00 ... 0x3F	Register bank	64 bytes	Host
0x40	Bank selection	0..8 bits (1 byte)	Host
0x41	EDS bank	0..8 bits (1 byte)	Host
0x42 ... 0x43	Profile ID	16 bits (2 bytes)	Host
0x44 ... 0x47	Serial number	32 bits (4 bytes)	Host
0x48 ... 0x5F	Slave register	24 bytes	Host
0x60 ... 0x6F [1]	Config RAM	16 bytes	iC-MCB
0x70 ... 0x77	Slave register	8 bytes	Host
0x78 ... 0x7D	Device ID	48 bits (6 bytes)	Host
0x7E ... 0x7F	Manufacturer ID	16 bits (2 bytes)	Host

Notes:

[1] Access to the Config RAM via BiSS is completely managed by iC-MCB. All other registers can only be accessed via BiSS, if implemented by the Host MCU as described in chapter BiSS Control Communication.

[2] Further hints and requirements for BiSS C slave register implementations are available in the BiSS C Protocol Description.

Table 22: BiSS Register Assignment

ASID	Addr. 0x45 (SPI); bit 3 R/W 0 Addr. 0x65 (BiSS); bit 3 R/W 0
0	Additional slave ID deactivated. The number of occupied slave IDs is • 0, if ENDC1 = 0, ENDC2 = 0) • 1, if ENDC1 = 1, ENDC2 = 0) • 2, if ENDC1 = 1, ENDC2 = 1)
1	Additional slave ID activated. The number of occupied slave IDs is • 1, if ENDC1 = 0, ENDC2 = 0) • 2, if ENDC1 = 1, ENDC2 = 0) • 3, if ENDC1 = 1, ENDC2 = 1)

Table 23: Activate additional Slave ID

The BiSS commands with the codes 0 and 1 are managed by iC-MCB, but they can be disabled per configuration bit CMD01DI.

CMD01DI	Addr. 0x45 (SPI); bit 4 R/W 0 Addr. 0x65 (BiSS); bit 4 R/W 0
0	Enable BiSS commands 0 and 1
1	Disable BiSS commands 0 and 1

Table 24: BiSS Command 0/1 Control

Parameter CMD2EN configures if the BiSS command with opcode 2 is managed by iC-MCB or by the host. In iC-MCB the command opcode 2 is used to switch the signal level at I/O crossbar pin BK, e.g. to control a bus coupler. CMD2EN enables pin BK at the I/O crossbar with respect to the priority shown in Table 67.

CMD2EN	Addr. 0x45 (SPI); bit 5 R/W 0 Addr. 0x65 (BiSS); bit 5 R/W 0
0	BiSS command 2 managed by host
1	BiSS command 2 enabled (control BK at IOx)

Table 25: BiSS Command 2 Control

For access to iC-MCB's Config RAM via BiSS register addresses 0x60 to 0x6F are used. The access is denied, if REGPROT is set.

REGPROT	Addr. 0x45 (SPI); bit 0 R/W 0 Addr. 0x65 (BiSS); bit 0 R/W 0
0	BiSS access to iC-MCB's Config RAM allowed
1	BiSS access to iC-MCB's Config RAM denied
Notes	It is recommended to set REGPROT = 1 before setting CFGOK = 1, if the host interface is used.

Table 26: Register protection

All BiSS commands and register accesses that are not managed by iC-MCB have to be managed by the host as described in chapter BiSS Control Communication on page chapter 22ff.

FIELD INTERFACE: SSI

Note the hints in chapter DESIGN REVIEW: Notes On Chip Functions.

The interface uses the SSI protocol when ENSSI is set.

ENSSI	Addr. 0x45 (SPI); bit 6 R/W 0 Addr. 0x65 (BiSS); bit 6 R/W 0
0	BiSS C protocol
1	SSI protocol
Notes	For operation in SSI mode, set USDST = 1.

Table 27: Protocol selection

The SSI frame

The SSI frame is used to transmit process data from a sensor to a master. The process data is contained in logical data channels. Each data channel has a programmable data length (DLEN1, DLEN2) and CRC to increase the transmission safety. The generator polynomial (CPOLY1, CPOLY2) and the start value for CRC calculation (CSTART1, CSTART2) is programmable too. ENDC1 and ENDC2 enable the corresponding data channel. As the SSI protocol does not support the delayed transmission of sensor data, the data must already be stored in the RAM when the SSI frame starts (ACQMODE = 0, BANKSW = 1, USDST = 1). The banks are automatically switched after writing into the data RAM with the SPI command Transmit SDAD. Fig. 6 shows the active RAM bank with BANKSEL indicating the currently selected bank.

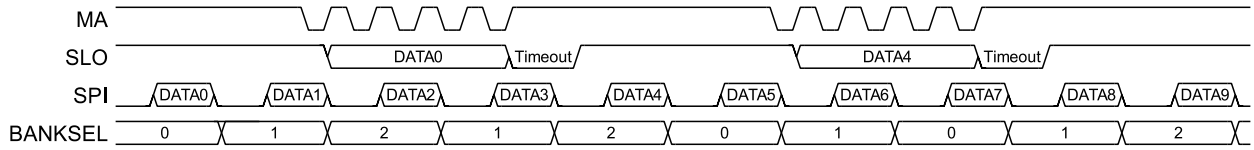


Figure 6: SSI frame

Serial timeout

For SSI operation the adaptive timeout is not recommended. A fixed timeout is enabled with NTOA with a length selected by TOS.

NTOA	Addr. 0x45 (SPI); bit 1 R/W 0 Addr. 0x65 (BiSS); bit 1 R/W 0
0	Adaptive timeout enabled (TOS configuration not relevant)
1	Adaptive timeout disabled (TOS configuration relevant)

Table 28: Adaptive timeout

TOS	Addr. 0x45 (SPI); bit 2 R/W 0 Addr. 0x65 (BiSS); bit 2 R/W 0
0	Long timeout (approx. 20 µs)
1	Short timeout (approx. 2 µs)

Table 29: Serial timeout

The fixed short or long timeout can also be used with the BiSS protocol.

Data format

A binary-to-Gray conversion can be enabled with GRAY1. With the SSI protocol two channels can be configured in iC-MCB to separate Gray-coded content in data channel 1 and following non-Gray-coded content in data channel 2. If the data contains additional SSI data bits which shall not be converted to Gray-code, those additional bits can be placed in data channel 2.

GRAY1	Addr. 0x40 (SPI); bit 7 R/W 0 Addr. 0x60 (BiSS); bit 7 R/W 0
0	No data conversion
1	Binary-to-Gray conversion

Table 30: SSI data format

Ring operation

The ring operation, which is selected with RSSI, defines a ring buffer with the data channel 1. In ring operation the data channel 2 can be used to define one or more bits, e.g. one stop bit, to separate the repetition.

RSSI	Addr. 0x45 (SPI); bit 7 R/W 0 Addr. 0x65 (BiSS); bit 7 R/W 0
0	Ring operation disabled
1	Ring operation enabled
Notes	For ring operation at least three Data RAM bytes need to be used (DLEN1 ≥ 8, ENDC1 = 1 and ENDC2 = 1 or DLEN1 ≥ 16 and ENDC1 = 1).

Table 31: Ring operation

HOST INTERFACE: SPI SLAVE

SPI Signals

Signal	Description
SPI Slave Signals	
NCS	Not chip select Input
SCLK	SPI clock Input
MOSI	SPI data Input
MISO	SPI data Output, if NCS = 0 High impedance, if NCS = 1
Optional Signals	
IRQ	Interrupt Output (if enabled with CB_IRQ)

Table 32: SPI Slave Signals

SPI Frame

Each SPI frame starts with one byte OPCODE sent from the host via MOSI and one byte STATUS sent from iC-MCB via MISO.

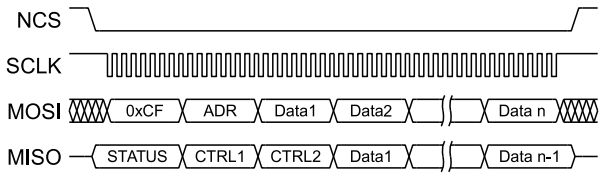


Figure 7: SPI frame example with OPCODE(0xCF), STATUS, CTRL1 and CTRL2

SPI Modes

The iC-MCB uses 8 bit wide SPI with phase and polarity = 0, or phase and polarity = 1.

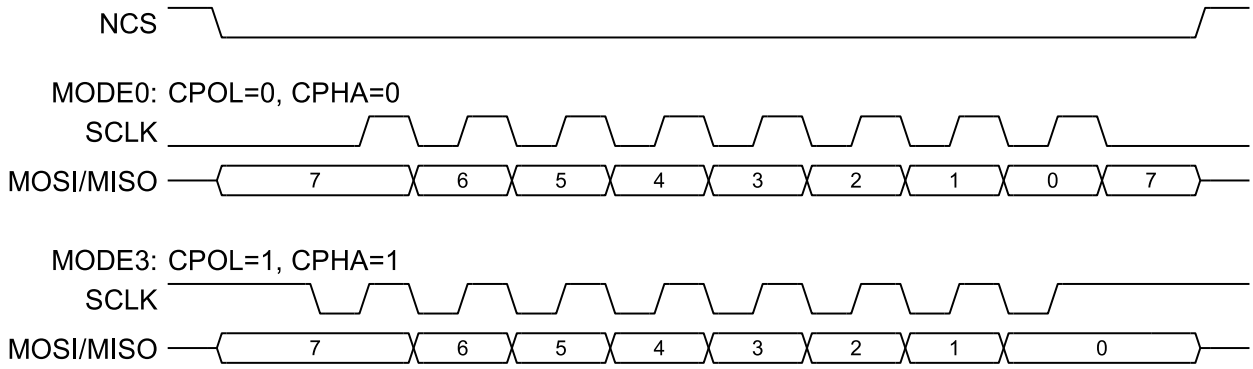


Figure 8: SPI: timing, phase and polarity

SPI Registers

The host uses the SPI interface to configure iC-MCB at startup and to write sensor data to iC-MCB.

Table 33 shows the register assignment for the SPI access.

Addr.	Name	Size	Access Level
0x00 .. 0x3F	Data RAM	64 bytes	R/W
0x40 .. 0x4F	Config RAM	16 bytes	R/W

Table 33: Table of register assignment

SPI Opcodes

The following opcodes are available.

OPCODE	
Code	Description
0xA6	Transmit SDAD
0x81	Read Register
0xCF	Write Register
0xE3	Sensor Feedthrough

Table 34: SPI Opcodes

All bytes after the first STATUS byte sent from iC-MCB via MISO depend on the SPI OPCODE and may contain additional BiSS Control Communication Data CTRL1 and CTRL2 or related device data.

SPI Opcode: Transmit SDAD

To transmit sensor data to iC-MCB the SPI OPCODE 0xA6 is used. Following the opcode the Single-Cycle Data (SCDATA) is read from the Data RAM starting at address 0x00 as shown in 9.

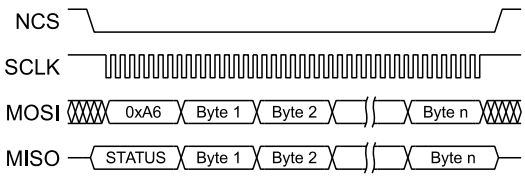


Figure 9: SPI: sensor data access (SDAD)

Within the Data RAM the SCDATA is arranged big-endian, i.e. with the highest-value byte at the lowest-value address. The MSB of data channel 1 is at address 0x00 and the LSB is always at bit position zero. The data for channel 2 starts at the next higher address following the memory area of data channel 1. The maximum data length is 8 byte per channel. Table 35 shows an example of data arrangement with 14 bit SCDATA length for channel 1 and 27 bit SCDATA2 length for channel 2 in the Data RAM. An access to the Data RAM during the BiSS frame is permitted, if it is partitioned into multiple banks using BANKSW. Only as many bytes as configured with DLEN1 and DLEN2 may be input during SPI access.

SDAD access to the configuration RAM (0x40 ... 0x4F) results in an SPI_ERR which will be sent in the STATUS during the next SPI frame.

Data RAM								
Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data Channel 1								
0x00	-	-	SCDATA1(13:8)					
0x01	SCDATA1(7:0)							
Data Channel 2								
0x02	-	-	-	-	-	SCDATA2(26:24)		
0x03	SCDATA2(23:16)							
0x04	SCDATA2(15:8)							
0x05	SCDATA2(7:0)							
0x06 ...0x3F	Unused, if no slave connected to SLI. Otherwise temporary buffer for data received at SLI.							

Table 35: Example for Data RAM assignment (BANKSW = 0)

SPI Opcode: Read Register

To read iC-MCB's registers the OPCODE 0x81 is sent via MOSI and followed by the address of the desired register. After the STATUS byte iC-MCB sends two additional control bytes CTRL1 and CTRL2 via MISO. The requested register data is sent in byte 4. Multiple consecutive bytes can be read during one read access. The register data stream on MISO is then extended and the address is incremented by one automatically.

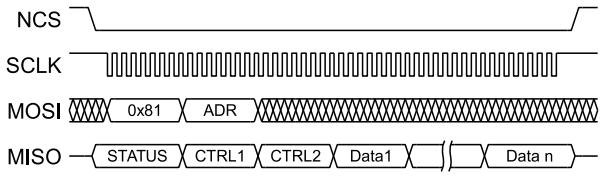


Figure 10: SPI: read register

SPI Opcode: Write Register

To write iC-MCB's registers the OPCODE 0xCF is sent followed by the address and the desired content of one or multiple consecutive registers via MOSI. After the STATUS byte iC-MCB sends two additional control bytes CTRL1 and CTRL2 via MISO. The transmitted register data is returned beginning in byte 4.

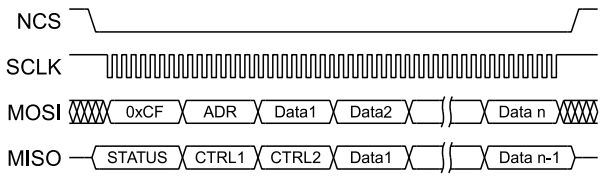


Figure 11: SPI: write register

Register access to an address above 0x4F results in an SPI_ERR which will be sent in the STATUS during the next SPI frame.

SPI Opcode: Sensor Feedthrough

To configure an SPI slave sensor that is connected to the Fast Sensor Interface the iC-MCB permits a Sensor Feedthrough to enable a direct communication between the host and a sensor. This connection to the fast sensor interface is enabled by the leading OP-CODE 0xE3. The lines NCS, SCLK, MOSI and MISO are connected to the IOs after evaluating the opcode.

If a BiSS request occurs while a Sensor Feedthrough operation is running, the data sent via BiSS is zero.

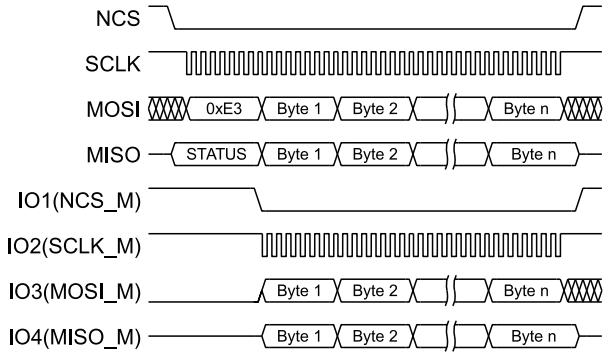


Figure 12: SPI: Sensor Feedthrough

SPI Status Byte

STATUS								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SPI_ERR	NCS_ERR	IRQ	STB	CTO(3:2)		PACTIVE(1:0)	

Table 36: STATUS Byte (returned during SPI access)

The PACTIVE status indicates the host that BiSS commands have activated or deactivated individual BiSS data channels. If data channels 1 and 2 are disabled by the Host MCU (ENDC1=0 or ENDC2=0) then the corresponding PACTIVE bit remains zero.

PACTIVE	STATUS; bit 1:0	R
0x0	All BiSS data channel deactivated	
0x1	BiSS data channel 1 activated	
0x2	BiSS data channel 2 activated	
0x3	BiSS data channel 1 + 2 activated	

Table 37: Process data channels activated/deactivated by BiSS Commands

A running BiSS Control Communication is indicated with CTO ≠ 0. It should be read every BiSS frame.

CTO	STATUS; bit 3:2	R
0x0	No BiSS Control Communication running	
0x1	BiSS Command	
0x2	BiSS Read register access	
0x3	BiSS Write register access	

Table 38: BiSS Control Communication

With STB iC-MCB indicates that the host has to confirm the execution of a pending Register Access or BiSS Command.

STB	STATUS; bit 4	R
0	No action pending	
1	Register access or command execution must be confirmed by host	

Table 39: Strobe for BiSS Control Communication

Bit IRQ signals an active interrupt request. Its value can also be output at the I/O crossbar, if enabled. Details are available in chapter I/O CROSSBAR on page 44.

IRQ	STATUS; bit 5	R
0	No interrupt request	
1	Interrupt request active	

Table 40: Interrupt request line/signal

If the pulse on the chip select line NCS is too short, an error is indicated with NCS_ERR.

NCS_ERR	STATUS; bit 6	R
0	No NCS error	
1	NCS pulse too short. Last SPI access not finished.	

Table 41: Frame separation error

An SPI error is indicated with SPI_ERR.

SPI_ERR	STATUS; bit 7	R
0	No SPI error	
1	SPI error detected. Possible reasons are: · Invalid SPI OPCODE · Register access to an address which is not implemented	

Table 42: SPI Error

BiSS Control Communication

BiSS enables two types of control communication:

- BiSS Register Communication
  - BiSS Read Register Access
  - BiSS Write Register Access
- BiSS Commands

The basics of the BiSS control communication (BiSS Commands and Register Communication) are managed by iC-MCB. This includes receiving CDM, sending CDS, Slave ID assignment, addressing, processing time request and CRC calculation. iC-MCB manages all accesses to all BiSS registers 0x60...0x6F completely. The host has to support the iC-MCB in some BiSS commands (see CMD2EN) and all register accesses except of BiSS registers 0x60...0x6F. To this end STATUS, CTRL1 and CTRL2 are sent by iC-MCB on MISO during a SPI register access.

iC-MCB sends its information for the BiSS Control Communication via STATUS, CTRL1 and CTRL2 while the host manages the BiSS Control Communication via SPI using parameters RDATA, CVALID, CONFIRM and IVALID in register addresses 0x4E and 0x4F.

BiSS Control Bytes

While the STATUS indicates the host an ongoing control communication with CTO during every SPI opcode, control bytes CTRL1 and CTRL2 are only sent during SPI opcodes Read Register and Write Register. CTRL1 and CTRL2 provide the requested register address ADR and slave ID SIDDC during a BiSS register access (CTO > 1) or the requested slave IDs IDSDC and BiSS command CMD / BROADC during a BiSS Command frame (CTO = 1).

CTRL1								
Cond.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTO = 0	0	0	0	0	0	0	0	0
CTO = 1	IDSDC(7:0)							
CTO > 1	0	ADR(6:0)						

Table 43: Control word 1 (returned during SPI register access for processing of BiSS Control Communication)

CTRL2								
Cond.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTO = 0	0	0	0	0	0	0	0	0
CTO = 1	0	0	0	0	0	BROADC	CMD(1:0)	
CTO > 1	0	0	0	0	0	SIDDC(2:0)		

Table 44: Control word 2 (returned during SPI register access for processing of BiSS Control Communication)

BiSS Access Validation
During every BiSS control communication control bytes CTRL1 and CTRL2 have to be evaluated by the host to validate or deny access to the register(s) requested by the BiSS master or validate or deny the transmitted BiSS command. Access is validated with CVALID.

CVALID	Addr. 0x4F (SPI);	bit 2:0	R/W 0
	Addr. 0x6F (BiSS);	bit 2:0	R/W 0

Code	Description
0x0	Address or opcode not valid (Deny register access or opcode execution.)
0x1	Current address for BiSS Read Register Access is valid
0x2	Current address for BiSS Write Register Access is valid
0x3	Current address for BiSS Read Register Access and BiSS Write Register Access request is valid
0x4	BiSS Command CMD is valid
0x5	Confirming RDATA was read/ written or BiSS Command execution was successful
0x6	Current and next address for BiSS Write Register Access request are valid
0x7	Current address for BiSS Read Register Access request is valid. Additionally, current and next address for BiSS Write Register Access requests are valid

Table 45: Control valid indication

For processing of BiSS register accesses the host has to inform iC-MCB about the access level of the current register (ADR) and the next register (ADR+1) during each control state CSTATE = AdrValid. The BiSS master can access a single register or several registers sequentially, if enabled by the host with CVALID as described in Table 46. Details about single and sequential register accesses are available in the BiSS C Protocol Description.

Validating BiSS Register Accesses		
Access Level of		**Recommended host reaction during CSTATE = AdrValid**
ADR	**ADR+1**	
NA	-	Deny access to current address (ADR) with CVALID = 0x0.
R	-	Enable read access to the current register address (ADR) with CVALID = 0x1. Sequential read access is enabled by repetitively enabling access to the current register address (ADR) with CVALID = 0x1 as shown in Figure 14.
W	W	Enable sequential write access to the current (ADR) and next register address (ADR+1) with CVALID = 0x6 a shown in Figure 15.
	¬ W	Enable write access to the current register address (ADR) with CVALID = 0x2.
R/W	W	Enable read access to the current register address (ADR) and enable sequential write access to the current (ADR) and next register address (ADR+1) with CVALID = 0x7.
	¬ W	Enable read and write access to the current register address (ADR) with CVALID = 0x3.

Notes:
"NA": No access to register allowed
"-": "Don't care"
"R": Read access to register allowed
"W": Write access to register allowed
"¬ W": No write access to register allowed
"R/W": Read and write access to register allowed

Table 46: Validation of BiSS Register Accesses (CTO > 1) with CVALID during CSTATE=AdrValid.

BiSS Read Register Access

The register read access starts with CTO = 0x2. Within the next four BiSS frames the host must read CTRL1 and CTRL2, which contain the register address ADR and the mapped slave ID for BiSS Register Access SIDDC, and must determine if the address is valid for access with CVALID. iC-MCB automatically maps the received slave ID to the enabled data channels ENDC1, ENDC2 and ASID as shown in Figure 13. The mapped BiSS Slave ID for BiSS register accesses SIDDC is sent via MISO within the CTRL1 byte.

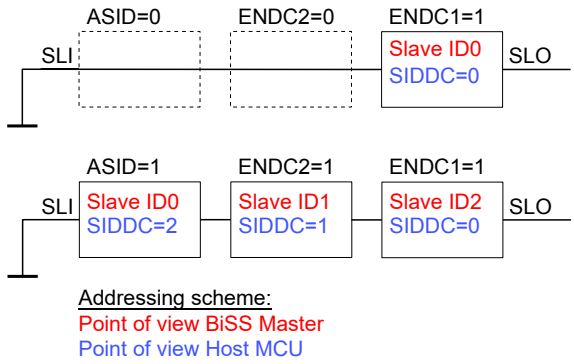


Figure 13: Data channel and ID arrangement

If reading of the current address is allowed, the host sets CVALID = 0x1 (Refer to Table 46 for further options). At the BiSS Interface iC-MCB then sets bits 'RW'=0b10 according to the BiSS C Protocol Description. With STB = 1 the register data should be written to RDATA and confirmed with CVALID = 0x5. This can be done in a single SPI Write Register operation. For a sequential BiSS Read Register Access (reading multiple registers within one control frame) the host increments the register address internally and repeats the same procedure for the next bytes as shown in Figure 14. The BiSS Read Register Access is finished with CTO = 0x0 and the host sets CVALID = 0x0 to return to Idle state.

After confirming availability of register data with CVALID = 0x5, iC-MCB will be in CSTATE = AdrValid. ADR should be incremented internally in the host and verified with CVALID.

ADR	CTRL1; bit 6:0	R
0x00 ... 0x7F	BiSS slave register access address	

Table 47: BiSS register address

SIDDC	CTRL2; bit 2:0	R
0x0	DC1 is addressed (condition ENDC1 = 1)	
0x1	DC2 is addressed (condition ENDC2 = 1)	
0x2	NODC is addressed (condition ASID = 1)	
0x3	not used	
Note	DC1: Data Channel 1 DC2: Data Channel 2 NODC: Additional Slave ID activated with ASID	

Table 48: Slave ID for BiSS register access (mapped)

If the microcontroller is not able to validate access with CVALID within four BiSS frames, CVALID can be set in advance of a register access or BiSS Command (e.g. if the registers of a register bank all have the same access level) and CONFIRM is used to confirm STB.

CONFIRM	Addr. 0x4F (SPI); bit 4 Addr. 0x6F (BiSS); bit 4	R/W 0 R/W 0
0	CVALID used to validate access and confirm execution for BiSS Control Communication (see Figure 18).	
1	CVALID used to validate access and CONFIRM used to confirm execution for BiSS Control Communication (see Figure 19).	
Note	CONFIRM is not implemented before chip rev. Z.	

Table 49: Confirming BiSS Control Communication

The parameter RDATA in SPI register 0x4E is used for data exchange during both a BiSS Read Register Access and BiSS Write Register Access.

RDATA	Addr. 0x4E (SPI); bit 7:0 Addr. 0x6E (BiSS); bit 7:0	R/W 0 R/W 0
0x00 ... 0xFF	Any data value for register access	

Table 50: Register access transfer byte

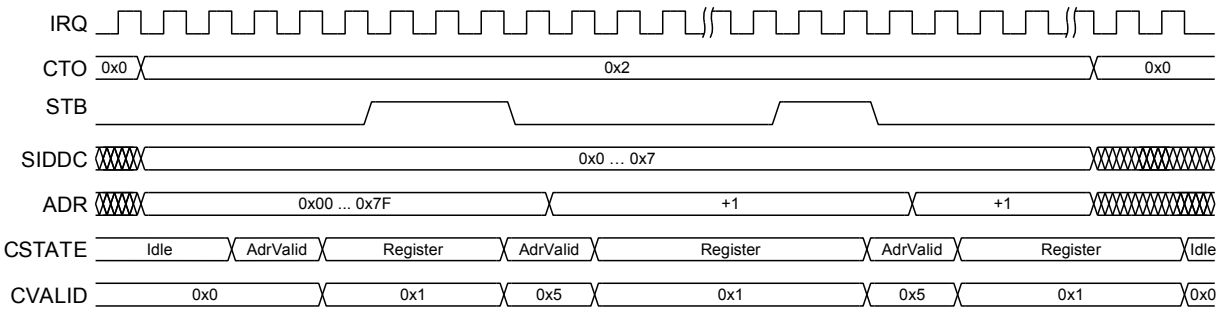


Figure 14: Register read via BiSS

BiSS Write Register Access

The BiSS Write Register Access starts also with CTO = 0x2. Within the next four BiSS frames the host must read CTRL1 and CTRL2, which contain the register address ADR and the mapped slave ID for BiSS Write Access SIDDC, and must determine if the address can be written with CVALID. SIDDC is mapped to the internal ID range as shown in Figure 13.

If writing of the current address is allowed, the host sets CVALID = 0x2 enabling a write access to a single register requested by the BiSS master. At the BiSS Interface iC-MCB then sets bits 'RW'=0b01 according to the BiSS C Protocol Description. If writing of the current and the next address is allowed, the host sets CVALID = 0x6 enabling a sequential register access by the BiSS master. At the BiSS Interface iC-MCB then also sets bits 'RW'=0b01 and continues the control frame with another start bit after successful write access according to the BiSS C Protocol Description. (Refer to Table 46 for further options).

After four BiSS frames CTO changes to 0x3. With STB = 1 the data has to be read from RDATA in SPI register 0x4E and must be confirmed with CVALID = 0x5 as shown in Figure 15. The confirmation procedure has to be completed within two SPI frames. For a sequential BiSS Write Register Access (reading multiple registers within one control frame) the host increments the register address internally and repeats the same procedure for the next bytes as shown in Figure 14. The BiSS Write Register Access is finished with CTO = 0x0 and the host sets CVALID = 0x0 to return to Idle state.

After confirming availability of register data with CVALID = 0x5, iC-MCB will be in CSTATE = AdrValid. ADR should be incremented internally in the host and verified with CVALID.

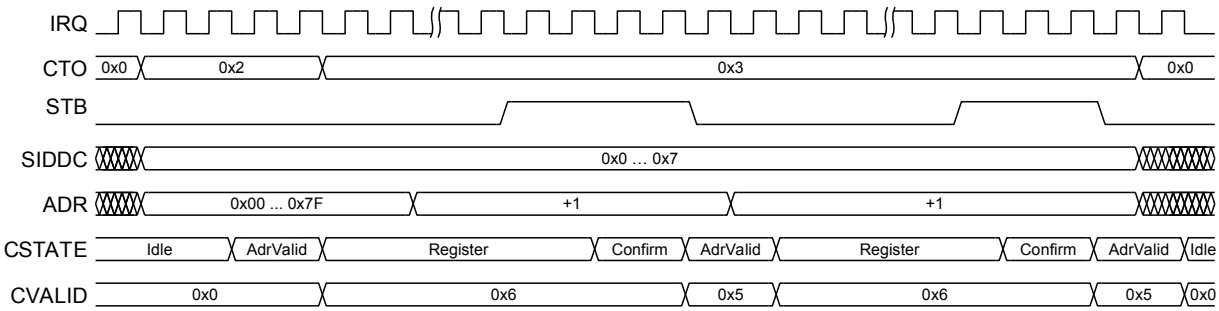


Figure 15: Register write via BiSS

BiSS Command Execution

The BiSS Command execution is indicated by iC-MCB with CTO = 0x1. Within the next four BiSS frames the host must read CTRL1 and CTRL2, which contain the mapped slave ID for BiSS Commands IDSDC, the BiSS Command CMD and the addressing BROADC, and must validate (set CVALID = 0x4) or deny (set CVALID = 0x0) the BiSS Command, if the command is host managed (see CMD2EN). If the microcontroller is not able to set CVALID within four BiSS frames, the parameter IVALID can be used to permit all commands independently of BiSS CMD, BROADC and IDSDC. When iC-MCB sets STB = 1 the BiSS Command CMD must be executed and confirmed with CVALID = 0x5 as shown in Figure 16. After confirmation the BiSS Command procedure is completed with CTO = 0x0 and the host sets CVALID = 0x0 to return to Idle state.

iC-MCB automatically maps the received slave ID IDSDC to the enabled data channels ENDC1, ENDC2 and ASID as specified for SIDDC and shown in Figure 13. The mapped BiSS Slave ID for BiSS commands IDSDC is sent via MISO within the CTRL2 byte. For example, if only one data channel is enabled (ENDC1 = 1, ENDC2 = 0 and ASID = 0 and iC-MCB is used in a Point-To-Point configuration, data channel 1 can be addressed with a BiSS Command via Slave ID = 0. If the iC-MCB is used in a bus configuration with one slave connected to SLI (Slave ID 0) and both data channels enabled (ENDC1 = 1, ENDC2 = 1 and ASID = 0), the data channel 1 can be addressed with a BiSS Command via the Slave ID 2 and data channel 2 via Slave ID 1. If the iC-MCB is used in a bus configuration with one slave connected to SLI (Slave ID 0), and both process data channels as well as the additional Slave ID enabled (ENDC1 = 1, ENDC2 = 1 and ASID = 1), data channel 1 can be addressed via the Slave ID 3, data channel 2 via Slave ID 2 and the additional slave ID via Slave ID 1. In Table 51 the tokens DC1 and DC2 are used for addressing the single-cycle data channel 1 resp. 2 and NODC is used for the additional slave ID enabled with ASID.

IDSDC	CTRL1; bit 7:0	R
0x00	No data channel is addressed with the BiSS command CMD	
0x01	DC1 is addressed (condition: ENDC1 = 1)	
0x02	DC2 is addressed (condition: ENDC2 = 1)	
0x03	DC1 and DC2 are addressed (condition: ENDC1 = 1, ENDC2 = 1)	
0x04	NODC is addressed (condition: ASID = 1)	
0x05	DC1 and NODC are addressed (condition: ENDC1 = 1), ASID = 1)	
0x06	DC2 and NODC are addressed (condition: ENDC2 = 1), ASID = 1)	
0x07	DC1, DC2 and NODC are addressed (condition: ENDC1 = 1, ENDC2 = 1, ASID = 1))	
0x08 ... 0xFF	not used	
Note	DC1: Data Channel 1 DC2: Data Channel 2 NODC: Additional Slave ID activated with ASID	

Table 51: Slave ID for BiSS command (mapped)

CMD	CTRL2; bit 1:0	R
0x0 ... 0x3	BiSS Command	

Table 52: BiSS Command

BROADC	CTRL2; bit 2	R
0	BiSS Command is addressed	
1	BiSS Command is broadcast	

Table 53: Broadcast

IVALID	Addr. 0x4F (SPI); bit 3	R/W 0
	Addr. 0x6F (BiSS); bit 3	R/W 0
0	Validity of BiSS command CMD is set individually by CVALID	
1	All BiSS commands CMD are valid (see Figure 19).	
Note	IVALID is not implemented before chip rev. Z.	

Table 54: Validity of BiSS commands

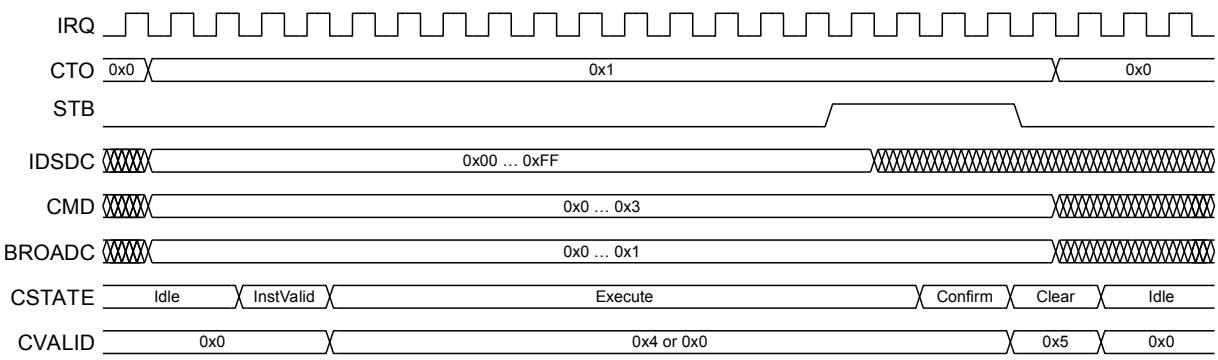


Figure 16: Command via BiSS

Microcontroller Program Flow

Figure 17 shows the flow of the controller program that needs to be implemented in the host to manage BiSS Command execution and access to the Host's registers via BiSS Control Communication. The flag **EOF** is used to enter the control frame sequence in Figure 18 at least every other frame. During each entry to the control frame sequence one condition (grey box) is checked, one MCU procedure (green box) is executed and the next control frame state (yellow box) is reached.

See Table 22 for details on which BiSS Commands and BiSS Register Accesses have to be managed by the host.

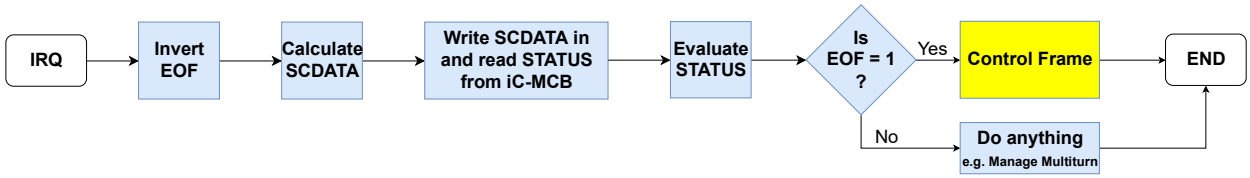


Figure 17: MCU program flow (example for ACQMODE = 1)

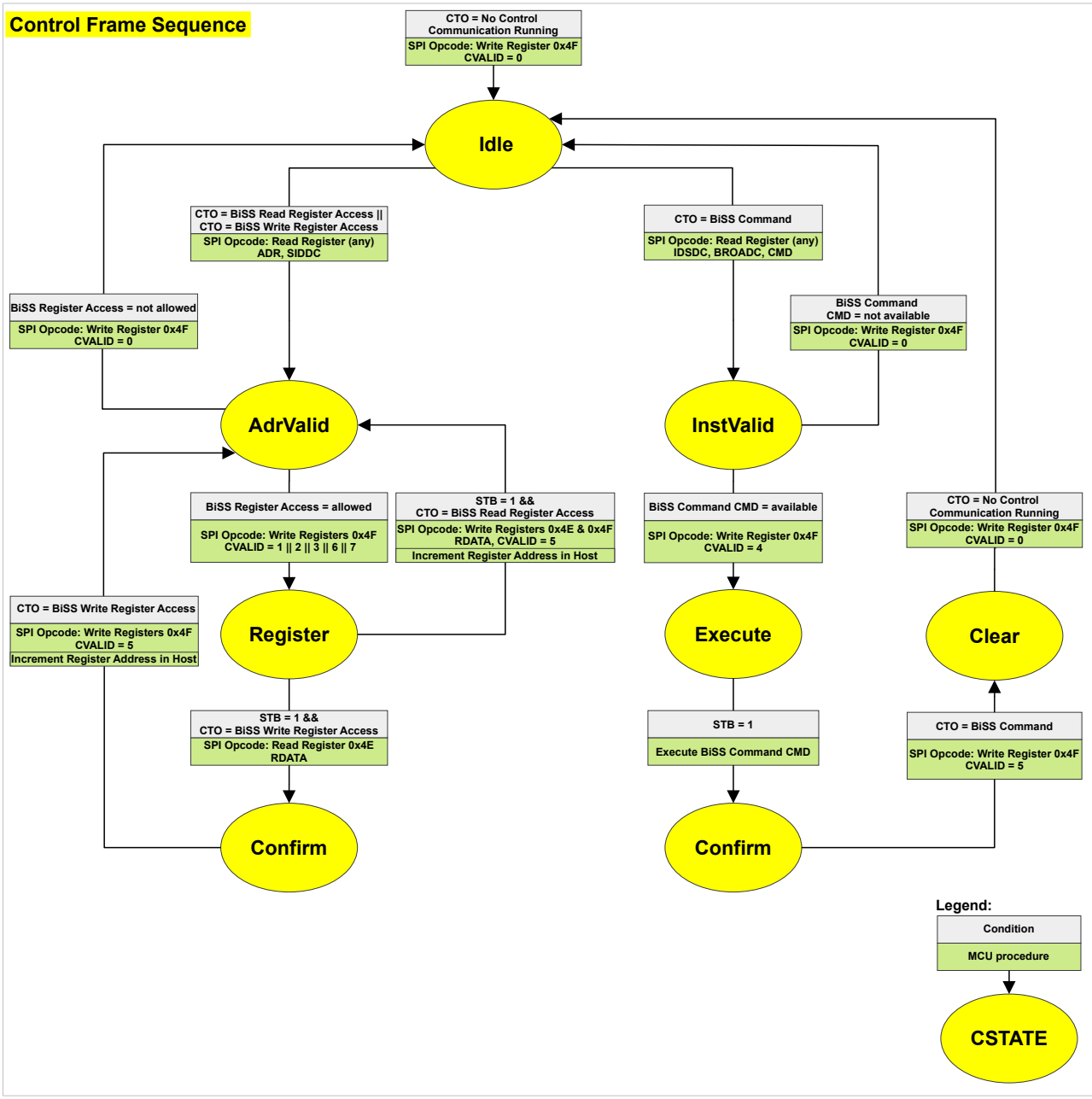


Figure 18: Microcontroller program flow for control frame sequence using CVALID.

As shown in Figure 18 CVALID is set several times to validate the register address or BiSS command and to confirm execution. In order to reduce the time critical access validation for the host, CVALID can be used to set the access level for the BiSS registers and IVALID can be used to set the access level for the BiSS commands. For instance, if the BiSS master selects a register bank with equal access level for all registers, CVALID can be set as soon as the bank is selected. The access to the registers is then validated or denied accordingly and the host only needs to confirm execution of the register access with CONFIRM. Similarly, host workload for access validation of BiSS commands can be reduced by setting IVALID = 1, if all BiSS commands are implemented. The host then only needs to confirm execution of the BiSS command. Figure 19 shows the MCU's programm flow when IVALID and CONFIRM are used.

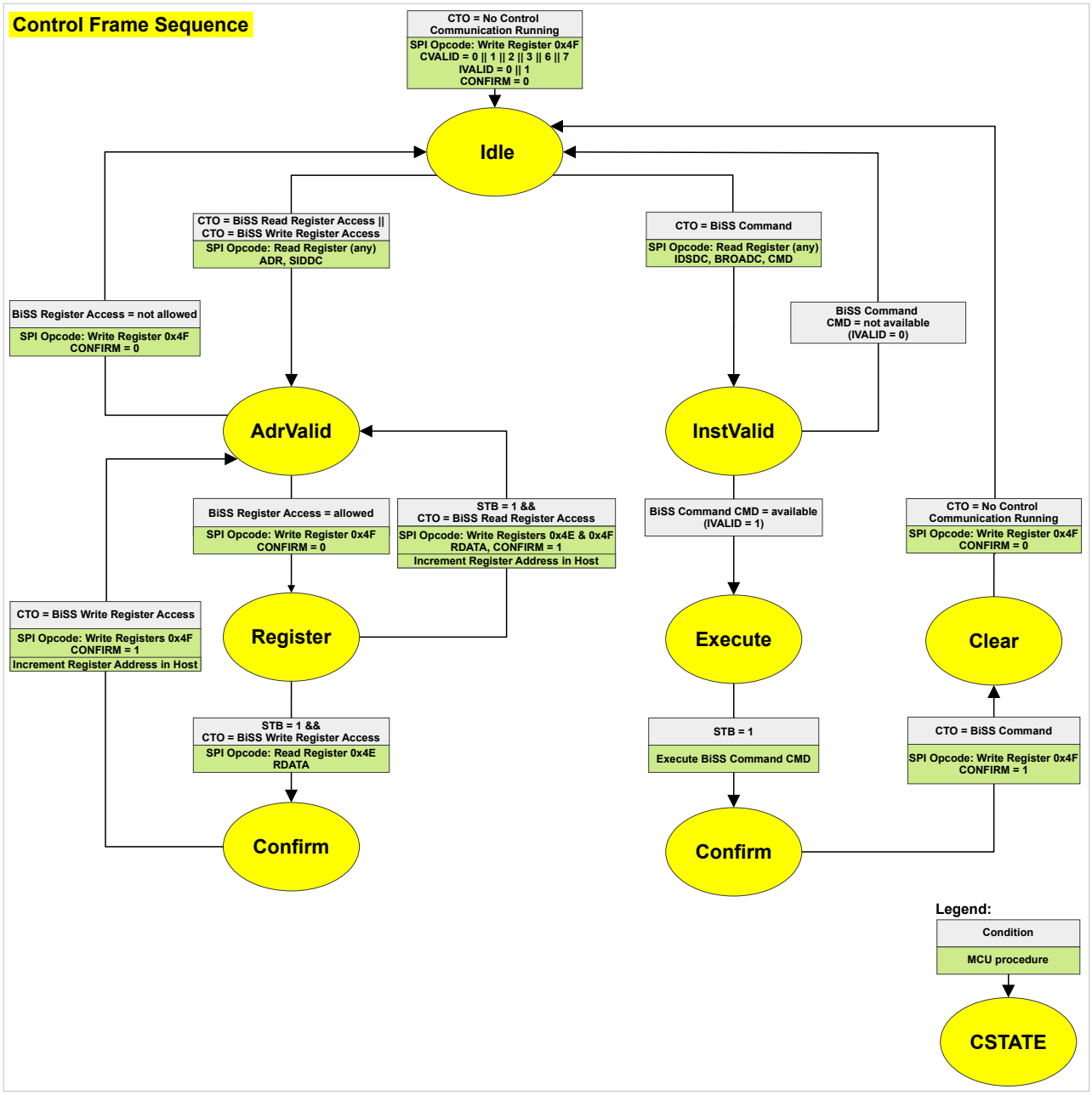


Figure 19: Microcontroller programm flow for control frame sequence using CONFIRM. CVALID and IVALID are set in advance for access validation.

FAST SENSOR INTERFACE: SPI MASTER

When ENFSI = 1 an external sensor can automatically be read in realtime without controller support via the Fast Sensor Interface at IO1 . . . IO4. The data received by the Fast Sensor Interface is assigned to data channel 1. The Fast Sensor Interface is used stand-alone (no sensor data is provided by via the HOST INTERFACE: SPI SLAVE) and requires ACQMODE = 0 and ENSSI = 0.

ENFSI	Addr. 0x47 (SPI);	bit 6	R/W 0
	Addr. 0x67 (BiSS);	bit 6	R/W 0
0	Fast Sensor interface disabled		
1	Fast Sensor interface enabled		
Notes	See Table 10 for application details.		

Table 55: Enable Fast Sensor Interface

Depending on the crossbar configuration parameter CB_FSI, at least the clock signal (SCLK_M) and a data signal (MISO_M or MOSI_M) are used. The SPI master clock frequency is configured with CLKDIV.

CLKDIV	Addr. 0x49 (SPI);	bit 7:4	R/W 0
	Addr. 0x69 (BiSS);	bit 7:4	R/W 0
	before chip release Z	from chip release Z	
0x0	1 (20 MHz)		
0x1	2 (10 MHz)		
0x2	4 (5 MHz)		
. . .	2*CLKDIV (3.33 MHz . . . 1.11 MHz)		
0xA	20 (1 MHz)		
0xB	22 (909 kHz)	24 (833 KHz)	
0xC	24 (833 kHz)	32 (625 KHz)	
0xD	26 (769 kHz)	40 (500 KHz)	
0xE	28 (714 kHz)	50 (400 KHz)	
0xF	30 (667 kHz)	64 (312.5 KHz)	

Table 56: SPI clock divider

Polarity CPOL and phase CPHA are configurable as shown in Figure 20 and 21.

CPOL	Addr. 0x49 (SPI);	bit 0	R/W 0
	Addr. 0x69 (BiSS);	bit 0	R/W 0
0	SPI polarity 0		
1	SPI polarity 1		

Table 57: SPI protocol polarity

CPHA	Addr. 0x49 (SPI);	bit 1	R/W 0
	Addr. 0x69 (BiSS);	bit 1	R/W 0
0	SPI phase 0		
1	SPI phase 1		

Table 58: SPI protocol phase

DLFSI defines the data length/ count of SCLK_M clock periods at the Fast Sensor Interface. The data received by the Fast Sensor Interface is always assigned to data channel 1 and stored in the Data RAM starting at address 0x00.

DLFSI	Addr. 0x47 (SPI);	bit 5:0	R/W 0
	Addr. 0x67 (BiSS);	bit 5:0	R/W 0
0x00	1 bit		
...	(DLFSI + 1) bit		
0x3F	64 bit		
Notes	The Fast Sensor Interface is assigned to data channel 1. DLEN1, CPOLY1, CSTART1, ENDC1 have to be considered.		

Table 59: Data length Fast Sensor Interface

HEADL determines the length of the header HEADER that is sent by the SPI Master.

HEADL	Addr. 0x48 (SPI);	bit 3:0	R/W 0
	Addr. 0x68 (BiSS);	bit 3:0	R/W 0
Code	Header Length (Bits)		
0x00	0 (Header not used)		
0x01	1 (HEADER(7))		
0x02	2 (HEADER(7:6))		
. . .			
0x08	8 (HEADER(7:0))		
0x09	9 (HEADER(7:0) & '0')		
. . .			
0x0F	15 (HEADER(7:0) & '000 0000')		

Table 60: SPI request header length

HEADER defines a command that is sent to the connected SPI Slave in order to request data.

HEADER	Addr. 0x4A (SPI);	bit 7:0	R/W 0
	Addr. 0x6A (BiSS);	bit 7:0	R/W 0
Code	Description		
0x00 . . . 0xFF	SPI Master header		

Table 61: SPI request header

With STAFSI=0x2 or 0x3 iC-MCB observes MISO_M and waits for a start bit. Therefore a delay of data availability (e.g. the SPI slave's processing time) can be considered and is indicated by the transmitted data.

STAFSI	Addr. 0x48 (SPI); bit 5:4 R/W 0 Addr. 0x68 (BiSS); bit 5:4 R/W 0
0x0	No start bit in sensor data
0x1	Reserved
0x2	Wait for high active start bit
0x3	Wait for low active start bit
Notes	If STAFSI=0x2 or 0x3, it must be ensured that a start bit is sent by the sensor.

Table 62: Observe start bit from sensor

IDLE determines the volate level at MOSI_M during idle as shown in Figure 21.

IDLE	Addr. 0x48 (SPI); bit 6 R/W 0 Addr. 0x68 (BiSS); bit 6 R/W 0
0	MOSI_M at low level during idle
1	MOSI_M at high level during idle

Table 63: Idle state at MOSI_M

The parameter G2B is used to convert gray coded sensor data into binary for BiSS transmission.

G2B	Addr. 0x49 (SPI); bit 3 R/W 0 Addr. 0x69 (BiSS); bit 3 R/W 0
0	No data conversion
1	Gray to binary conversion

Table 64: Gray to binary conversion for sensor data

The parameter OSCDIV2 = 1 does half the internal oscillator frequency f_{OSC} and affects all f_{OSC} related timings of iC-MCB.

OSCDIV2	Addr. 0x47 (SPI); bit 8 R/W 0 Addr. 0x67 (BiSS); bit 8 R/W 0
0	f_{OSC} divide by 2 disabled
1	f_{OSC} divide by 2 enabled
Note	OSCDIV2 is not implemented from chip revision Z.

Table 65: Oscillator Frequency divide by 2

In BiSS the sensor data is captured with the first rising edge at the clock signal MA ('Latch point'). The BiSS latch point is transferred to SCLK_M or to the additional chip select signal NCS_M using REQ_FT.

REQ_FT	Addr. 0x49 (SPI); bit 2 R/W 0 Addr. 0x69 (BiSS); bit 2 R/W 0
0	Feed forward to NCS_M
1	Feed forward to SCLK_M

Table 66: BiSS request Sensor Feedthrough

With REQ_FT = 0 the first falling edge of NCS_M matches with the BiSS latch point (first rising edge of MA).

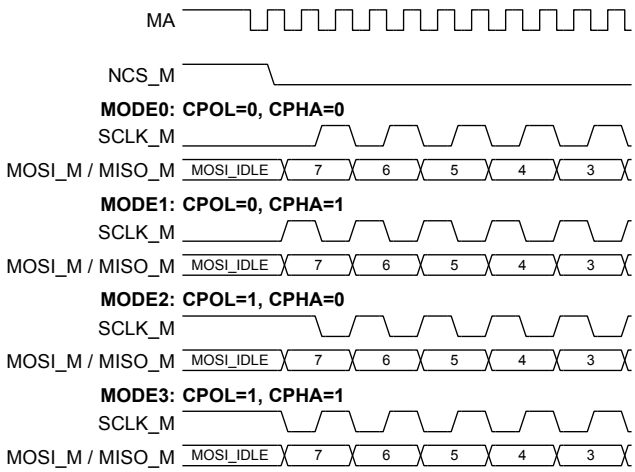


Figure 20: Fast Sensor Interface: phase and polarity (REQ_FT = 0)

With REQ_FT = 1 the first rising edge of SCLK_M matches with the BiSS latch point (first rising edge of MA).

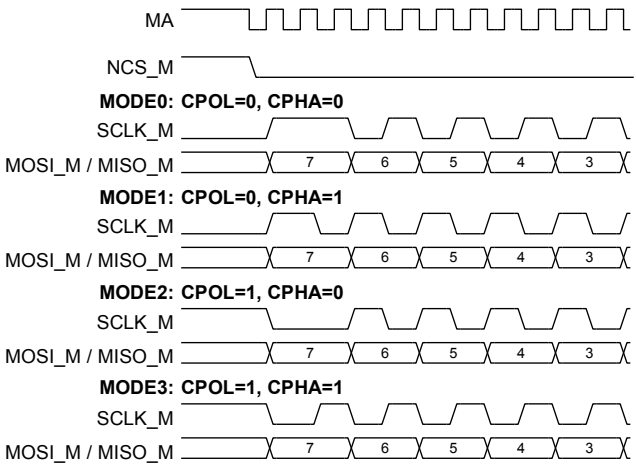


Figure 21: Fast Sensor Interface: phase and polarity (REQ_FT = 1)

I/O CROSSBAR

The I/O crossbar is used to map several functions to the six I/O pins. The mapping is created with a priority order, an enabled function uses the next unused I/O. The Table 67 shows the priority in descending order (Highest priority on top, lowest priority at the bottom). A (X) is used for a possible mapping and a (-) if the function cannot be mapped to the I/O.

I/O CROSSBAR

Function	Priority	Signals	IO1	IO2	IO3	IO4	IO5	IO6
Fast Sensor Interface (FSI) / SPI Master	1	SCLK_M	X	-	-	-	-	-
		MOSI_M	-	X	-	-	-	-
		MISO_M	-	X	X	-	-	-
		NCS_M	-	-	X	X	-	-
External Oscillator Clock Input	2	CLK	X	-	X	X	X	X
Interrupt Request Output	3	IRQ	X	X	X	X	X	X
BiSS Clock Output (Delayed)	4	MAO	-	X	X	X	X	X
BiSS Slave Data Input (from previous slave)	5	SLI	-	-	X	X	X	X
Bus Coupler Control Output	6	BK	-	-	-	X	X	X
BiSS Slave Data Output (to following slave)	7	SLO_O	-	-	-	-	X	X
BiSS Slave Data Input (from following slave)	8	SLO_I	-	-	-	-	-	X

Examples:
(1) If CB_FSI=0x0, CB_CLK=1 and CB_IRQ=1, then CLK will be mapped to IO1 and IRQ to IO2.
(2) If CB_FSI=0x3 and CB_IRQ=1, then SCLK_M will be mapped to IO1, MISO_M to IO2 and IRQ to IO3.

Table 67: Possible mappings to IOx ports

Fast Sensor Interface (FSI) / SPI Master

iC-MCB provides a Fast Sensor Interface (FSI). It can be used to automatically read out data from sensors (e.g. SPI sensors). CB_FSI is used to map the signals to the IOs according to the connected sensor. The FSI is configured as described in FAST SENSOR INTERFACE: SPI MASTER.

CB_FSI	Addr. 0x4C (SPI); bit 2:0 R/W 0 Addr. 0x6C (BiSS); bit 2:0 R/W 0
0x0	Fast Sensor interface not used
0x1	SCLK_M, MOSI_M and MISO_M used (IO1...IO3)
0x2	SCLK_M and MOSI_M used (IO1...IO2)
0x3	SCLK_M and MISO_M used (IO1...IO2)
0x4	Reserved
0x5	SCLK_M, MOSI_M, MISO_M and NCS_M used (IO1...IO4)
0x6	SCLK_M, MOSI_M and NCS_M used (IO1...IO3)
0x7	SCLK_M, MISO_M and NCS_M used (IO1...IO3)
Notes	CB_FSI maps the Fast Sensor Interface to the I/O pins. It is enabled by ENFSI.

Table 68: Configuration Fast Sensor Interface

External Oscillator Clock Input

iC-MCB implements an internal oscillator (see El.Char. f_{OSC}). CB_CLK can be enabled to use an external oscillator clock signal instead.

CB_CLK	Addr. 0x4C (SPI); bit 3 R/W 0 Addr. 0x6C (BiSS); bit 3 R/W 0
0	Internal oscillator clock used (El.Char. 401: f_{osc}).
1	External oscillator clock input connected to next unused I/O (El.Char. 402: f_{osc_in}).

Table 69: External oscillator clock input

Interrupt Request Output

With CB_IRQ an interrupt request output (IRQ) signal is enabled at the I/O crossbar. The IRQ signal level is high as soon as the BiSS/SSI frame begins and goes low after the timeout is terminated as shown in Figure 5. The IRQ signal level is also available in the STATUS byte (refer to bit IRQ).

CB_IRQ	Addr. 0x4C (SPI); bit 4 R/W 0 Addr. 0x6C (BiSS); bit 4 R/W 0
0	IRQ output not used
1	IRQ output connected to next unused I/O

Table 70: Interrupt request output

BiSS Clock Output (Delayed)
If several BiSS slaves are daisy-chained in a bus structure, the timing of the clock signal MA must match the timing of the data input signal SLI at the following slave to ensure proper data processing, particularly at high speed communication. To this end, the BiSS clock input MA is delayed with respect to iC-MCB's propagation delay (refer to El.Char 223 (t_P)). The delayed clock signal MAO is output at the I/O crossbar, if enabled by CB_MAO.

CB_MAO	Addr. 0x4C (SPI); bit 5 R/W 0 Addr. 0x6C (BiSS); bit 5 R/W 0
0	MAO not used
1	MAO connected to next unused I/O

Table 71: BiSS clock output MA

BiSS Slave Data Input (from previous slave)
In order to implement BiSS bus structure capability, the BiSS data input signal can be enabled using CB_SLI. It is recommended to implement an RS422 transceiver for the data input signal and the clock output signal.

CB_SLI	Addr. 0x4C (SPI); bit 6 R/W 0 Addr. 0x6C (BiSS); bit 6 R/W 0
0	SLI internally connected to '0'
1	SLI connected to next unused I/O

Table 72: BiSS data input SLI

BiSS Coupler Control Output
Pin BK can control an external bus coupler for enabling or disabling/terminating BiSS daisy chain (bus) structures. The function is assigned to the I/O crossbar with respect to the priorities shown in Table 67, if CMD2EN=1. The voltage at pin BK is then switched between high and low level, if an addressed or broadcasted BiSS Command 2 is sent by the BiSS master.

BiSS Slave Data Input/Output (from/to following slave)
In order to implement further BiSS sensors within the same device and connect them in a daisy chain structure with iC-MCB, a BiSS Slave Data Output signal SLO_O and a BiSS Slave Data Input signal SLO_I can be enabled using CB_SLO. iC-MCB's single-ended BiSS data output signal is transmitted to the following slave(s) via SLO_O. The following slave(s) return their single-ended data to iC-MCB via SLO_I and iC-MCB transmits the BiSS stream of the daisy chain as a differential signal via its RS422 transceivers.

CB_SLO	Addr. 0x4C (SPI); bit 7 R/W 0 Addr. 0x6C (BiSS); bit 7 R/W 0
0	SLO_O and SLO_I internally connected
1	SLO_O and SLO_I connected to next unused IOs

Table 73: BiSS data output SLO

DESIGN REVIEW: Notes On Chip Functions

iC-MCB 3		
No.	Function, Parameter/Code	Description and Application Notes
1	USDST, IVALID, CONFIRM	Not available in chip revision 3.
2	BUSY, CLKDIV	Coding changed as of chip revision Z.
3	OSCDIV2	Not available as of chip revision Z.
4	OPERATING REQUIREMENTS: Field Interface BiSS/SSI	At the end of a BiSS/SSI frame a minimum wait time with both MA and SLO at high level needs to be considered as described with I008 and I108 on Page 8.

Table 74: Notes on chip functions regarding iC-MCB chip revision 3

iC-MCB Z		
No.	Function, Parameter/Code	Description and Application Notes
1	FIELD INTERFACE: SSI	When SSI is enabled (ENSSI=1) a data length of 16 bit must not be exceeded to ensure proper SSI data transmission.
2	OPERATING REQUIREMENTS: Field Interface BiSS/SSI	At the end of a BiSS/SSI frame a minimum wait time with both MA and SLO at high level needs to be considered as described with I009 and I108 on Page 8.
3	CB_SLI	The data of a previous sensor connected to SLI is temporarily stored in the Data RAM while the host provides data with Transmit SDAD. The host must ensure that the SPI access is finished before the Data RAM overflows.
4	DLEN1, DLEN2	For data lengths < 9 bit, a CRC must be enabled for the corresponding data channel.
5	RSSI	Ring operation may only be enabled, if at least three Data RAM bytes are used. Thus, DLEN1 $\geq$ 8, ENDC1 = 1 and ENDC2 = 1 or DLEN1 $\geq$ 16 and ENDC1 = 1.

Table 75: Notes on chip functions regarding iC-MCB chip revision Z

iC-MCB Z2		
No.	Function, Parameter/Code	Description and Application Notes
1	OPERATING REQUIREMENTS: Field Interface SSI	At the end of a SSI frame a minimum wait time with both MA and SLO at high level needs to be considered as described with I108 on Page 8.
2	DLEN1, DLEN2	For data lengths < 9 bit, a CRC must be enabled for the corresponding data channel.
3	RSSI	Ring operation may only be enabled, if at least three Data RAM bytes are used. Thus, DLEN1 $\geq$ 8, ENDC1 = 1 and ENDC2 = 1 or DLEN1 $\geq$ 16 and ENDC1 = 1.

Table 76: Notes on chip functions regarding iC-MCB chip revision Z2

REVISION HISTORY

Rel.	Rel. Date[1]	Chapter	Modification	Page
A1	2017-11-17		Initial release.	

Rel.	Rel. Date[1]	Chapter	Modification	Page
B1	2020-09-11	STARTUP AND OPERATION	CHPREL extended by 0x04: iC-MCB Z	13
		STARTUP AND OPERATION	ACQMODE: "Direct" changed to "No delay" and "Sample" changed to "Request"	14
		STARTUP AND OPERATION	Parameter USDST added and description extended	14
		FIELD INTERFACE: BiSS	Parameter BUSY coding changed Renamed characteristic fsys → f_{osc}	15
		BiSS CONTROL COMMUNICATION	Parameter IVALID and CONFIRM added Renamed parameter IDS → IDSDC Renamed parameter BROADCAST → BROADC Renamed parameter OPCODE → CMD Renamed parameter SLAVEID → SIDDC	26f
		HOST INTERFACE: SPI SLAVE	Renamed SPI Opcodes: SDAD Transmission → Transmit SDAD Read REGISTER (delayed) → Read Register Write REGISTER (cont.) → Write Register	19ff
		FAST SENSOR INTERFACE: SPI MASTER	Parameter CLKDIV coding and OSCDIV2 changed.	29

Rel.	Rel. Date[1]	Chapter	Modification	Page
C1	2022-09-23	All	Overall update. Preliminary removed Added SPI and BiSS addresses and links.	All
		DESCRIPTION	Updated.	2
		ELECTRICAL CHARACTERISTICS	El.Char. 214: Added condition for RS422 voltages. El.Char. 225: Corrected T_{CLK}: T_{CLK} = 0.75/fosc → T_{CLK} = 1.33/fosc El.Char. 402: Added characteristic (fosc_in)	6
		OPERATING REQUIREMENTS: Field Interface BiSS	Renamed I001 (t_{Cycle}) and I008 (t_{TO}). Updated I002 (t_{busy}). Added I003 (busy_s) and I009 (t_{Wait}).	8
		OPERATING REQUIREMENTS: Field Interface SSI	I102 (t_C) updated. Renamed I101 (t_{Cycle}), I107 (t_{TO}) and added I108 (t_{Wait}). Added condition for I105 (t_{RQ}).	8
		OPERATING REQUIREMENTS: Host Interface SPI Slave	Renamed I201: t_{c1} → t_c (according to Figure 3).	9
		CONFIGURATION PARAMETERS	Added links for parameters.	10
		REGISTER MAP (HOST INTERFACE)	Split into SPI and BiSS Register Map. Added Data RAM. Updated notes.	11f
		STARTUP AND OPERATION	Added hint on REGPROT. Updated USDST description and added Table 10.	13f
		FIELD INTERFACE: BiSS	Improved BUSY description. Updated ASID description. Added note for DLEN1 and DLEN2.	15
		FIELD INTERFACE: SSI	Added hint on notes in design review. Added note for RSSI.	18
		HOST INTERFACE: SPI SLAVE	Improved description for data channel and slave ID arrangment (Figure 13). Updated Control Frame Sequence Figures 18 and 19. Updated PACTIVE description. Updated Figure 11. Updated parameter tables for STATUS, CTRL1 and CTRL2 bits. Added section "BiSS Access Validation". Updated order and description of sections "BiSS Read Register Access", "BiSS Write Register Access", "BiSS Commands". Updated description of CVALID.	19ff
		FAST SENSOR INTERFACE: SPI MASTER	Added note on ACQMODE configuration. Renamed SCLK → SCLK_M, MISO → MISO_M, MOSI → MOSI_M, NCS → NCS_M (according to I/O CROSSBAR). Coding of STAFSI updated. STAFSI=0x01 and STAFSI=0x02 have been swapped.	29
		I/O CROSSBAR	Improved descriptions and Table 67 including example and description. Removed parameter table CMD2EN and added reference to FIELD INTERFACE: BiSS.	31
		APPLICATION OPTIONS	Removed chapter.	
		DESIGN REVIEW: Notes On Chip Functions	Added note 4 for chip revision 3. Added notes 1 to 5 for chip revision Z.	33
		ORDERING INFORMATION	Updated Order Designation.	36

Rel.	Rel. Date[1]	Chapter	Modification	Page
D1	2023-06-13	STARTUP AND OPERATION	Added chip revision Z2 in CHPREL.	13
		FAST SENSOR INTERFACE: SPI MASTER	Swapped Figures 20 and 21 to comply with description.	30
		DESIGN REVIEW: Notes On Chip Functions	iC-MCB_Z, note 2: corrected I008 → I009. Added notes on chip functions for chip revision Z2.	33

[1] Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-MCB	16-pin QFN16, 3 mm x 3 mm, thickness 0.9 mm, RoHS compliant		iC-MCB QFN16-3x3
Evaluation Board	80 mm x 100 mm eval board		iC-MCB EVAL MCB1D

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