

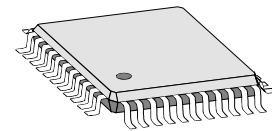
FEATURES

- ◆ Supply voltage range of VBAT= 6 to 16.5V
- ◆ Autarky function to maintain temporarily output voltages with breakdown of supply voltage
- ◆ Adjustable 200mA boost converter (VA1= VBAT+2V to 48V)
- ◆ 6V step-down regulator with integrated 125kHz oscillator
- ◆ Two downstream 5V linear regulators with 200mA/60mA output current
- ◆ 12V/30mA tri-state output
- ◆ Low standby current of typ. 30µA
- ◆ Integrated high/low-side drivers e.g. to attach indicator lamps
- ◆ Overtemperature shutdown of high- and low-side drivers
- ◆ Undervoltage detection
- ◆ Serial single-wire communication interface
- ◆ Watchdog for monitoring of the external µ-controller
- ◆ CMOS-compatible inputs
- ◆ TTL-/CMOS-compatible outputs
- ◆ ESD protection

APPLICATIONS

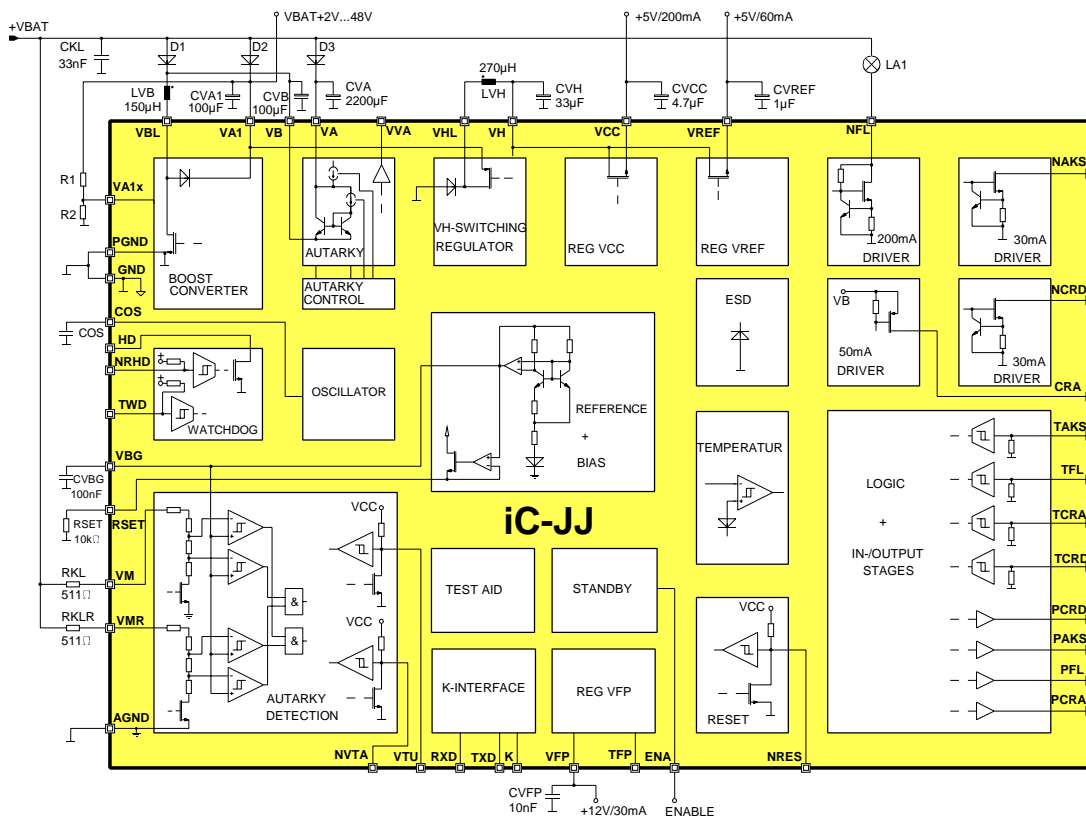
- ◆ Universal voltage supply iC with monitoring and autarky function for the voltage supply of automotive and industrial applications

PACKAGE



MFQ44

BLOCK DIAGRAM



GENERAL DESCRIPTION

Monolithic device iC-JJ supplies electronic systems from a single input voltage VBAT (6V to 16.5V) with voltages which range from 5V to 48V. The autarky function guarantees that the output voltages are maintained for up to several hundred milliseconds, even after the input voltage has been aborted.

A step-up converter produces a voltage of VBAT+2V to 48V, whose setpoint is adjusted via two external resistors at VA1x. Two 5V linear regulators provide 200mA (VCC) and 60mA (VREF). Alternatively, 260mA are available from the 6V step-down converter (VH) whose switching frequency is generated by an integrated 120kHz oscillator. An additional tristate-competent output provides 12V to 30mA and can be activated via a control input for writing data to EEPROMs, for example.

The integrated low voltage and autarky detection function indicates at the error message outputs VTU and NVTA when the relevant low voltage thresholds are reached; there are two different error message outputs for this purpose. The error message is deleted by an external low signal and not when the supply voltage rises again. Information on temporary voltage drops is retained.

If the autarky voltage threshold is undershot, the iC automatically switches into autarky mode. This mode can also be simulated in order to test the autarky capacitor CVA.

Integrated high- and low-side drivers permit various loads to be connected, such as panel indicators (visual monitors), for example. The drivers are switched via control inputs and status outputs are signaling the current switching state back to the controller.

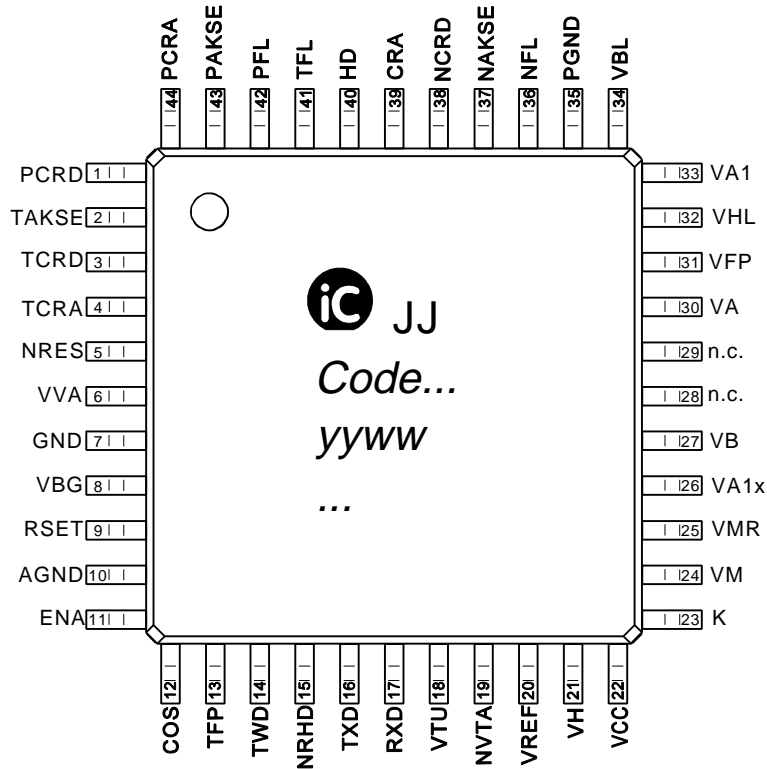
iC-JJ monitors the chip temperature; with excessive temperature the high- and low-side drivers are switched off to reduce the power dissipation.

The integrated watchdog can monitor the correct operation of an external processor. If used, the bi-directional serial communication interface connects the chip with external diagnosis components. The iC can be switched to standby via the input ENA and then draws a low standby current of typically 30 μ A.

The device is protected against destruction due to ESD.

PACKAGE MQFP44 according to the JEDEC standard

PIN CONFIGURATION MQFP44 (top view)



PIN FUNCTIONS

No.	Name	Function	No.	Name	Function
1	PCRD	Message Output for Pin NCRD	25	VMR	Measurement Input Undervoltage- and Autarky Detection
2	TAKS	Trigger Input for Output NAKS	26	VA1x	Setpoint Assignment VA1
3	TCRD	Trigger Input for Output NCRD	27	VB	Supply during autarky mode
4	TCRA	Trigger Input for Output CRA	28	n.c.	
5	NRES	Reset, low active	29	n.c.	
6	VVA	Capacitor Test Output	30	VA	Voltage VA
7	GND	Ground	31	VFP	+12V Tri-state Output (30mA)
8	VBG	Bandgap Reference Voltage	32	VHL	Attachment Inductance for Step-down Regulator
9	RSET	Attachment RSET	33	VA1	VBAT+2V...+48V Output
10	AGND	Analog Ground	34	VBL	Attachment Inductance for Boost Converter
11	ENA	Enable	35	PGND	Ground
12	COS	Capacitor for Oscillator Adjustment	36	NFL	200mA Low-side Driver Output
13	TFP	Trigger Input for Output VFP	37	NAKS	30mA Low-side Driver Output
14	TWD	Trigger Input for Watchdog	38	NCRD	30mA Low-side Driver Output
15	NRHD	Trigger Input for Pin HD	39	CRA	50mA High-side Driver Output
16	TXD	Trigger Input K-Interface	40	HD	Tri-state Output, Low-side Driver
17	RXD	Digital Output K-Interface	41	TFL	Trigger Input for Output NFL
18	VTU	Message Output Undervoltage Detection	42	PFL	Message Output for Pin NFL
19	NVTA	Message Output Autarky Detection	43	PAKS	Message Output for Pin NAKS
20	VREF	+5V Output (60mA)	44	PCRA	Message Output for Pin CRA
21	VH	+6V Output			
22	VCC	+5V Output (200mA)			
23	K	Bidirectional K-Interface			
24	VM	Measurement Input Undervoltage- and Autarky Detection			

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item	Symbol	Parameter	Conditions	Fig.			Unit
					Min.	Max.	
G001	V()	Voltage at COS, TWD, VBG, RSET, RXD, TXD, TFP, TAKS, TFL, TCRD, TCRA, PFL, PAKS, PCRD, PCRA, NRES, NVTA, VTU, NRHD, VVA	$V() \leq VCC + 0.3V$		-0.3	5.5	V
G002	I()	Current in Pins COS, TWD, VBG, RSET, RXD, TXD, TFP, TAKS, TFL, TCRD, TCRA, PFL, PAKS, PCRD, PCRA, NRES, NVTA, VTU, NRHD, VVA			-10	10	mA
G003	ESD	ESD Susceptibility at VM, VMR, VHL	MIL-STD-883, Method 3015.7 HBM 100pF discharged through 1.5kΩ			0.8	kV
G004	ESD	ESD Susceptibility at all other Pins	MIL-STD-883, Method 3015.7 HBM 100pF discharged through 1.5kΩ			1.4	kV
G201	V(NAKS)	Voltage at NAKS			-1.2	48	V
G202	I(AKS)	Current in NAKS			-30	30	mA
G401	V(ENA)	Voltage at ENA			-0.3	48	V
G402	I(ENA)	Current in ENA			-4	4	mA
G501	V(VHL)	Voltage at VHL	$V(VHL) \leq V(VA1)$		-1.4	48	V
G502	I(VHL)	Current in VHL			-600	10	mA
G503	V(VH)	Voltage at VH	$V(VH) \geq V(VCC)$ $V(VH) \geq V(VREF)$		-0.3	7	V
G504	I(VH)	Current in VH			-6	600	mA
G505	V(VH)	Voltage at VH	$V(VH) \geq V(VCC)$ $V(VH) \geq V(VREF), I < 50mA$		-0.3	10	V
G601	V(VCC)	Voltage at VCC	$V(VCC) \leq V(VH)$		-0.3	5.5	V
G602	I(VCC)	Current in VCC			-300	10	mA
G701	V(VREF)	Voltage at VREF	$V(VREF) \leq V(VH)$		-0.3	5.5	V
G702	I(VREF)	Current in VREF			-100	10	mA
G901	V(VFP)	Voltage at VFP			-0.3	12.5	V
G902	I(VFP)	Current in VFP			-40	6	mA
GA01	V(VA1)	Voltage at VA1			-0.3	48	V
GA02	I(VA1)	Current in VA1			-1600	10	mA
GA03	V(VA1x)	Voltage at VA1x			-0.3	7	V
GA04	I(VA1x)	Current in VA1x			-4	4	mA
GA05	V(VBL)	Voltage at VBL			-0.3	48	V
GA06	I(VBL)	Current in VBL			-10	1600	mA
GB01	V(K)	Voltage at K			-8.8	48	V
GB02	I(K)	Current in K			-6	200	mA
GC01	V(HD)	Voltage at HD			-0.3	48	V
GC02	I(HD)	Current in HD			-4	4	mA
GD01	V(NFL)	Voltage at NFL	applied via lamp of 2W		-1.2	48	V
GD02	I(NFL)	Current in NFL			-200	200	mA
GG01	V(VA)	Voltage at VA			-0.3	48	V
GG02	I(VA)	Current in VA	$V(VA, VB) < 3V, t < 2s$		-20	500	mA

All voltages are referenced to ground unless otherwise noted.

All currents into the device pins are positive; all currents out of the device pins are negative.

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item	Symbol	Parameter	Conditions	Fig.			Unit
					Min.	Max.	
GG03	V(VB)	Voltage at VB			-0.3	48	V
GG04	I(VB)	Current in VB	V(VA, VB) < 3V, t < 2s		-500	50	mA
GG05	I _{max} (VB)	Max. Current Load at VB during Autarky Case	VA1 < 30.6V, CVB < 120μF, RVB > 9.5Ω		-200	0	mA
GH01	V(NCRD)	Voltage at NCRD			-1.2	48	V
GH02	I(NCRD)	Current in NCRD			-30	30	mA
GI01	V(CRA)	Voltage at CRA			-8.8	48	V
GI02	I(CRA)	Current in CRA			-50	50	mA
GP01	V(VM)	Voltage at VM	via 511Ω		-1.5	48	V
GP02	I(VM)	Current in VM			-55	20	mA
GP03	V(VMR)	Voltage at VMR	via 511Ω		-1.5	48	V
GP04	I(VMR)	Current in VMR			-55	20	mA
GP05	I(VM)	Current in VM	t < 100ms		-160	20	mA
GP06	I(VMR)	Current in VMR	t < 100ms		-160	20	mA
TG1	T _j	Junction Temperature			-40	125	°C
TG2	T _s	Storage Temperature Range			-40	125	°C
TG3	T _l	Lead Temperature	soldering, 10sec			260	°C

THERMAL DATA

Operating conditions: +VBAT= 6..16.5V, PGND= GND, COS= 680pF, RSET= 10kΩ, RKL= 511Ω, RKLr= 511Ω, T_j= -40..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Fig.				Unit
					Min.	Typ.	Max.	
T001	T _a	Operating Ambient Temperature Range			-40		95	°C
T002	R _{thja}	Thermal Resistance Chip / Ambient				40		K/W

ELECTRICAL CHARACTERISTICS

Operating conditions: +VBAT= 6..16.5V, PGND= GND, COS= 680pF,
RSET= 10kΩ, RKL= 511Ω, RKLR= 511Ω, Tj= -40..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.				Unit
						Min.	Typ.	Max.	
Total Device									
1	I(VA1)	Supply Current in VA1	outputs passive, VA1= 30V, VH= 6V			8	3	52	mA
002	I(VH)	Supply Current in VH	in-/outputs passive, VA1= 30V, VH= 6V			25	5	75	mA
003	I(KL, KLR)	Supply Current in KL, KLR	in-/outputs passive, switching regulator active, V(KL, KLR)= 12V			8	12	16	mA
004	I(KL, KLR)	Supply Current in KL, KLR	in-/outputs passive, switching regulator active, V(KL, KLR)= 6.5V			20	25	32	mA
5	I(KL, KLR)	Supply Current in KL, KLR	no external capacitance at VA1, VA, VB; ENA= lo, V(KL, KLR) < 18V					100	μA
006	Rpu()	Pull-up Resistor to VCC at Inputs TWD, TXD, NRHD, NRES, NVTA, VTU		27		5.4	9.1	15.4	kΩ kΩ
7	Rpd()	Pull-down Resistor to GND at Inputs TFP, TAKS, TFL, TCRD, TCRA	for TFP test mode= lo	27		8.8	14.7	24.6	kΩ kΩ
8	Vpu()	Pull-up Voltage to VCC at Inputs TWD, TXD, NRHD, NRES, NVTA, VTU	Vpu()= V()- VCC; I()= -10..10μA			-0.3			V
9	Vpd()	Pull-down Voltage to GND at Inputs TFP, TAKS, TFL, TCRD, TCRA	I()= -10..10μA, for TFP test mode= lo					0.3	V
10	Vt()hi	Threshold Voltage hi at Inputs TWD, TXD, TFP, TAKS, TFL, TCRD, TCRA, NRHD, NRES, NVTA, VTU						67	%VCC
11	Vt()lo	Threshold Voltage lo at Inputs TWD, TXD, TFP, TAKS, TFL, TCRD, TCRA, NRHD, NRES, NVTA, VTU				33			%VCC
12	Vt()hys	Hysteresis at Inputs TWD, TXD, TFP, TAKS, TFL, TCRD, TCRA, NRHD, NRES, NVTA, VTU	Vt()hys= Vt()hi- Vt()lo			500			mV
13	Vs()lo	Saturation Voltage lo at Outputs NRES, NVTA, VTU, RXD, PFL, PAKS, PCRD, PCRA	I()= 1.6mA, outputs lo					0.4	V
14	Vs()hi	Saturation Voltage hi vs. VCC at Outputs RXD, PFL, PAKS, PCRD, PCRA	Vs()= V()- VCC; I()= -1mA, outputs hi			-0.8			V
15	Isc()	Short-circuit Current in Outputs NRES, NVTA, VTU, HD	V()= VCC, pins= lo, V(HD)= VA1	27			10	30	mA mA
16	tsup()	Permissible Spurious Pulse Width at Inputs TWD, TXD, TFP, TAKS, TFL, TCRD, TCRA, NRHD, NRES, NVTA, VTU	no switching triggered					40	ns

ELECTRICAL CHARACTERISTICS

Operating conditions: +VBAT= 6..16.5V, PGND= GND, COS= 680pF,
RSET= 10kΩ, RKL= 511Ω, RKLr= 511Ω, Tj= -40..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.				Unit
						Min.	Typ.	Max.	
Total Device (continued)									
17	Vc()lo	ESD Clamp Voltage lo at COS, TWD, VBG, RSET, AGND, RXD, TXD, NRES, NVTA, VTU, VM, VMR, TFP, TFL, PFL, VH, VREF, VCC, ENA, TAKS, PAKS, TCRD, TCRA, PCRD, PCRA, NRHD, VVA, HD, VA1x, VA, VB	against GND, I()= -10mA			-1.4		-0.3	V
18	Vc()lo	ESD Clamp Voltage lo at NFL, VHL, VFP, VA1, VBL, NCRD, NAKS	against PGND, I()= -10mA			-1.4		-0.3	V
19	Vc()lo	ESD Clamp Voltage lo at K	against GND, I()= -10mA			-15		-5.5	V
20	Vc()lo	ESD Clamp Voltage lo against PGND at CRA	against PGND, I()= -10mA			-15		-5.5	V
21	Vc()hi	ESD Clamp Voltage hi at COS, TWD, VBG, RSET, AGND, RXD, TXD, NRES, NVTA, VTU, VREF, VCC, VH, VA1x, VVA, TAKS, PAKS, TFL, PFL, TCRD, TCRA, PCRD, PCRA, NRHD	against GND, I()= 10mA			5.5		14	V
22	Vc()hi	ESD Clamp Voltage hi at TFP	against GND, I()= 10mA			5.5		16	V
023	Vc()hi	ESD Clamp Voltage hi at VFP	against PGND, I()= 10mA			12.5		28	V
24	Vc()hi	ESD Clamp Voltage hi at CRA, NCRD, K, VM, VMR, NFL, NAKS, VHL, VA1, VBL, VA, VB, ENA, HD	against PGND, I()= 10mA	27		48	52	60	V
25	tTHL	Fall Time at RXD, PFL, PAKS, PCRD, PCRA, NRES, NVTA, VTU	CL= 75pF V(): hi= 80% - lo= 20% VCC					60	ns
026	tTHL	Rise Time at RXD, PFL, PAKS, PCRD, PCRA	CL= 75pF V(): lo= 20% - hi= 80% VCC					80	ns
27	V()	Permissible Voltage at VA1, VA, VB, VBL						48	V
Reference and Bias									
101	V(VBG)	Voltage at VBG	CVBG= 10..200nF	27		2.36	2.44	2.52	V V
102	V(RSET)	Voltage at RSET	R(RSET/AGND)= 10kΩ ±1%	27		2.36	2.44	2.52	V V
30mA Low-side Driver									
201	VsNAKS	Saturation Voltage at NAKS	I(NAKS)= 30mA, T < Tab, TAKS= hi, NAKS= lo					1	V
202	IscNAKS	Short-circuit Current in NAKS	V(NAKS) < 18V, T < Tab, TAKS= hi, NAKS= lo	27			65	200	mA mA
203	IpdNAKS	Pull-down Current in NAKS	V(NAKS)= 2..16.5V, TAKS= lo			25		100	μA
204	VtNAKS	Switching Threshold at NAKS for PAKS				2.25		2.75	V
205	VfNAKS	Free-wheeling Voltage at NAKS	I(NAKS)= 10mA, TAKS= lo, NAKS= hi			48			V

ELECTRICAL CHARACTERISTICS

Operating conditions: +VBAT= 6..16.5V, PGND= GND, COS= 680pF,
RSET= 10kΩ, RKL= 511Ω, RKLr= 511Ω, Tj= -40..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.				Unit
						Min.	Typ.	Max.	
Thermal Shutdown									
301	Toff	Thermal Shutdown Threshold for NFL, NAKS, CRA, NCRD, K				135		160	°C
302	Ton	Thermal Lock-on Threshold for NFL, NAKS, CRA, NCRD, K				110		145	°C
303	Thys	Temperature Hysteresis Thys= Toff- Ton					12		°C
Standby									
401	V(ENA)lo	Lower Enable Threshold				2			V
402	V(ENA)hi	Upper Enable Threshold						4	V
403	VENAhy	Hysteresis Enable Input				80		800	mV
404	V(ENA)	Permissible Voltage at ENA						48	V
405	Ipd(ENA)	Pull-down Current in ENA	V(ENA)= 2..48V			5		50	μA
VH-Switching Regulator									
501	VHn	Voltage at VH	LVH= 150μH±20%..470μH±20%, CVH= 33μF ±20%, Ri(LVH) < 1.1Ω, I(VH)= -200..0mA	27		5.6	6	6.3	V V
502	Ia(VHL)	Max. DC cutoff Current in VHL	VH < VHn			-800	-500		mA
503	Vs(VHL)	Saturation Voltage at VHL	Vs()= V(VA1)- V(VHL); I(VHL)= -300mA					1.3	V
504	Vf(VHL)	Free-wheeling Diode Forward Voltage	Vf()= V(GND)- V(VHL); I(VHL)= -300mA					1.4	V
505	Iik(VHL)	Leakage Current in VHL	VHL= lo, V(VHL)= 0V..VA1			-100		100	μA
506	ηVH	VH-Switching Regulator Efficiency	I(VH)= -200..-20mA			70			%
Regulator VCC									
601	VCCn	Voltage at VCC	I(VCC)= -200..0mA, VH= 5.6..6.3V, CVCC ≥ 4.7μF ±30%			4.85		5.15	V
602	CVCC	Permissible Capacitance at VCC to AGND	Tolerance ±30%			3.3			μF
603	RiCVCC	Permissible Internal Resistance of Capacitor at VCC						10	Ω
604	dVCCoff	Turn-off Threshold Over- and Undervoltage VCCoff - VCCn for NRES= lo						200	mV
605	dVCCon	Turn-on Threshold Over- and - Undervoltage	dVCCon= VCCon - VCCn , NRES= hi			40			mV
606	dVCCres	Hysteresis of Turn-un and Turn-off Threshold at VCC	dVCCres= VCCon - VCCoff			40			mV
607	tl(NRES)	Reset Pulse Width lo at NRES	Triggered by VCC			6.8			μs
608	Vr(VCC)	Voltage Ratio VCC / VREF	I(VCC)= 0..200mA			0.99		101	

ELECTRICAL CHARACTERISTICS

Operating conditions: +VBAT= 6..16.5V, PGND= GND, COS= 680pF,
RSET= 10kΩ, RKL= 511Ω, RKLR= 511Ω, Tj= -40..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.				Unit
						Min.	Typ.	Max.	
Regulator VREF									
701	VREFn	Voltage at VREF	I(VREF)= -60..0mA, VH= 5.6..6.3V, CVREF ≥ 1μF ±30%			4.9		5.1	V
702	CVREF	Permissible Capacitor at VREF to AGND	tolerance ±30%			1			μF
703	RiCVREF	Permissible Internal Resistance of Capacitor at VREF						10	Ω
704	dVREFoff	Turn-off Threshold Over- and Undervoltage	dVREFoff= VREFoff - VREFn , NRES= lo					200	mV
705	dVREFon	Turn-on Threshold Over- and Undervoltage	dVREFon= VREFon - VREFn , NRES= hi			40			mV
706	dVREFres	Hysteresis of Turn-on and Turn-off Threshold at VREF	dVREFres= VREFon-VREFoff			20			mV
707	tl(NRES)	Reset Pulse Width lo at NRES	Triggered by VREF			6.8			μs
708	Vf	Forward Voltage Discharging Diode between VREF and VCC	I()= 20mA					1.2	V
VFP-Regulator									
901	V(VFP)	Voltage at VFP	I(VFP) ≤ -30mA, VA1 > 15V, TFP= hi	27		11.5	12	12.5	V V
902	Isc(VFP)	Short-circuit Current in VFP	V(VFP) < 11.5V, TFP= hi	27		-200	-90		mA mA
903	Ilk(VFP)	Leakage Current in VFP	V(VFP)= 0..10V, TFP= lo			-10		10	μA
904	Ilk(VFP)	Leakage Current in VFP	V(VFP)= 10..12.5V, TFP= lo			-10		250	μA
905	tsu(VFP)	Settle Time at VFP	V(VFP)= 12V ±0.5V					10	μs
Boost Converter									
A01	VA1n	Voltage at VA1	VB= 14V, LVB= 150μH ±20%, Ri(LVB) < 1Ω, I(VA1)= -200..0mA			28.4		30.6	V
A02	VA1n	Voltage at VA1	VB= 5V, I(VA1)= -25..0mA			28.4		30.6	V
A03	VA1n	Voltage at VA1	VB= 6.5V, I(VA1)= -60mA			284		306	V
A04	VA1	Voltage at VA1	VB= 6.5V, I(VA1)= -120mA			190		306	V
A05	VA1	Voltage at VA1	VB= 6.5V, I(VA1)= -200mA			14.0		30.6	V
A06	Ico(VBL)	DC Cutoff Current in VBL	V(VA1) < 28.5V				1		A
A07	Vs(VBL)	Saturation Voltage at VBL	VBL= lo, I(VBL)= 600mA					1	V
A08	Vf(VBL)	Forward Voltage Free-wheeling Diode	Vf()= V(VBL) - V(VA1); VBL= hi, I(VBL)= 20mA					1.1	V
A09	Vf(VBL)	Forward Voltage Free-wheeling Diode	Vf()= V(VBL) - V(VA1); VBL= hi, I(VBL)= 600mA					1.4	V
A10	ηVA1	Efficiency of VA1-Regulator	VB= 5V, V(VA1) > 28.5V			50			%
A11	ηVA1	Efficiency of VA1-Regulator	VB= 6.5V, V(VA1) > 28.5V			65			%
A12	ηVA1	Efficiency of VA1-Regulator	VB= 18V, V(VA1) > 28.5V			80			%
A13	Ilk(VBL)	Leakage Current in VBL	V(VBL)= 0V..VA1, VBL= hi			-100		100	μA
A14	Vr(VA1)	Voltage Ratio V(VA1) / V(VREF)	internal VA1-voltage divider	27		5.7	5.9	6.1	

ELECTRICAL CHARACTERISTICS

Operating conditions: +VBAT= 6..16.5V, PGND= GND, COS= 680pF,
RSET= 10kΩ, RKL= 511Ω, RKLr= 511Ω, Tj= -40..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.				Unit
						Min.	Typ.	Max.	
Boost Converter (continued)									
A15	Ipu(VA1x)	Pull-Up Current in VA1x	V(VA1x) < 1V	27		-25	-5	-1	μA μA
A16	Vr(VA1x)	Transformation Ratio with external Voltage Divider R(VA1/VA1x) / R(VA1x/AGND)	V(VA1)= (1+R(VA1/VA1x) / R(VA1x/AGND)) × V(VBG), R(VA1x/AGND)= 1..5k, V(VA1)= V(VB)..48V			2		18	
K-Interface									
B01	Vs(K)	Saturation Voltage at K	I(K)= 15.7mA, TXD= lo, T < Tab					1.4	V
B02	Vs(K)	Saturation Voltage at K	I(K)= 32.4mA, TXD= lo, T < Tab					1.7	V
B03	Isc(K)	Short-circuit Current in K	V(K)= 2..27V, TXD= lo, t < 100ms	27			60	150	mA mA
B04	C(K)	Permissible Input Capacitance K						25	pF
B05	Ipu(K)	Pull-Up Current in K	V(KL, KLR)= 8..16.5V, V(K)= 0.2V..V(KL, KLR)-1V V(VA1) > V(VM) + 2V, TXD= hi			-80		-20	μA
B06	Vt(K)	Switching Threshold at K related to Maximum V(KL, KLR)	V(KL, KLR)= 6..16.5V, TXD= hi			45		55	%
B07	Vt(K)	Switching Threshold at K during Autarky	V(KL, KLR) < 5.5V	27		54	60	66	%VCC %VCC
B08	Vhys(K)	Hysteresis at K	V(KL, KLR)= 6..16.5V or Autarky			50		300	mV
B09	tf(K)	Fall Time at K	R(KLR/K)= 511Ω, CK < 5nF, V(K) from hi= 80% → lo= 20% V(KLR), TXD from hi to lo					2	μs
B10	In(K)	Current in K	V(K)= -3V, TXD= hi			-8			mA
B11	Ilk(K)	Leakage Current in K	V(K) > KL, KLR, TXD= hi, V(K) < 27V, VM, VMR > 0V			-20		20	μA
B12	Vf(K)	Free-wheeling Voltage at K	I(K)= 10mA, TXD= hi			48			V
B13	Vpu(K)	Pull-up Current at K against V(VM, VMR)	I(K)= -20μA, TXD= hi, V(VM), V(VMR)= 8..16.5V V(VA1) > V(VM) + 2V			-0.3		0.3	V
B14	tp(K)	Transmission Delay K → RXD	f ≤ 200kHz, V(K) from 25% → 75% V(VM, VMR)				6	2	μs
B15	tp(K)	Transmission Delay TXD→K	f ≤ 200kHz, V(K) from 75% → 25% V(VM, VMR)				4	2	μs
B16	dtp(K)	Transmission Delay Difference K → RXD, K lo → hi to K hi → lo	f ≤ 200kHz, V(K) from 25% → 75% V(VM, VMR)					1	μs
B17	tf(K)	Fall Time at K	R(KLR/K)= 511Ω,, CK < 10nF, V(K) from hi= 80% → lo= 20% V(KLR), TXD from hi to lo					1	μs
Watchdog									
C01	tl(NRES)	Reset Pulse Width lo at NRES	triggered by watchdog			6.5		8.9	μs
C02	Tu(TWD)	Lower TWD Period for Reset		27		404	480	558	μs μs
C03	To(TWD)	Upper TWD Period for Reset		27		652	770	885	ms ms
C04	tp(TWD)	Permissible Pulse Width at TWD	TWD detection at lo pulse			18		649.9	ms

ELECTRICAL CHARACTERISTICS

Operating conditions: +VBAT= 6..16.5V, PGND= GND, COS= 680pF,
RSET= 10kΩ, RKL= 511Ω, RKLR= 511Ω, Tj= -40..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.				Unit
						Min.	Typ.	Max.	
Watchdog (continued)									
C05	tt(TWD)	Permissible Spurious Pulse Width at TWD	no TWD detection at lo pulse					6.5	μs
C06	Ilk(HD)	Leakage Current in HD	V(HD)= 0V..VA1, NRHD= lo			-10		10	μA
C07	Vs(HD)lo	Saturation Voltage lo at Output HD	I()= 1.6mA, output lo					0.5	V
200mA Low-side Driver									
D01	Vs(NFL)	Saturation Voltage at NFL	I(NFL)= 100mA, TFL= hi, NFL= lo, T < Tab					1	V
D02	Vs(NFL)	Saturation Voltage at NFL	I(NFL)= 200mA, TFL= hi, NFL= lo, T < Tab					2	V
D03	Isc(NFL)	Short-circuit Current in NFL	V(NFL) < 18V, TFL= hi, NFL= lo, T < Tab	27			300	500	mA mA
D04	Isc(NFL)	Short-circuit Current in NFL	V(NFL) < 18V, T < Tab, no supply voltage	27			300	500	mA mA
D05	Vt(NFL)	Threshold Voltage at NFL				2.25		2.75	V
D06	Ipd(NFL)	Pull-down Current in NFL	V(NFL)= 2..16.5V, TFL= lo, NFL= hi			0.25		1	mA
D07	Vs(NFL)	Saturation Voltage at NFL	I(NFL)= 100mA, T < Tab, without supply voltage					3.5	V
D08	Vs(NFL)	Saturation Voltage at NFL	I(NFL)= 200mA, T < Tab, without supply voltage					4	V
D09	Vf(NFL)	Free-wheeling Voltage at NFL	I(NFL)= 10mA, TFL= lo, NFL= hi			48			V
D10	Vf(NFL)	Free-wheeling Voltage at NFL	I(NFL)= 200mA, TFL= lo, NFL= hi			48			V
Autarky									
G01	II(VA)	Charging Current from VA1 to VA	V(VA)= 0..V(VA1)- 2V	27		-33	-30	-27	mA mA
G02	Vs(VA)	Saturation Voltage at VA	I(VA)= -2mA, V(VA1) - V(VA)					0.2	V
G03	Vs(VB)	Saturation Voltage VB referred to VA	Vs()= V(VA)- V(VB); I(VB)= -500..0mA, LSA= on					3	V
G04	Ilk(VB)	Leakage Current in VB	V(VA) > V(VB), LSA= off			-100			μA
G05	liik(VB)	Inverse Leakage Current in VB	V(VB)- V(VA)= 0..5V, LSA= off					40	mA
G06	V(VVA)	Output Voltage at VVA related to V(VA)	I(VVA)= -10..10μA, V(VVA)= 0.6V..VREF- 0.1V	27		12	12.5	13	% %
G07	Isc(VVA)	Short-circuit Current in VVA	V(VVA)= 0V..VREF			-1		10	mA
G08	VAmix	Minimal Discharge Voltage at VA at Test-Discharging by NVTA	internal VA1-voltage divider, VA1x against GND	27		20	21	22	V
G09	Vvalo	Lower Turn-off Threshold of Converter				5.5			V
G10	Vvahi	Upper Turn-off Threshold of Converter						7	V
G11	Vhys	Hysteresis Turn-off Threshold	Vhys= Vvahi- Vvalo			0.2		1	V
G12	VAmixx	Minimal Discharge Voltage at VA at Test-Discharging by NVTA	external VA1-voltage divider	27		66	71	76	%VA1 %VA1
G13	I _{max} (VA,VB)	Maximal Current Load at VA during Autarky	VA1 < 30.6V, CVB < 120μF, RVB > 9.5					200	mA

ELECTRICAL CHARACTERISTICS

Operating conditions: +VBAT= 6..16.5V, PGND= GND, COS= 680pF,
RSET= 10kΩ, RKL= 511Ω, RKLR= 511Ω, Tj= -40..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.				Unit
						Min.	Typ.	Max.	
30mA Low-side Driver									
H01	Vs(NCRD)	Saturation Voltage at NCRD	I(NCRD)= 10mA, TCRD= hi, T < Tab					0.5	V
H02	Vs(NCRD)	Saturation Voltage at NCRD	I(NCRD)= 30mA, TCRD= hi, T < Tab					1.5	V
H03	IscNCRD	Short-circuit Current in NCRD	V(NCRD) < 18V, TCRD= hi, T < Tab	27			65	200	mA mA
H04	IpdNCRD	Pull-down Current in NCRD	V(NCRD)= 2..16.5V, TCRD= lo			25		100	μA
H05	Vt(NCRD)	Switching Threshold at NCRD				2.25		2.75	V
H06	Vf(NCRD)	Free-wheeling Voltage at NCRD	I(NCRD)= 10mA, TCRD= lo, NCRD= hi			48			V
H07	tth(NCRD)	Rise Time at NCRD	R(KLR/NCRD)= 1k, V(NCRD) from lo= 10% → hi= 90% V(KL, KLR)					10	μs
H08	thl(NCRD)	Fall Time at NCRD	R(KLR/NCRD)= 1k, CNCRD < 50nF, V(NCRD) from lo= 90% → hi= 10%, V(KL, KLR)					20	μs
H09	tf(NCRD)	Requested Turn-on Duration at NCRD	TCRD= hi, T > Tab, Vs(NCRD) > 2.75V			16.2		31.2	μs
50mA High-side Driver									
I01	Vs(CRA)	Saturation Voltage hi at CRA against VB	Vs()= V(VB)- V(CRA), I(CRA)= -50mA, V(KL, KLR)= 6..16.5V, TCRA= hi, T < Tab					2	V
I02	Vt(CRA)	Switching Threshold at CRA related to Maximum V(KL, KLR)	V(KL, KLR)= 6..16.5V, TCRA= lo			45		55	%
I03	Vt(CRA)	Switching Threshold at CRA during Autarky	V(KL, KLR) < 5.5V	27		54	60	66	%VCC %VCC
I04	VhysCRA	Hysteresis at CRA	V(KL, KLR)= 6..16.5V or autarky			50		300	mV
I05	Vf(CRA)	Free-wheeling Voltage at CRA	I(CRA)= 10mA, TCRA= lo, VB open			48			V
I06	Ipu(CRA)	Pull-up Current in CRA	V(CRA) < VB- 2V, TCRA= lo			-100		-25	μA
I07	Isc(CRA)	Short-circuit Current in CRA	V(CRA) < 18V, TCRA= hi, T < Tab	27		-200	-100		mA mA
I08	Ir(CRA)	Inverse Current in CRA	V(CRA) > V(B), TCRA= lo					50	mA
I09	tf(CRA)	Requested Turn-on Duration at CRA	TCRA= hi, Vs(CRA) > 2V, T > Tab			16.2		31.2	μs
Oscillator									
J01	fos	Oscillator Frequency	COS= 680pF ±5%, VA1 > 4.2V	27		110.5	130	149.5	kHz kHz

ELECTRICAL CHARACTERISTICS

Operating conditions: +VBAT= 6..16.5V, PGND= GND, COS= 680pF,
RSET= 10kΩ, RKL= 511Ω, RKLR= 511Ω, Tj= -40..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.				Unit
						Min.	Typ.	Max.	
Autarky Detection									
P01	Ri()	Input Resistance at VM, VMR		27		50	100	220	kΩ kΩ
P02	Vvtulo	Lower Undervoltage Threshold at KL, KLR	RKL= RKLR= 511Ω ±1%	27		8.75	9		V V
P03	Vvtuhi	Upper Undervoltage Threshold at KL, KLR	RKL= RKLR= 511Ω ±1%	27			10	10.3	V V
P04	Vhys	Hysteresis Undervoltage Detection	Vhys= Vvtuhi- Vvtulo	27		0.8	1	1.2	V V
P05	Vautlo	Lower Autarky Threshold at KL, KLR	RKL= RKLR= 511Ω ±1%			5.5			V
P06	Vauthi	Upper Autarky Threshold at KL, KLR	RKL= RKLR= 511Ω ±1%					6	V
P07	Vhys	Hysteresis Autarky Detection	Vhys= Vauthi- Vautlo			80		300	mV
P08	V(VM, VMR)	Permissible Voltage at KL, KLR						48	V
P09	tt(VM, VMR)	Permissible Spurious Pulse Width at VM, VMR	no undervoltage detection, no autarky detection					6.5	μs

DESCRIPTION OF FUNCTIONS

BOOST CONVERTER

If VA1x is connected to ground, a voltage of 30V becomes available at VA1. An external voltage divider can be used to adjust voltages at VA1 from VBAT+2V to +48V. In this case the band gap voltage of 2.44V is present

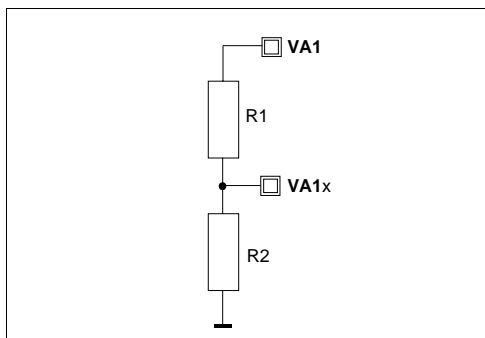


Figure 1: Adjustment V(VA1)

at VA1x. The voltage at VA1 can be calculated via $VA1 = 2.44V \cdot (R1+R2)/R2$.

AUTARKY / LOW VOLTAGE DETECTION

To create a system with a redundant voltage supply, measurement inputs VM and VMR are connected to KL15 and KL15R respectively via a 511Ω resistor. If both supply inputs are used they need to be connected with 511Ω to VBAT. If only one of the two inputs (VM or VMR) is used the unused inputs must be connected to GND.

The system is checked for low voltage and autarky via the internal voltage dividers (at 100kΩ each). The voltage dividers are shut off in standby mode. The outputs of the two comparators for low voltage and autarky are AND-gated, meaning that a message at VTU or NVTA delayed by one clock pulse (8us) is only generated when the relevant voltage thresholds are undershot at both measurement inputs. A reset of the outputs VTU and/or NVTA via the microcontroller with a rising edge at VTU is only possible if low voltage or autarky is no longer detected.

AUTARKY CIRCUIT / MEASUREMENT OF AUTARKY CAPACITANCE

The switch between VA and VB is closed for at least 5 clock cycles after autarky has been detected. With this, the voltage of the autarky capacitor is connected to the input of the VA1 up converter; a stable VA1 voltage can thus be maintained during autarky. At the same time the 30mA current source, which supplies current for charging the autarky capacitor, is switched off.

The voltage of the autarky capacitor can be measured at output VVA ($V(VVA) = 1/8 V(VA)$). This serves to check whether the capacitor is charged to a suitably high voltage to sustain the system during autarky. The capacitance of the capacitor can be determined while the capacitor is being charged. The system's energy consumption can be determined during autarky.

Autarky can be simulated using NVTA as an input. If $V(VA) > 21V$, then the switch between VA and VB can be closed via a rising edge at NVTA. The 30mA current source is then shut down and the autarky capacitor is discharged to the level of the threshold voltage ($V(VA) = 21V$). This is automatically followed by the switch being opened and the current source switched on again. A second falling edge at NVTA will stop discharging the capacitor if $V(VA) > 21V$.

WATCHDOG

If the watchdog is not activated within the stipulated period (500 μ s..800ms), a reset is triggered via NRES. The watchdog counter restarts with each falling edge at TWD. Reset pulses from the microcontroller or V(VCC) or V(VREF) not included in the specifications also reset the watchdog counter.

NRHD and HD activate external hardware in conjunction with the watchdog.

NRDH: CMOS input with a pull-up resistor to activate output HD.

HD: after 128 correct watchdog cycles and when pin NRHD = high, the open-drain transistor is activated (HD = low). Via NRHD = low, a reset (NRES) or false operation of the watchdog, the output is switched to tristate and can only become low again when 128 correct watchdog cycles have again occurred.

RESET

If V(VCC) or V(VREF) are not within specifications range or if the watchdog is operated incorrectly a reset is triggered via the open-drain output NRES. The microcontroller can also trigger a reset externally, thus resetting the watchdog and switching the indicator lamp on via NFL.

VFP REGULATOR

The VFP regulator provides the microcontroller with 12V programming supply voltage. When TFP= high, output VFP is activated; otherwise this output is switched to tristate.

STANDBY

Via input ENA a sleep mode can be set; current consumption is reduced to a minimum of 30 μ A approximately.

K-Interface

The K-Interface uses two pins that can be connected with the serial interface of the microcontroller.

TXD is used to send data via the interface. If TXD is switched from high to low then K switches from V (VM) to low. RXD switches to low if $V(\text{RXD}) < V(\text{VM})/2$ (in Autarky mode $\text{RXD} < 3\text{V}$). If TXD is open then RXD will reflect the external voltage at K.

TEMPERATURE MONITORING

The K interface, indicator lamp output and NAKS output are shut off in the event of excessive temperature. The two driver outputs can be forcibly switched on with excessive temperature for a short period if they are the cause of this excessive temperature. If the level falls below that of the shutdown temperature (hysteresis) the drivers can be switched on again.

OSCILLATOR

The oscillator provides an internal frequency of ca. 125kHz for the switching converters, watchdog counter and autarky control.

30mA LOW-SIDE DRIVER (NCRD)

The low-side driver is switched on by the microcontroller via TCRD = high. A comparator at output PCRD signals the state of the digital crash output to the microcontroller.

TCRD	PCRD	State of the Driver Output NCRD
low	low	Output off
low	high	Short circuit to ground or broken wire
high	low	Short circuit to KL15, KL15R
high	high	Output on

50mA HIGH-SIDE DRIVER (CRA)

The high-side driver is switched on by the microcontroller via TCRA = high. A comparator at output PCRA signals the state of the analog crash output to the microcontroller.

TCRA	PCRA	State of the Driver Output CRA
low	low	Output off
low	high	Short circuit vs. VBAT or broken wire
high	low	Short circuit to ground
high	high	Output on

200mA LOW-SIDE DRIVER (NFL)

The low-side driver which is switched on by the microcontroller via TFL = high. It is also switched on by a flip-flop which mirrors the reset state. This flip-flop can be reset via a falling edge at TFL after the reset has ended. A comparator at output PFL signals the state of the indicator lamp output to the microcontroller. The driver is normally on when no supply voltage is available at the iC.

TFL	PFL	State of the Driver Output
low	low	Output off, lamp off
low	high	Short circuit to ground or broken wire
high	low	Short circuit to KL15, KL15R
high	high	Output on, lamp on

30mA LOW-SIDE DRIVER (NAKS)

The NAKS output is a low-side driver which is switched on by the microcontroller via TAKS= high. A comparator at output PAKS signals the state of the NAKS output to the microcontroller.

TAKS	PAKS	State of NAKS Output
low	low	Output off, lamp off
low	high	Short circuit to ground or broken wire
high	low	Short circuit vs. VBAT
high	high	Output on

ORDERING INFORMATION

Type	Package	Order designation
iC-JJ	MQFP44	iC-JJ MQFP44

For information about prices, terms of delivery, options for other case types ec., please contact:

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