

iC-PVL EVAL PVL1M

EVALUATION KIT DESCRIPTION

ORDERING INFORMATION

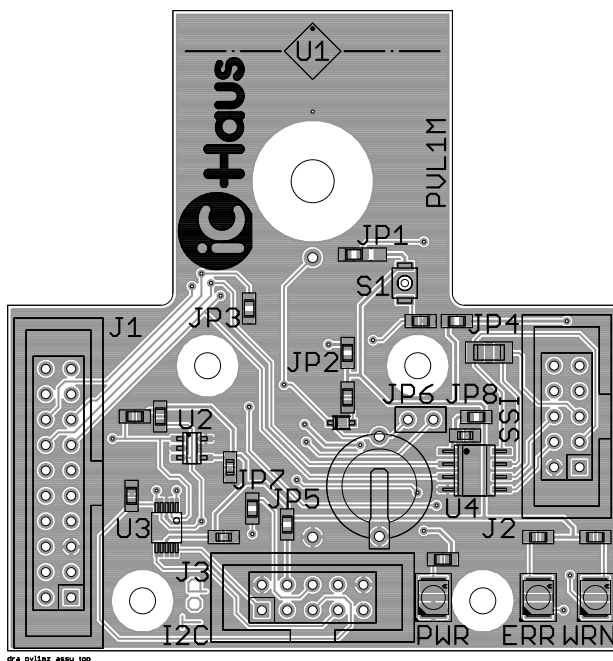
Type	Order Designation	Description Options
Evaluation Kit	iC-PVL EVAL PVL1M	iC-PVL Evaluation Board Ready-to-operate, supplied with premounted magnetic code disc and BiSS adapter cable
Evaluation Software	iC-PVL GUI	GUI Software for Windows PC Device setup file generation, board configuration via adapter For download link check www.ichaus.de/pvl_gui
Related parts PC Adapter	(to be ordered separately) iC-MB3 iCSY MB3U-I2C	PC-USB adapter for BiSS/SSI w. I2C/SPI extension cable Download documentation at www.ichaus.com/tools

BOARD PVL1M

(size 61 mm x 64 mm)

PLUG

CONFIGURATION



J1

Signal Connector

J2

SSI Interface (to PC adapter via BiSS adapter cable)

J3

I²C Interface (to PC adapter I²C extension cable)

Figure 1: Component side

iC-PVL EVAL PVL1M

EVALUATION KIT DESCRIPTION

OVERVIEW OF KIT ITEMS

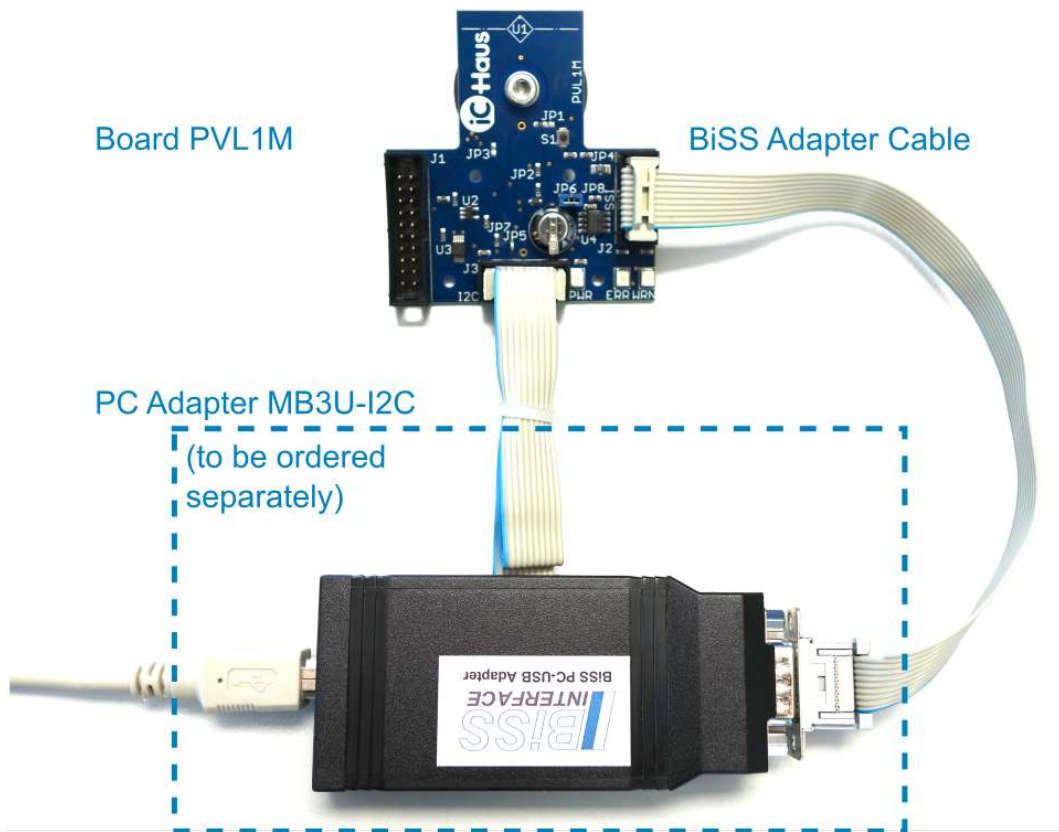


Figure 2: Application of evaluation kit



Figure 3: Bottom side with MU18S 30-32N magnetic code disc

ON-AXIS APPLICATION EXAMPLE

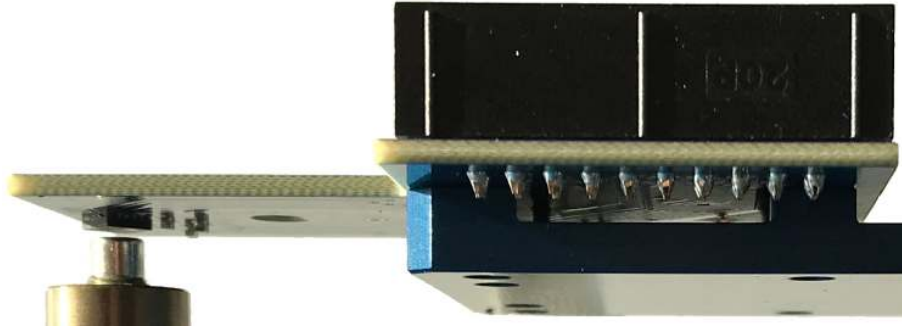


Figure 4: On-Axis application of evaluation kit. Dismount default Off-Axis target and set parameter ONAX = 0x01 and POLEWID = 0x01. PCR = 0x00 is recommended. Please refer to iC-PVL specification.

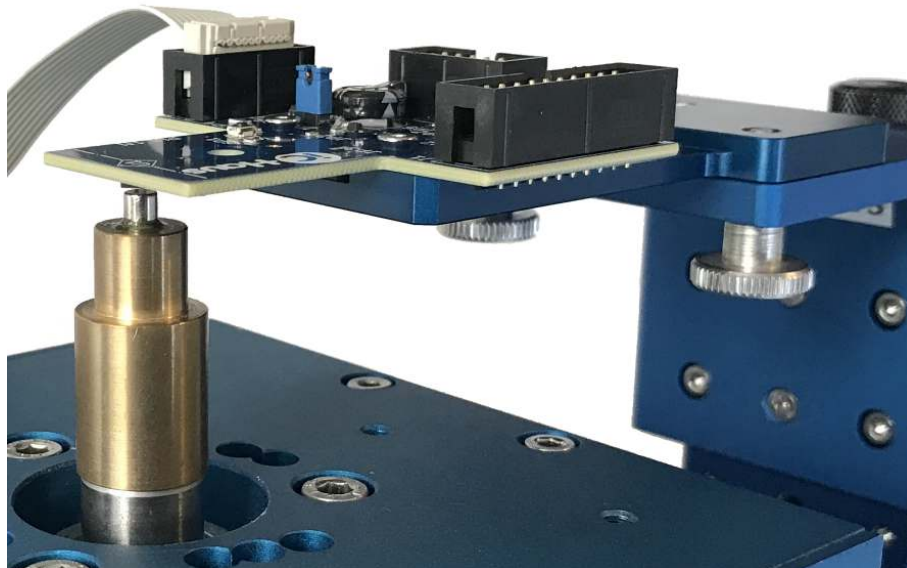


Figure 5: On-Axis application of evaluation kit

iC-PVL EVAL PVL1M

EVALUATION KIT DESCRIPTION



Rev A2, Page 4/9

RELATED PRODUCTS AND DOCUMENTS

- IC Documentation
→ <http://www.ichaus.de/PVL>
- PC-USB Adapter Description
→ http://www.ichaus.de/MB3U_MB3U-I2C_datasheet_en
- GUI Software for Windows PC: check here for download links
→ <http://www.ichaus.de/PVL>

PINOUT OF CONNECTORS

J2: SSI Interface Connector

(2x5 pin male)

Pin	Name	Function
1	-	-
2	GND	Ground
3	MA	SSI Clock Input P
4	SL*	SSI Data Output P
5	NMA	SSI Clock Input N
6	NSL*	SSI Data Output N
7	+5V	Supply Voltage
8	-	-
9	-	-
10	-	-

J3: I²C Interface Connector

(2x5 pin male)

Pin	Name	Function
1	SCL	I ² C Interface, Clock Line
2	GND	Ground
3	-	-
4	+5V	Supply Voltage
5	ENI2C	Enable I2C Access from J3
6	PRE	Preset of iC-PVL
7	SDA	I ² C Interface, Data Line
8	-	-
9	-	-
10	GND	Ground

J1: Signal Connector

(2x10 pin male)

Pin	Name	Function
J1-1	SEL	Mode Select Input
J1-2	PRE	Preset Trigger Input
J1-3	NERR	Error Output (active low)
J1-4	SDA	I ² C Interface, Data Line
J1-5	GND	Ground
J1-6	VBAT	Battery Supply Voltage Input (typ. 3.6 V)
J1-7	VDDS	Switched Supply Voltage Output
J1-8	VDD	+3.0 V to 5.5 V Main Supply Voltage Input
J1-9	N2	Parallel Output MSB, Incremental Output B
J1-10	P2	Parallel Output MSB-1, Incremental Output A
J1-11	N0	Parallel Output LSB
J1-12	NWRN	Battery Warning Output (active low)
J1-13	DO_P0	Multiturn Interface, Data Output, Parallel Output Bit 0 (positive logic)
J1-14	CLK_N1	Multiturn Interface, Clock Line, Parallel Output Bit 1 (negative logic)
J1-15	DI_P1	Multiturn Interface, Data Input, Parallel Output Bit 1 (positive logic)
J1-16	SCL	I ² C Interface, Clock Line
J1-17	Battery	On-board Capacitor (CBATT) or Battery (CBATT2)
J1-18	-	-
J1-19	-	-
J1-20	-	-

* When using differential signaling the line needs to be terminated appropriately. Single ended signaling should only be used for very short line lengths.

iC-PVL EVAL PVL1M

EVALUATION KIT DESCRIPTION

DESCRIPTION OF JUMPERS

Jumper JP1	iC-PVL Operating Mode
Pos. 1-2	SEL connected to GND: Battery Buffered Counter with Serial Readout (default)
Pos. 2-3	SEL connected to Board Power Supply: 3 bit parallel Encoder with Complementary Output
Open	Not Allowed

Jumper JP2	Function
Closed	iC-PVL Power Supply VDD connected to Board Power Supply (default)
Open	iC-PVL Power Supply VDD disconnected from Board Power Supply

Jumper JP3	Function
Closed	DI connected to GND
Open	DI open (default)

Jumper JP4	Function
Closed	Board Power Supply via SSI connector J2 (default)
Open	Board not supplied via J2

Jumper JP5	Function
Closed	Board Power Supply via I2C connector J3
Open	Board not supplied via J3 (default)
Note	Do not install JP4 and JP5 simultaneously

Jumper JP6	Function
Closed	iC-PVL VBAT connected to on-board capacitor CBATT (default)
Open	iC-PVL VBAT disconnected from on-board capacitor CBATT

Jumper JP7	Function
Closed	iC-PVL preset pin PRE connected to I2C connector J3 (default)
Open	iC-PVL preset pin PRE not connected to I2C connector J3

SWITCH DESCRIPTION

Switch S1	Function
Push	iC-PVL preset. Configuration is loaded from EEPROM.

iC-PVL EVAL PVL1M

EVALUATION KIT DESCRIPTION

CIRCUIT SCHEMATIC

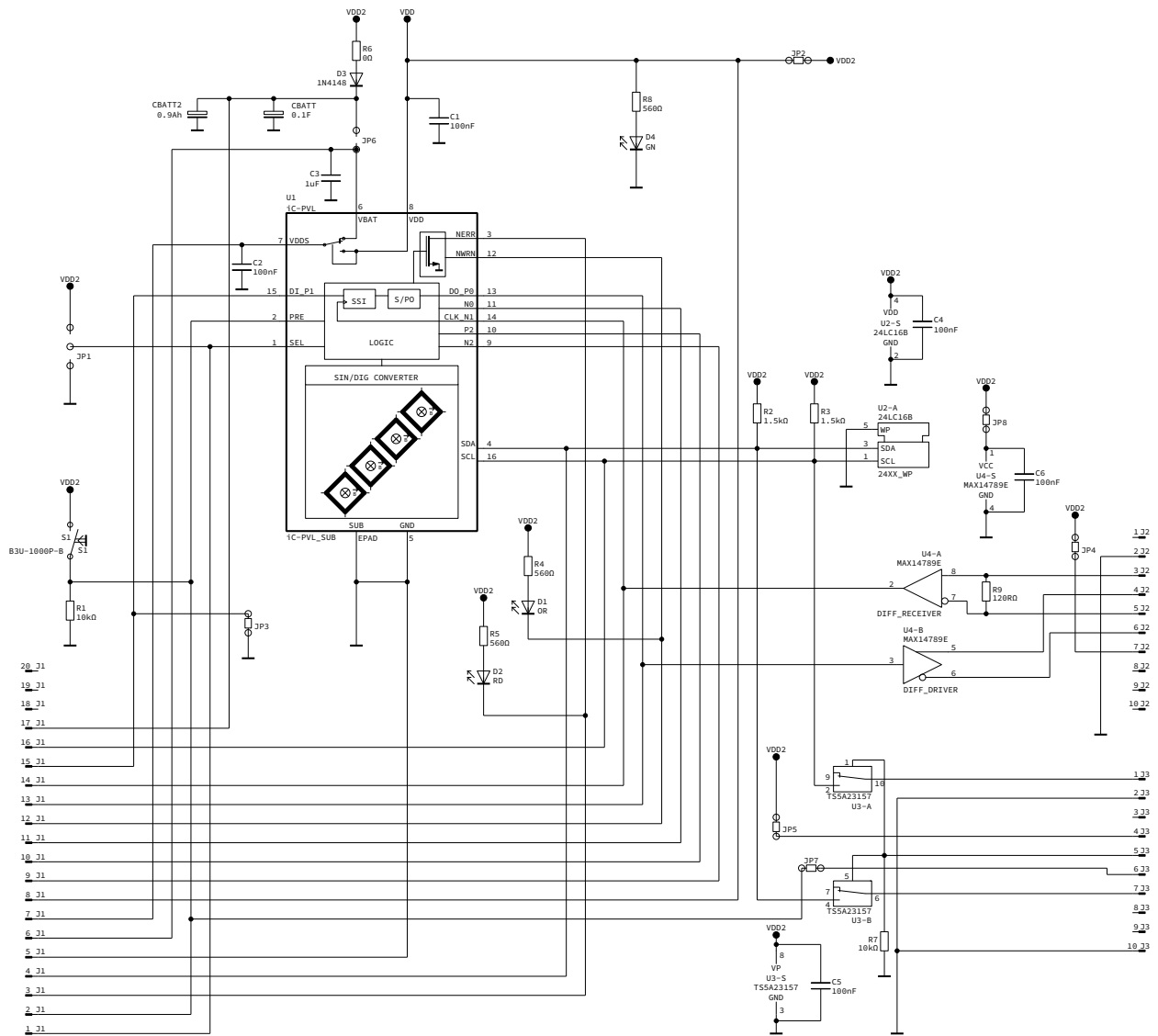


Figure 6: Circuit diagram (board PVL1MZ)

PHYSICAL DIMENSIONS

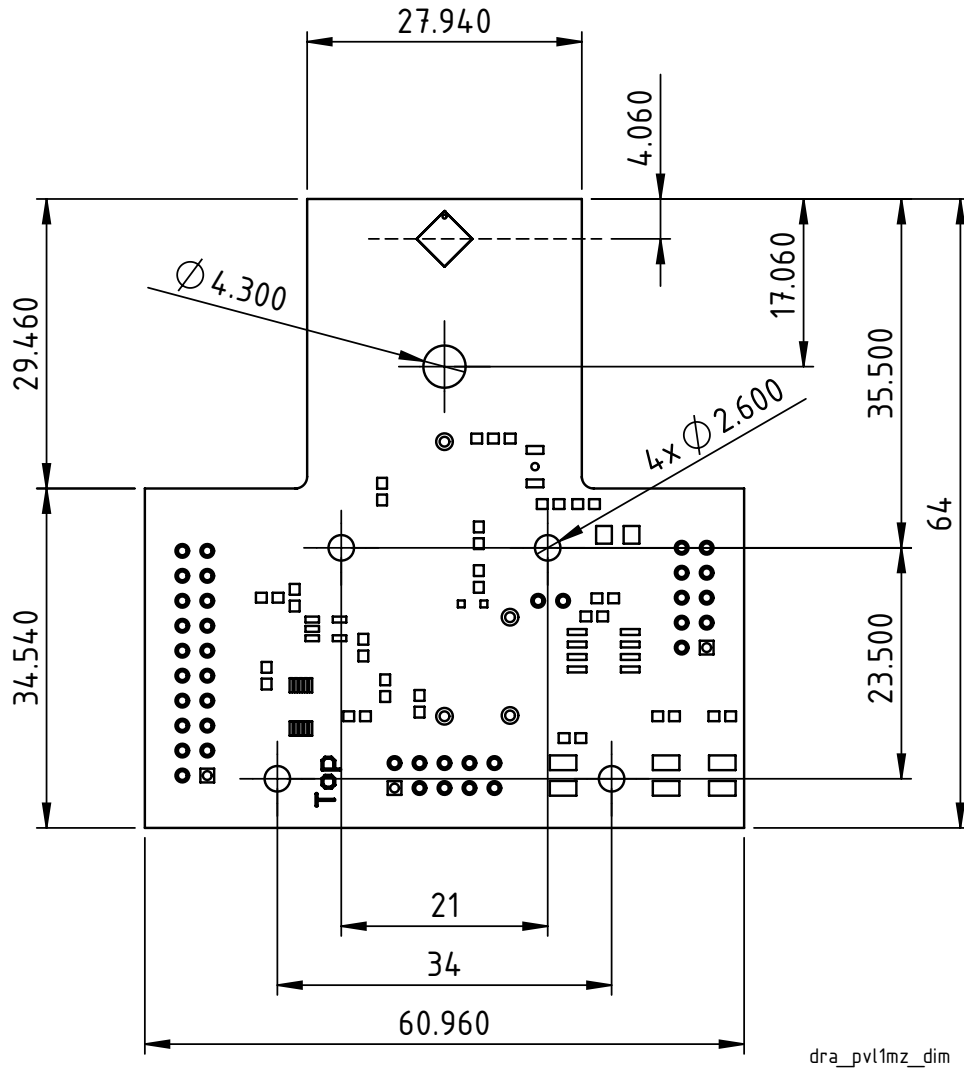


Figure 7: Physical dimensions (board PVL1MZ)

iC-PVL EVAL PVL1M

EVALUATION KIT DESCRIPTION

ASSEMBLY PART LIST

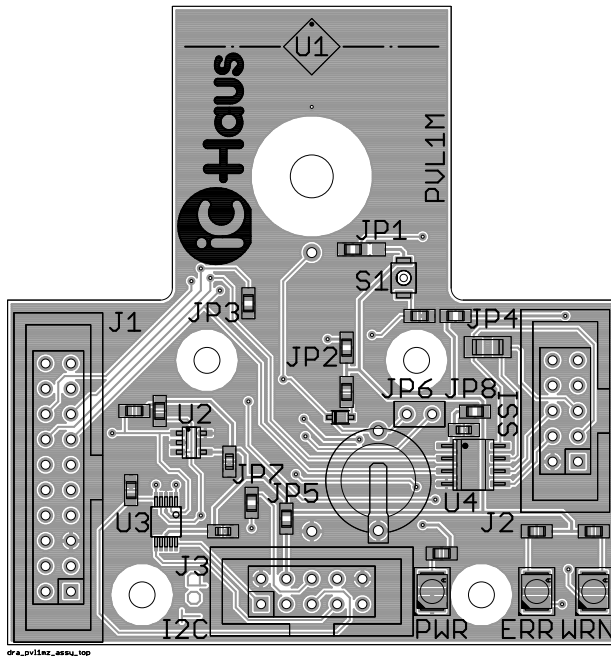


Figure 8: PCB (top side)

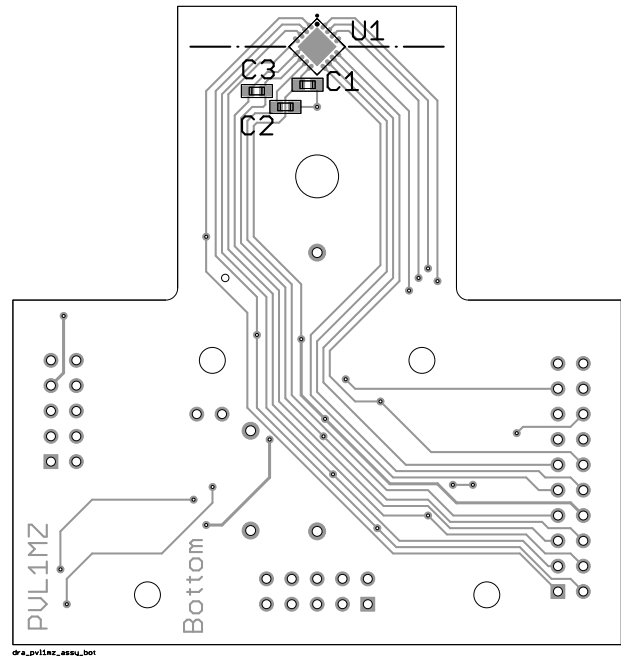


Figure 9: PCB (bottom side)

Device	Value (typical)	Comment
U1	iC-PVL	Linear/off-axis hall-multiturn encoder IC
U2	24AA02	Serial EEPROM
U3	TS5A23157	Dual analog MUX
U4	MAX14789E*	Differential line driver/receiver
R1, R7	10 k Ω	Pull-down resistor
R2, R3	1.5 k Ω	I2C pull-up resistor
R4, R5, R8	560 Ω	LED series resistor
R9	120 Ω	Line termination resistor
JP1, JP2, JP4, JP7, R6	0	0 Ω resistor
D1	LO-T67K	Indicator LED for warning message (orange)
D2	LS-T67K	Indicator LED for error message (red)
D3	1N4148WS	Series diode for CBATT voltage reduction
D4	LG-T67K	Indicator LED for board power supply (green)
C1, C2, C4, C5, C6	100 nF	Supply backup capacitor
C3	1 μ F	Supply backup capacitor
CBATT	100 mF	Supercapacitor for iC-PVL battery-buffer evaluation
J1	WSL20G	Signal connector
J2	WSL10G	SSI interface (to PC adapter via BiSS adapter cable)
J3	WSL10G	I2C connector (to PC adapter I ² C extension cable)
S1	B3U-1000P-B	Preset switch

* Replaces SN65LBC179A for 3V compatibility from batch 5 on.

iC-PVL EVAL PVL1M

EVALUATION KIT DESCRIPTION



Rev A2, Page 9/9

REVISION HISTORY

Rel.	Rel. Date [†]	Chapter	Modification	Page
A1	16-05-25	All	Initial release	All

Rel.	Rel. Date [†]	Chapter	Modification	Page
A2	2019-06-12	ASSEMBLY PART LIST	U4: MAX14789E replaces SN65LBC179A from batch 5 on.	8
		All	Minor corrections / updates	All

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[†] Release Date format: YYYY-MM-DD