

# iC-PN Series

## PHASED ARRAY NONIUS ENCODERS



Rev F2, Page 1/16

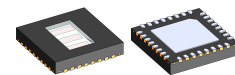
### FEATURES

- ◆ Compact, high resolution absolute encoder ICs for up to 23 bit singleturn resolution (with nonius interpolation)
- ◆ For code discs of  $\varnothing$  18 mm,  $\varnothing$  26 mm,  $\varnothing$  33 mm,  $\varnothing$  39 mm
- ◆ Monolithic 3-channel *HD Phased Array* with excellent signal matching
- ◆ Moderate track pitch for reduced cross talk
- ◆ Ultra low dark currents for operation up to high temperature
- ◆ Low noise amplifiers with high transimpedance gain
- ◆ Enhanced EMI tolerance by low impedance differential, short-circuit-proof, analog sine/cosine outputs
- ◆ Low power consumption from single 4.1 to 5.5 V supply
- ◆ Operational temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- ◆ Space saving optoQFN and optoBGA packages (RoHS compliant)
- ◆ Evaluation kits with LED and code disc available for sampling

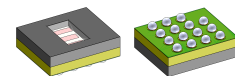
### APPLICATIONS

- ◆ Absolute position encoders
- ◆ AC servo feedback

### PACKAGES

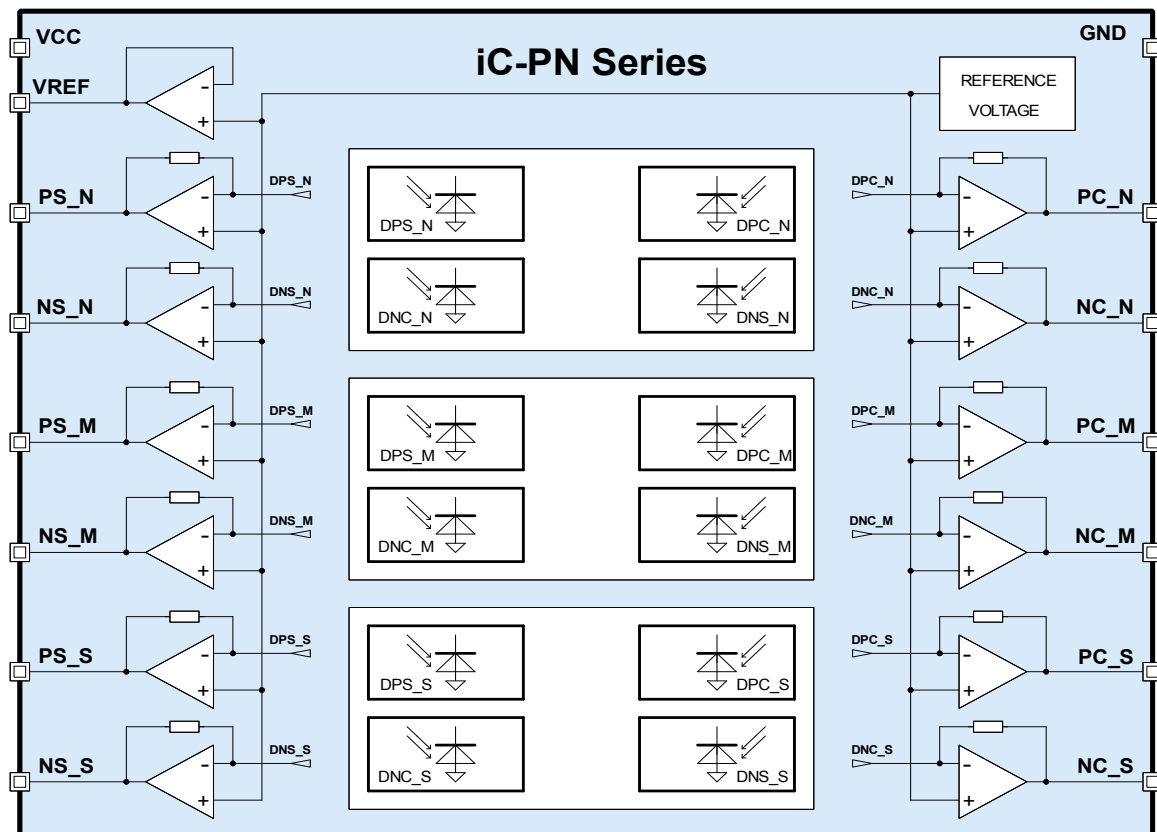


32-pin optoQFN  
5 mm x 5 mm x 0.9 mm  
RoHS compliant



15-pin optoBGA  
6.2 mm x 5.2 mm x 1.7 mm  
RoHS compliant

### BLOCK DIAGRAM



# iC-PN Series

## PHASED ARRAY NONIUS ENCODERS



Rev F2, Page 2/16

### DESCRIPTION

The iC-PN device series represents advanced optical encoder ICs featuring monolithically integrated photosensors arranged as an *HD Phased Array*, providing excellent signal fidelity at relaxed alignment tolerances.

Precise sine/cosine output signals allow for a high-resolution interpolation by subsequent devices: depending on the iC-PN version, a singleturn position can be resolved with up to 23 bit utilizing the 3-channel nonius interpolation of iC-MN.

The typical application of iC-PN devices are absolute position encoders for motion control and drive applications.

The iC-PN scans 3 incremental tracks by a phased-array of multiple photosensors each per track, and generates positive and negative going sine signals, as well as positive and negative going cosine signals. An excellent matching and common mode behavior of the differential signal paths is obtained by a paired

amplifier design. Due to a typical transimpedance gain of  $1\text{ M}\Omega$ , the output signal level reaches a few hundred millivolts already at low light conditions.

#### iC-PN18xx Series

Optical radius 6.9 mm, code disc  $\varnothing$  18.0 mm;  
 iC-PN1864: 64 CPR (63/64/56 CPR)  
 iC-PN1856: 256 CPR (255/256/240 CPR)

#### iC-PN26xx Series

Optical radius 10.9 mm, code disc  $\varnothing$  26.0 mm;  
 iC-PN2656: 256 CPR (256/255/240 CPR)  
 iC-PN2612: 512 CPR (511/512/496 CPR)  
 iC-PN2624: 1024 CPR (1023/1024/992 CPR)

#### iC-PN33xx Series

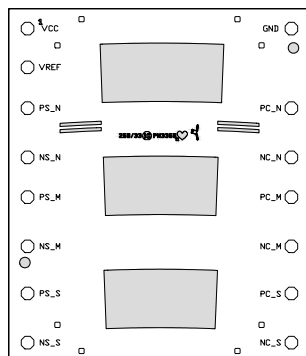
Optical radius 14.5 mm, code disc  $\varnothing$  33.0 mm;  
 iC-PN3356: 256 CPR (256/255/240 CPR)

#### iC-PN39xx Series

Optical radius 17.5 mm, code disc  $\varnothing$  39.0 mm;  
 iC-PN3924: 1024 CPR (1023/1024/992 CPR)

### PACKAGING INFORMATION

#### PAD LAYOUT



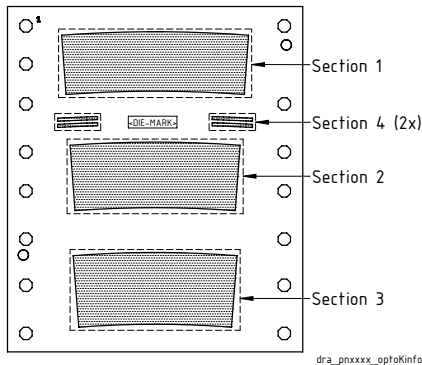
#### PAD FUNCTIONS

##### No. Name Function

Chip layout example.

Grey sections represent sensor layout areas; fill factors vary.

### SENSOR LAYOUT



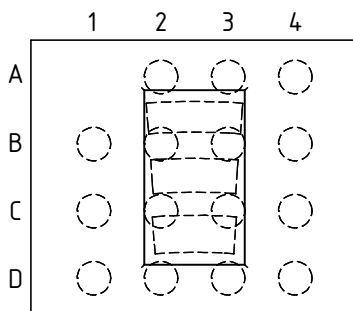
### AOI CRITERIA

<Die Mark>	<Section>	<Area Class> <sup>1</sup>
iC PN2656 Y1	1, 3	A25
	2	A16
	4	A40
iC PN1864		see iC-PN2656
iC PN1856		see iC-PN2656
iC PN3356		see iC-PN2656
iC PN2624 Y1, X	1, 3	A25
	2	A16
	4	A40
iC PN2612		see iC-PN2624
iC PN3312		see iC-PN2624
iC PN3324		see iC-PN2624
iC PN3924		see iC-PN2624

<sup>1</sup> Selection class for the optical inspection of detector areas. Refer to [Optical Selection Criteria](#) for further description.

### PIN CONFIGURATION

oBGA LSH2C (6.2 mm x 5.2 mm)



### PIN FUNCTIONS

No. Name Function

A2	VCC	+4.1..5.5 V Supply Voltage
A3	VREF	Reference Voltage Output
A4	GND	Ground
B1	PS_N	N-Track Sine +
B2	NS_N	N-Track Sine -
B3	NC_N	N-Track Cosine -
B4	PC_N	N-Track Cosine +
C1	PS_M	M-Track Sine +
C2	NS_M	M-Track Sine -
C3	NC_M	M-Track Cosine -
C4	PC_M	M-Track Cosine +
D1	PS_S	S-Track Sine +
D2	NS_S	S-Track Sine -
D3	NC_S	S-Track Cosine -
D4	PC_S	S-Track Cosine +

Note: All signal outputs are analog voltage outputs.

For dimensional specifications refer to the relevant package data sheet, available separately.

# iC-PN Series

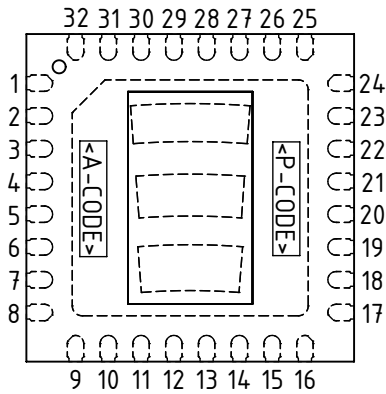
## PHASED ARRAY NONIUS ENCODERS



Rev F2, Page 4/16

### PIN CONFIGURATION

oQFN32-5x5 (5 mm x 5 mm)



### PIN FUNCTIONS

No.	Name	Function
1	VCC	+4.1..5.5 V Supply Voltage
2	VREF	Reference Voltage Output
3	PS_N	N-Track Sine +
4	NS_N	N-Track Sine -
5	PS_M	M-Track Sine +
6	NS_M	M-Track Sine -
7	PS_S	S-Track Sine +
8	NS_S	S-Track Sine -
9..16	n.c. <sup>1</sup>	
17	NC_S	S-Track Cosine -
18	PC_S	S-Track Cosine +
19	NC_M	M-Track Cosine -
20	PC_M	M-Track Cosine +
21	NC_N	N-Track Cosine -
22	PC_N	N-Track Cosine +
23	n.c. <sup>1</sup>	
24	GND	Ground
25..32	n.c. <sup>1</sup>	

BP<sup>2</sup> Backside paddle

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);

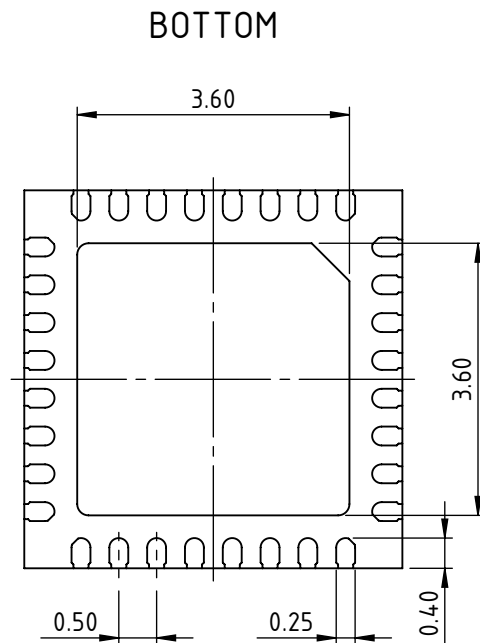
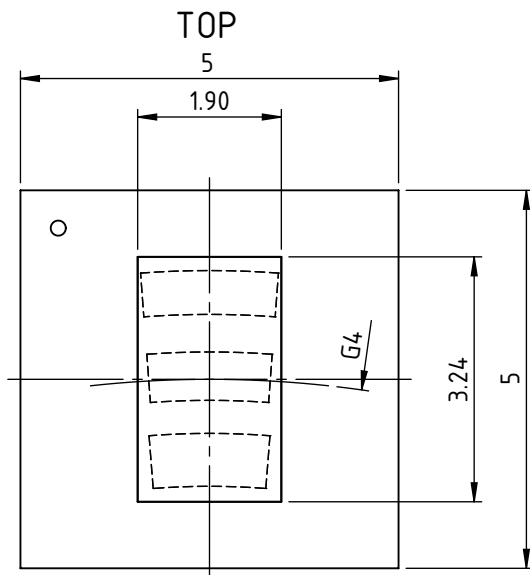
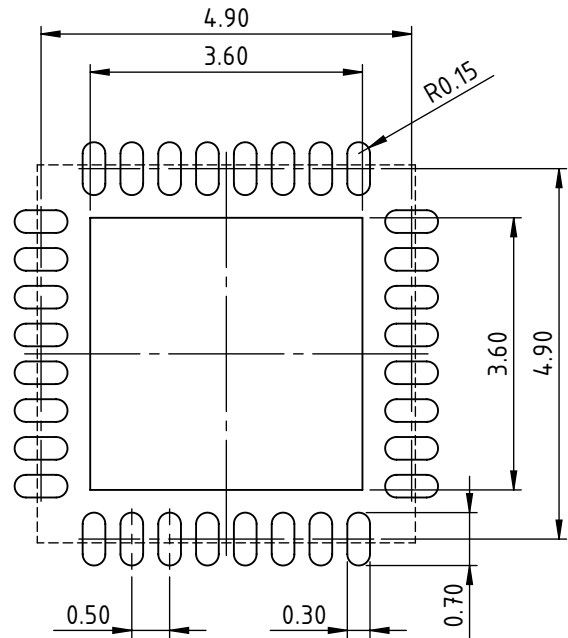
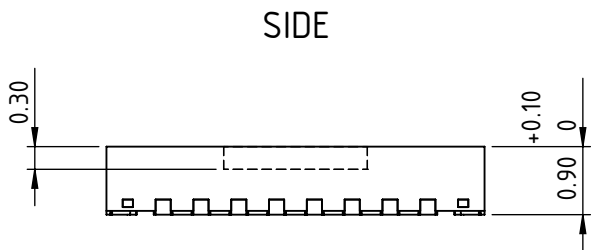
<sup>1</sup> Pin numbers marked n.c. are not connected.

<sup>2</sup> Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

### PACKAGE DIMENSIONS oQFN32-5x5

Drawing valid for chip release Y1, Y1H, Y2.

### RECOMMENDED PCB-FOOTPRINT

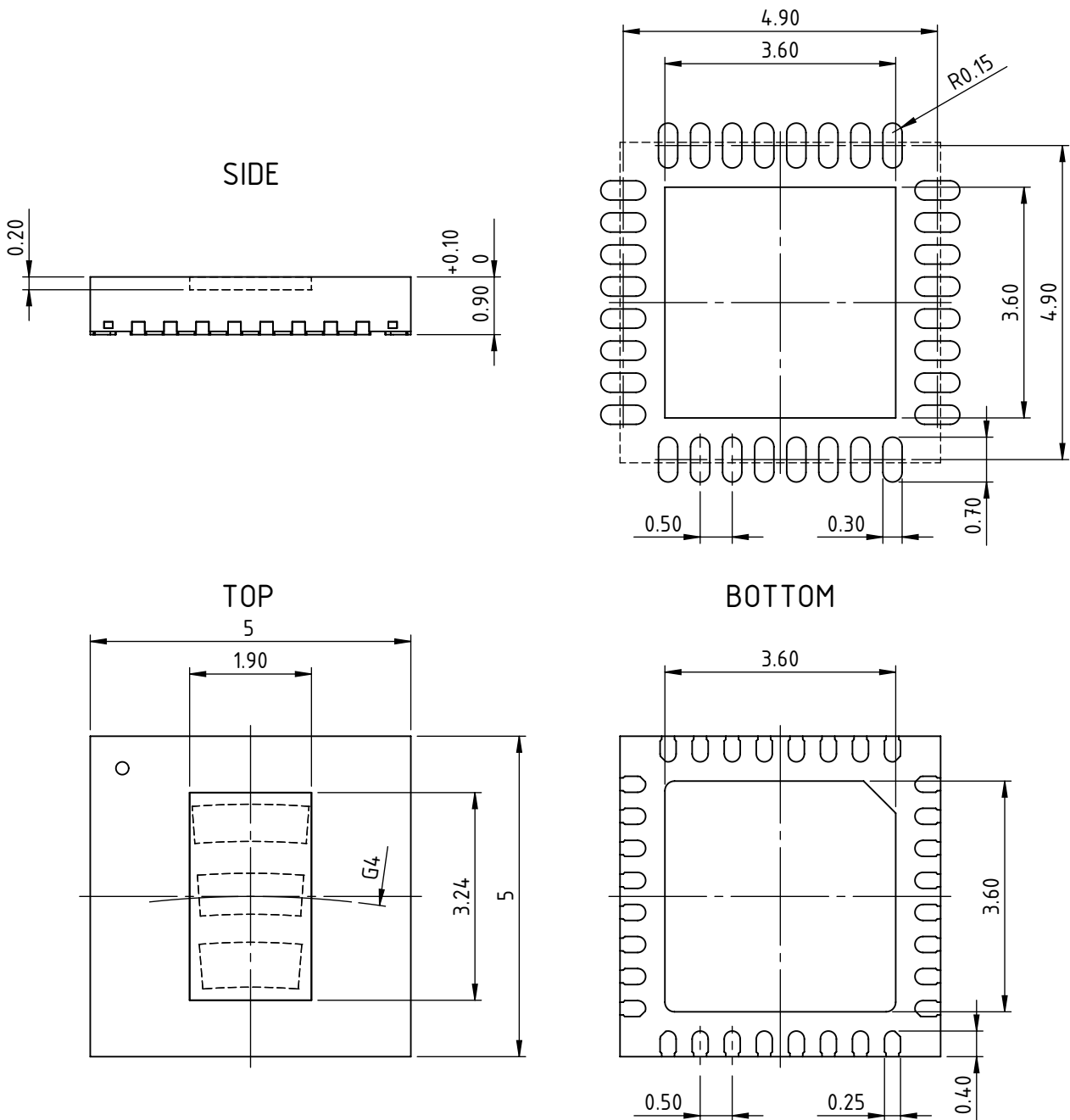


All dimensions given in mm. General Tolerances of form and position according to JEDEC MO-220.  
 Positional tolerance of sensor pattern:  $\pm 70\mu\text{m}$  /  $\pm 1^\circ$  (with respect to center of backside pad).  
 G4: radius of chip center (refer to the relevant encoder disc and code description).  
 Maximum molding excess  $+20\mu\text{m}$  /  $-75\mu\text{m}$  versus surface of glass. Small pits in the mold surface, which may occasionally appear due to the manufacturing process, are cosmetic in nature and do not affect reliability.

### PACKAGE DIMENSIONS oQFN32-5x5

Drawing valid for chip release X.

### RECOMMENDED PCB-FOOTPRINT



All dimensions given in mm. General Tolerances of form and position according to JEDEC MO-220.  
 Positional tolerance of sensor pattern:  $\pm 70\mu\text{m}$  /  $\pm 1^\circ$  (with respect to center of backside pad).  
 G4: radius of chip center (refer to the relevant encoder disc and code description).  
 Maximum molding excess  $+20\mu\text{m}$  /  $-75\mu\text{m}$  versus surface of glass. Small pits in the mold surface, which may occasionally appear due to the manufacturing process, are cosmetic in nature and do not affect reliability.

# iC-PN Series

## PHASED ARRAY NONIUS ENCODERS



Rev F2, Page 7/16

### ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions			Unit
				Min.	Max.	
G001	VCC	Voltage at VCC		-0.3	6	V
G002	I(VCC)	Current in VCC		-20	20	mA
G003	V()	Pin Voltage, all signal outputs		-0.3	VCC + 0.3	V
G004	I()	Pin Current, all signal outputs		-20	20	mA
G005	Vd()	ESD Susceptibility, all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G006	Tj	Junction Temperature		-40	150	°C
G007	Ts	Chip Storage Temperature		-40	150	°C

### THERMAL DATA

Operating conditions: VCC = 4.1...5.5 V

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
T01	Ta	Operating Ambient Temperature Range	package oQFN32-5x5	-40		125	°C
			package oBGA LSH2C	-40		110	°C
T02	Ts	Storage Temperature Range	package oQFN32-5x5	-40		125	°C
			package oBGA LSH2C	-40		110	°C
T03	Tpk	Soldering Peak Temperature	package oQFN32-5x5				
			tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering  MSL 5A (max. floor life 24 h at 30 °C and 60 % RH); Refer to <a href="#">Handling and Soldering Conditions</a> for details.			245 230	°C °C
T04	Tpk	Soldering Peak Temperature	package oBGA LSH2C				
			tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering  TOL (time on label) 8 h; Refer to <a href="#">Handling and Soldering Conditions</a> for details.			245 230	°C °C

All voltages are referenced to ground unless otherwise stated.

All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

# iC-PN Series

## PHASED ARRAY NONIUS ENCODERS



Rev F2, Page 8/16

### ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 4.1...5.5 V, Tj = -40...125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
<b>Total Device</b>							
001	VCC	Permissible VCC Supply Voltage		4.1		5.5	V
002	I(VCC)	VCC Supply Current	no load, Vout() < Vout()mx		9.5	15	mA
003	Vc()hi	Clamp-Voltage hi at all pins	Vc()hi = V() - VCC; I() = 4 mA	0.6		2.0	V
004	Vc()lo	Clamp-Voltage lo at all pins	I() = -4 mA	-1.2		-0.3	V
<b>Photosensors</b>							
101	$\lambda_{ar}$	Spectral Application Range	$Se(\lambda_{ar}) = 0.25 \times S(\lambda_{pk})$	400		950	nm
102	$S(\lambda)$	Spectral Sensitivity	$\lambda_{LED} = 460 \text{ nm}$ $\lambda_{LED} = 740 \text{ nm}$ $\lambda_{LED} = 850 \text{ nm}$		0.25 0.5 0.35		A/W A/W A/W
103	$\lambda_{pk}$	Peak Sensitivity Wavelength			680		nm
<b>Photocurrent Amplifiers</b>							
201	Iph()	Permissible Photocurrent Operating Range		0		1120	nA
202	$\eta()$ r	Photo Sensitivity (light-to-voltage conversion ratio)	$\lambda_{LED} = 740 \text{ nm}$		0.3		V/ $\mu$ W
203	Z()	Equivalent Transimpedance Gain	$Z = Vout() / Iph()$	0.7	1.0	1.4	M $\Omega$
204	TCz	Temperature Coefficient of Transimpedance Gain			-0.12		%/°C
205	$\Delta Z()$ pn	Transimpedance Gain Matching	P.. channel vs. corresponding N.. channel	-0.2		0.2	%
206	$\Delta Vout()$ pn	Signal Matching	no illumination; any output vs. any output P.. output vs. corresponding N.. output	-35 -2.5		35 2.5	mV mV
207	fc()hi	Cut-off Frequency (-3 dB)			400		kHz
208	VNoise()	RMS Output Noise	illuminated to 500 mV signal level above dark level, 500 kHz band width		0.5		mV
<b>Signal Outputs</b>							
301	Vout()mx	Permissible Max. Output Voltage	refer to Figure 1	2.0			V
302	Iout()mx	Permissible Max. Load Current		-100		250	$\mu$ A
303	Vout()d	Dark Signal Level	no illumination, I() $\leq$ 50 $\mu$ A	575	770	1000	mV
304	Isc()hi	Short-Circuit Current hi	load current to ground	100	420	1300	$\mu$ A
305	Isc()lo	Short-Circuit Current lo	load current to IC	250	480	700	$\mu$ A
306	Ri()	Internal Output Resistance	f = 1 kHz	70	110	180	$\Omega$
307	ton()	Power-On Settling Time	VCC = 0 V $\rightarrow$ 5 V			100	$\mu$ s
<b>Reference Voltage VREF</b>							
401	VREF	Reference Voltage	I(VREF) = -100...+300 $\mu$ A	575	770	1000	mV
402	dVout()	Load Balancing	I(VREF) = -100...+300 $\mu$ A	-10		+10	mV
403	Isc()hi	Short-Circuit Current hi	load current to ground	200	420	2000	$\mu$ A
404	Isc()lo	Short-Circuit Current lo	load current to IC	0.5	4.5	10	mA
<b>Device Specific: iC-PN1864</b>							
V101	Aph()	Radiant Sensitive Area	chip release Y chip release X		0.065 0.034		mm <sup>2</sup> mm <sup>2</sup>
V102	E()mxr	Irradiance For Max. Signal Level	$\lambda_{LED} = 740 \text{ nm}$ , Vout() not saturated; chip release Y  chip release X		12 23		mW/ cm <sup>2</sup> mW/ cm <sup>2</sup>



# iC-PN Series

## PHASED ARRAY NONIUS ENCODERS



Rev F2, Page 9/16

### ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 4.1...5.5 V, Tj = -40..125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min. Typ. Max.			Unit
				Min.	Typ.	Max.	
<b>Device Specific: iC-PN1856</b>							
V201	Aph()	Radiant Sensitive Area	chip release Y chip release X		0.038 0.050		mm <sup>2</sup> mm <sup>2</sup>
V202	E()mxr	Irradiance For Max. Signal Level	$\lambda_{LED} = 740 \text{ nm}$ , Vout() not saturated; chip release Y  chip release X		20 15		mW/ cm <sup>2</sup> mW/ cm <sup>2</sup>
<b>Device Specific: iC-PN2656</b>							
V301	Aph()	Radiant Sensitive Area	chip release Z chip release Y1, Y1H		0.11 0.12		mm <sup>2</sup> mm <sup>2</sup>
V302	E()mxr	Irradiance For Max. Signal Level	$\lambda_{LED} = 740 \text{ nm}$ , Vout() not saturated; chip release Z  chip release Y1, Y1H		6.4 4.6		mW/ cm <sup>2</sup> mW/ cm <sup>2</sup>
<b>Device Specific: iC-PN2612</b>							
V401	Aph()	Radiant Sensitive Area	chip release Z chip release Y1		0.08 0.13		mm <sup>2</sup> mm <sup>2</sup>
V402	E()mxr	Irradiance For Max. Signal Level	$\lambda_{LED} = 740 \text{ nm}$ , Vout() not saturated; chip release Z  chip release Y1		8.0 4.4		mW/ cm <sup>2</sup> mW/ cm <sup>2</sup>
<b>Device Specific: iC-PN2624</b>							
V501	Aph()	Radiant Sensitive Area	chip release Z chip release Y1 chip release X		0.1 0.07 0.06		mm <sup>2</sup> mm <sup>2</sup> mm <sup>2</sup>
V502	E()mxr	Irradiance For Max. Signal Level	$\lambda_{LED} = 740 \text{ nm}$ , Vout() not saturated; chip release Z  chip release Y1  chip release X		6.5 11.0 13.0		mW/ cm <sup>2</sup> mW/ cm <sup>2</sup> mW/ cm <sup>2</sup>
<b>Device Specific: iC-PN3356</b>							
V601	Aph()	Radiant Sensitive Area	chip release Z chip release Y		0.08 0.10		mm <sup>2</sup> mm <sup>2</sup>
V602	E()mxr	Irradiance For Max. Signal Level	$\lambda_{LED} = 740 \text{ nm}$ , Vout() not saturated; chip release Z  chip release Y		8.0 6.5		mW/ cm <sup>2</sup> mW/ cm <sup>2</sup>
<b>Device Specific: iC-PN3924</b>							
V901	Aph()	Radiant Sensitive Area	chip release Z chip release Y		0.09 0.11		mm <sup>2</sup> mm <sup>2</sup>
V902	E()mxr	Irradiance For Max. Signal Level	$\lambda_{LED} = 740 \text{ nm}$ , Vout() not saturated; chip release Z  chip release Y		6.4 5.8		mW/ cm <sup>2</sup> mW/ cm <sup>2</sup>

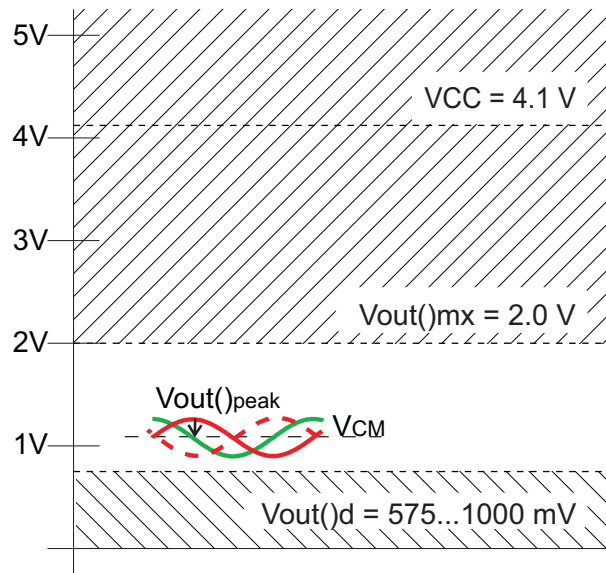


Figure 1: Permissible maximum output voltage range and example of typical output voltage.

# iC-PN Series

## PHASED ARRAY NONIUS ENCODERS



Rev F2, Page 11/16

### DEVICE OVERVIEW

Device	CPR Master	Code Disc P/O Code	Material	OR <sup>1</sup> [mm]	Code Radius begin / end [mm]	Resol. <sup>2</sup> [bit]	Error Tol. <sup>3</sup> [el.deg.]
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#### ∅ 18 Series (disc diameter 18 mm, bore hole 3.0 mm)

iC-PN1864	64	LSHC16S 18-64N	glass	6.905	5.3 / 8.4	19	± 19.6
iC-PN1856	256	LSHC15S 18-256N	glass	6.905	5.3 / 8.4	21	± 9.8

#### ∅ 26 Series (disc diameter 26.0 mm, bore hole 11.6 mm)

iC-PN2656	256	LSHC4S 26-256N	glass	10.905	9.3 / 12.5	21	± 9.8
iC-PN2612	512	LSHC11S 26-512N	glass	10.905	9.3 / 12.5	22	± 4.9
iC-PN2624	1024	LSHC1S 26-1024N	glass	10.905	9.3 / 12.5	23	± 4.9

#### H-Series (disc diameter 26.0 mm, bore hole 11.6 mm)

iC-PNH2628 <sup>4</sup>	2x64	PNH6S 26-128	glass	10.905	9.4 / 12.4	20	± 19.6
iC-PNH2612 <sup>4</sup>	2x256	PNH3S 26-512	glass	10.905	9.4 / 12.4	22	± 9.8
iC-PNH2624 <sup>4</sup>	2x512	PNH5S 26-1024	glass	10.905	9.4 / 12.4	23	± 4.9

#### ∅ 33 Series (disc diameter 33.0 mm, bore hole 18.0 mm)

iC-PN3356	256	LSHC13S 33-256N	glass	14.5	12.9 / 16.1	21	± 9.8
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#### H-Series (disc diameter 33.2 mm, bore hole 18.0 mm)

iC-PNH3312 <sup>4</sup>	2x256	PNH2S 33-512	glass	14.5	13.0 / 16.0	22	± 9.8
iC-PNH3348 <sup>5</sup>	2x1024	PNH1S 33-2048	glass	14.5	13.0 / 16.0	24	± 4.9

#### ∅ 39 Series (disc diameter 39.0 mm, bore hole 13.0 mm)

iC-PN3924	1024	LSHC12S 39-1024N	glass	17.5	15.9 / 19.1	23	± 4.9
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#### H-Series (disc diameter 39.0 mm, bore hole 18.0 mm)

iC-PNH3912 <sup>4</sup>	2x256	PNH8S 39-512	glass	17.5	16.0 / 19.0	22	± 4.9
iC-PNH3948 <sup>4</sup>	2x1024	PNH4S 39-2048	glass	17.5	16.0 / 19.0	24	± 4.9

<sup>1</sup> Optical center radius.

<sup>2</sup> Angle resolution per single turn; interpolated by iC-MN with 13 bit resolution.

<sup>3</sup> Permissible maximum track-to-track phase deviation in electrical degree per master signal cycle.

<sup>4</sup> Refer to iC-PNH Series datasheet available separately.

<sup>5</sup> Refer to iC-PNH3348 datasheet available separately. **EncoderBlue®** is a trademark of iC-Haus GmbH. Device availability on request.

Table 1: Device overview

### APPLICATION CIRCUITS

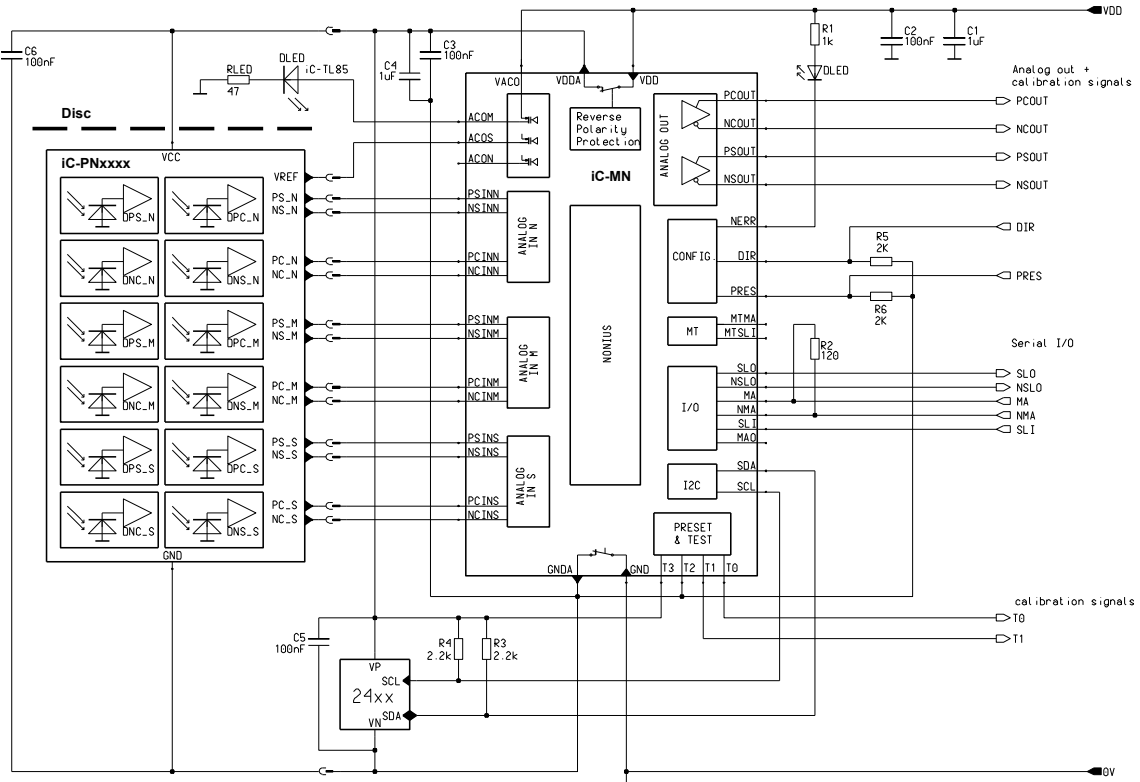


Figure 2: Application example of absolute encoder circuit.

### DESIGN REVIEW: Notes On Chip Functions

iC-PNxxxx .		
No.	Function, Parameter/Code	Description and Application Hints
1		Refer to former datasheet releases.

Table 2: Notes on chip functions regarding iC-PNxxxx chip releases O.

iC-PNxxxx Z		
No.	Function, Parameter/Code	Description and Application Hints
1		Changes to Elec. Char. are documented by this datasheet release, including the extension of operating voltage down to 4.1 V (safe by design).

Table 3: Notes on chip functions regarding iC-PNxxxx chip release Z.

iC-PNxxxx Y1, Y1H, Y2		
No.	Function, Parameter/Code	Description and Application Hints
1	<i>HD Phased Array</i>	Chip release utilizes a high definition phased array layout.

Table 4: Notes on chip functions regarding iC-PNxxxx chip release Y1, Y1H, Y2.

iC-PNxxxx X		
No.	Function, Parameter/Code	Description and Application Hints
1	<i>HD Phased Array</i>	Chip release utilizes a high definition phased array layout. Thickness of glass lid reduced to 200 µm.

Table 5: Notes on chip functions regarding iC-PNxxxx chip release X.

# iC-PN Series

## PHASED ARRAY NONIUS ENCODERS



Rev F2, Page 14/16

### REVISION HISTORY

Rel.	Rel. Date <sup>1</sup>	Chapter	Modification	Page
A1	2008	...	Initial introduction.	

Rel.	Rel. Date <sup>1</sup>	Chapter	Modification	Page
E1	2017-02-08	...	New datasheet for iC-PN chip series	all

Rel.	Rel. Date <sup>1</sup>	Chapter	Modification	Page
E2	2017-11-21	ELECTRICAL CHARACTERISTICS	Minor adaption of IC test limits: Item 304: max. limit 1300 µA, item 403: max. limit 2000 µA Items V501, V502: chip release X added to iC-PN2624	8

Rel.	Rel. Date <sup>1</sup>	Chapter	Modification	Page
E3	2018-08-17	DESCRIPTION	Obsolete devices removed (iC-PN3312, iC-PN3324)	2
		PACKAGING INFORMATION	Pad layout updated.	2
		ELECTRICAL CHARACTERISTICS	Item 102: condition added, limits adapted Item 301: comment added, and Figure 1 added	8
		DEVICE OVERVIEW	Footnote added on obsolete devices.	11
		DESIGN REVIEW	Chip release Y2 added	13
		ORDERING INFORMATION	Obsolete devices removed.	16

Rel.	Rel. Date <sup>1</sup>	Chapter	Modification	Page
E4	2020-03-02	PACKAGING INFORMATION	AOI criteria added	3
		ORDERING INFORMATION	Eval board added for iC-PN3356	16

Rel.	Rel. Date <sup>1</sup>	Chapter	Modification	Page
E5	2020-06-16	DESCRIPTION	iC-PN18xx: preliminary marking removed	2
		DEVICE OVERVIEW	Listing and footnote 5 updated	11
		ORDERING INFORMATION	Listing updated	16

Rel.	Rel. Date <sup>1</sup>	Chapter	Modification	Page
F1	2021-04-15	PACKAGING INFORMATION	Update of footnote: hyperlink to customer information	3
		PACKAGE DIMENSIONS	Update of package drawing and footnote, drawing added for chip release X	5, 6
		THERMAL DATA	Item T03: hyperlink to customer information	7
		ELECTRICAL CHARACTERISTICS	Items V101, V102, V201, V202 (iC-PN18xx): chip release X added	8

Rel.	Rel. Date <sup>1</sup>	Chapter	Modification	Page
F2	2021-09-27	ELECTRICAL CHARACTERISTICS	Item 003: correction of condition and limits Item V301, V302: chip release Y1H added	8
		DESIGN REVIEW	Inclusion of chip release Y1H. Table of chip release X separated and updated for clarity.	13

<sup>1</sup> Release Date format: YYYY-MM-DD

# iC-PN Series

## PHASED ARRAY NONIUS ENCODERS



Rev F2, Page 15/16

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# iC-PN Series

## PHASED ARRAY NONIUS ENCODERS



Rev F2, Page 16/16

### ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-PNxxxx	15-pin optoBGA, 6.2 mm x 5.2 mm, thickness 1.7 mm RoHS compliant	xxxx = device version	iC-PNxxxx oBGA LSH2C
	32-pin optoQFN, 5 mm x 5 mm, thickness 0.9 mm RoHS compliant	xxxx = device version	iC-PNxxxx oQFN32-5x5
Code Disc	Glass disc 1.0 mm	nn = design number aa = diameter cc...cccc = master track CPR	LSHCnnS aa-ccccN
		for iC-PN1864 (64 CPR)	LSHC16S 18-64N
		for iC-PN1856 (256 CPR)	LSHC15S 18-256N
		for iC-PN2656 (256 CPR)	LSHC4S 26-256N
		for iC-PN2612 (512 CPR)	LSHC11S 26-512N
		for iC-PN2624 (1024 CPR)	LSHC1S 26-1024N
Evaluation Kit	Kit with Scanner Module IC273 (61 mm x 64 mm), LED Module IC274 and Code Disc	xxxx = device version (availability on request)	iC-PNxxxx EVAL IC273
		for iC-PN2656 (256 CPR), incl. IR LED module (availability on request)	iC-PN2656 EVAL IC273
		for iC-PN3356 (256 CPR), incl. IR LED module (availability on request)	iC-PN3356 EVAL IC273
Illumination	IR LED module (28 mm x 29 mm) Blue LED module (28 mm x 29 mm)	with iC-SD85 (850 nm)	iC-SD85 EVAL IC274
		with iC-TL46 (460 nm)	iC-TL46 EVAL IC274
Mother Board Adapter Board	Adapter PCB (80 mm x 110 mm) Adapter PCB (41 mm x 41 mm), connects IC273 to MN1D	incl. ribbon cable	iC277 EVAL IC277
		incl. ribbon cable	iC306 EVAL IC306

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