iC-MNF EVAL MNF1D
EVALUATION BOARD DESCRIPTION

ORDERING INFORMATION

Type	Order Designation	Description/Options
Evaluation Board	iC-MNF EVAL MNF1D	Evaluation Board Ready-to-operate, accessible by GUI using PC adapter (not included)
Software	iC-MNF GUI	GUI Software for Windows PC Device setup file generation, board configuration via adapter For download link check www.ichaus.com/mnf
	BiSS Reader GUI	GUI software for Windows PC (optional) BiSS device access for data readout and visualization; For download link check www.ichaus.com/software
Related parts	(to be ordered separately)	
PC Adapters	iC-MB5 iCSY MB5U	High-Performance isolated PC-USB Adapter for BiSS C
	iC-MB4 iCSY MB4U	High-Performance PC-USB Adapter for BiSS C
	iC-MB3 iCSY MB3U-I2C	PC-USB Adapter recommended for SPI communication
		Download documentation at www.ichaus.com/tools

BOARD MNF1D

(size 140 mm x 100 mm)

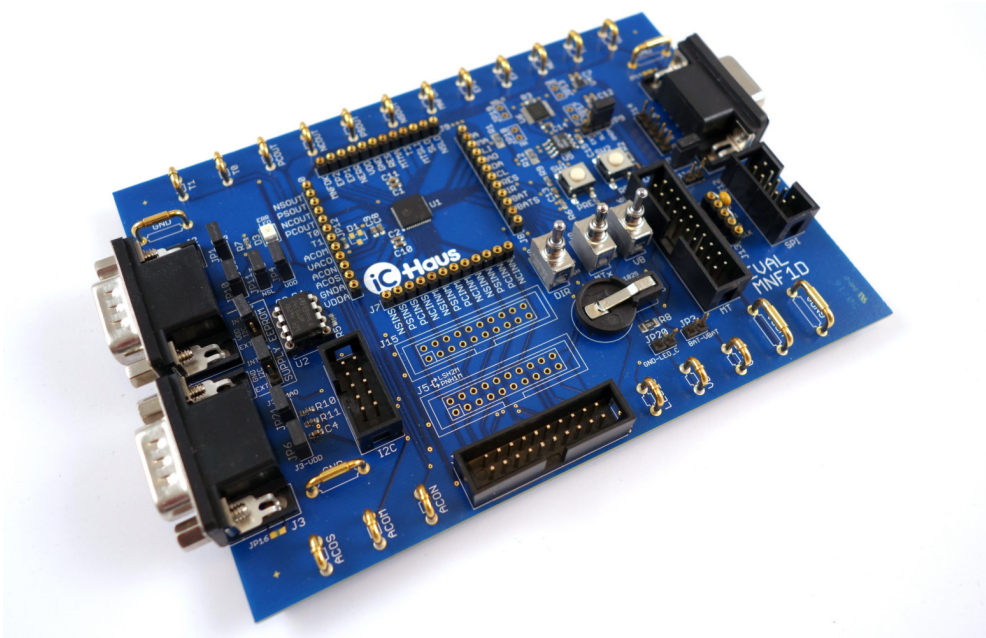

Figure 1: Board MNF1D top view

RELATED PRODUCTS AND DOCUMENTATION

- IC Documentation → http://www.ichaus.de/MNF
- GUI Software (Windows), check for download link at → http://www.ichaus.de/MNF
- BiSS-to-PC Adapter Descriptions
  → http://www.ichaus.de/MB5U_datasheet_en
  → http://www.ichaus.de/MB4U_datasheet_en
  → http://www.ichaus.de/MB3U_datasheet_en

CONNECTORS AND TERMINALS

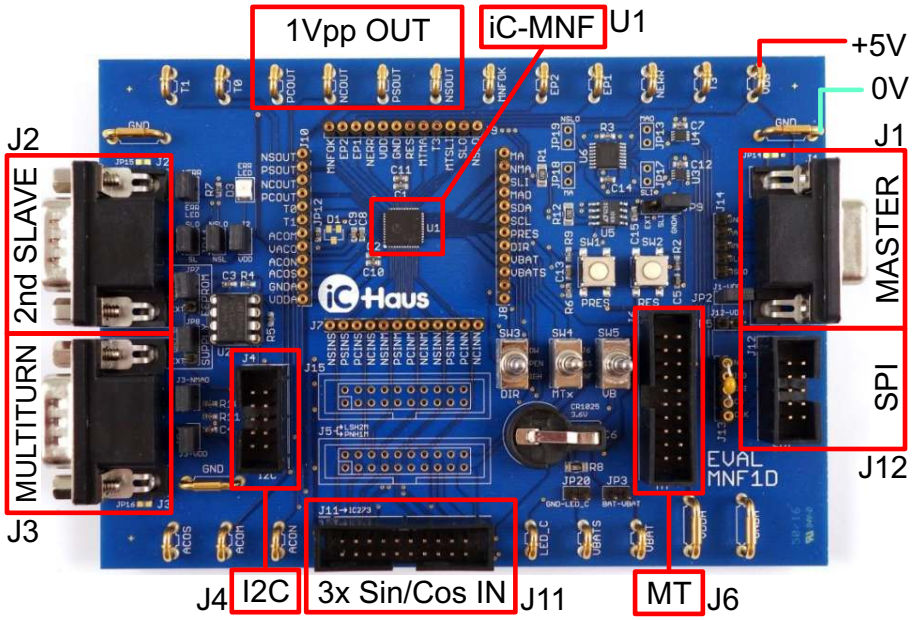

Figure 2: Component side

TERMINALS

Upper side	(from left to right)
GND	0 V Board Ground
T1	Calibration Signal Output
T0	Calibration Signal Output
PCOUT	Analog Output Cosine +
NCOUT	Analog Output Cosine –)
PSOUT	Analog Output Sine +
NSOUT	Analog Output Sine –
MNFOK	MNF OK Output
EP2	General purpose I/O pin 2
EP1	General purpose I/O pin 1
NERR	Error Message Output, System Error Message Input Connected to error LED D3 with JP1 closed.
T3	External Trigger Input
VDD	+5 V Board Supply Voltage Input Approx. 65 mA (no adapter connected); **When powering VDD, open jumpers JP2, JP5.**
GND	0 V Board Ground

Lower side	(from left to right)
ACOS	Signal Level Controller Outp. (Seg.), VREFin Ref. Voltage Input/Output
ACOM	Signal Level Controller Outp. (Master)
ACON	Signal Level Controller Outp. (Nonius)
LED_C	LED Cathode Series resistor (47 Ω) or direct connection to GND is controlled by jumper JP20.
VBATS	Battery Supply Voltage Sensor Output
VBAT	Battery Supply Voltage Input
VDDA	Sub-System Positive Supply Output
GNDA	Sub-System Ground Output

CONNECTORS

J1	BiSS interface to master (to PC adapter) (9-pin D-sub, female) **Do not connect J12 simultaneously.**
J2	BiSS interface to slaves (optional) (9-pin D-sub, male)
J3	Multiturn interface (to BiSS slave) (9-pin D-sub, male) **Use a short cable as there is no RS422 line driver implemented.**
J4	I2C interface (iC-MNF/EEPROM) (10-pin WSL connector, male)
J5	Sin/cos signal interface (e.g. to LSH2M or PNH1M board) (20-pin, male)
J6	Multiturn Interface (20-pin WSL connector, male)
J7 - J10	Pin signals (iC-MNF) (12-pin, female)
J11	Sin/cos signal interface (e.g. to IC273 board family) (20-pin WSL connector, male)
J12	SPI interface (to PC adapter) (10-pin WSL connector, male) **Do not connect J1 simultaneously.**
J13	SPI interface (iC-MNF) (5-pin, female)
J14	BiSS interface (5-pin, male)
J15	Sin/cos signal interface, not connected (e.g. to custom board) (20-pin male)

SWITCHES

PRES	Configurable command Input
RES	Reset input
DIR	Code direction
MTx	MTA, MTB destination (from J5, J11)
VB	VB source (to J5, J11)

PINOUT OF CONNECTORS

J1: BiSS interface to master (to PC adapter)
9-pin D-sub connector, female

Pin	Name	Function
1	n.c.	
2	MA	Clock input
3	NMA	Clock input (inverted)
4	VDD	+5 V supply input **(JP2 closed)**
5	NSLI	Data in / master out (inverted)
6	GND	Ground
7	SL	Data return line
8	NSL	Data return line (inverted)
9	SLI	Data in / master out

J2: BiSS interface to slaves (optional)
9-pin D-sub connector, male

Pin	Name	Function
1	n.c.	
2	MAO	Clock output
3	NMAO	Clock output (inverted)
4	VDD	+5 V supply output
5	NSLO	Data out / slave in (inverted)
6	GND	Ground
7	SL	Data return line
8	NSL	Data return line (inverted)
9	SLO	Data out / slave in

J3: Multiturn interface
9-pin D-sub connector, male

Pin	Name	Function
1	n.c.	
2	MTMA	Clock output
3	NMTMA	Clock output (inverted)
4	MTVDD	+5 V supply output **(JP6 closed)**
5	n.c.	
6	GND	Ground
7	MTSLI	Data input
8	n.c.	
9	n.c.	

J4: I2C Interface (iC-MNF/EEPROM)
10-pin WSL connector, male

Pin	Name	Function
1	SCL	EEPROM interface, clock line
2	GND	Ground
3	n.c.	
4	VDD	+5 V EEPROM supply input **(see JP7)**
5	n.c.	
6	n.c.	
7	SDA	EEPROM interface, data line
8	n.c.	
9	SDA	EEPROM interface, data line
10	GND	EEPROM Ground **(see JP8)**

J5: Sin/cos signal interface (e.g. to LSH2M or PNH1M board)
20-pin

Pin	Name	Function
1	PSINS	Signal input Sine + (Segment)
2	NSINS	Signal input Sine - (Segment)
3	PCINS	Signal input Cosine + (Segment)
4	NCINS	Signal input Cosine - (Segment)
5	PSINM	Signal input Sine + (Master)
6	NSINM	Signal input Sine - (Master)
7	PCINM	Signal input Cosine + (Master)
8	NCINM	Signal input Cosine - (Master)
9	PSINN	Signal input Sine + (Nonius)
10	NSINN	Signal input Sine - (Nonius)
11	PCINN	Signal input Cosine + (Nonius)
12	NCINN	Signal input Cosine - (Nonius)
13	GNDA	Sub-system ground output
14	VDDA	Sub-system positive supply output
15	ACOM	Signal level controller output (Master)
16	LED_C	LED cathode **(see JP20)**
17	ACON	Signal level controller output (Nonius)
18	ACOS	Signal level controller output (Segment), VREFin ref. voltage input/output
19	MTA	iC-PNH dig. output A **(see SW4)**
20	MTB	iC-PNH dig. output B **(see SW4)**

J6: Multiturn interface (e.g. to ext. microcontroller)
20-pin WSL connector, male

Pin	Name	Function
1	VBATS	Battery supply voltage sensor output
2	GNDA	Sub-system ground output
3	MNFOK	MNF OK output
4	MTSLI	Multiturn interface, data input
5	MTMA	Multiturn interface, clock output
6	ACOM	Signal level controller output (Master)
7	MTA_MT	iC-PNH dig. output A **(see SW4)**
8	MTB_MT	iC-PNH dig. output B **(see SW4)**
9	SCL	EEPROM interface, clock line
10	SDA	EEPROM interface, data line
11	VBAT	Battery supply voltage input
12	VBATS_MT	iC-PNH auxiliary supply voltage output **(see SW5)**
13	GNDA	Sub-system ground output
14-20	n.c.	

J7, J8, J9, J10: Pin signals iC-MNF
Connector 12x1 (4x), female

Pin	Name	Function
		Refer to iC-MNF datasheet.

J11: Sin/cos signal interface (e.g. to iC-PNHnnnn EVAL IC273)
20-pin WSL connector, male

Pin	Name	Function
1	NCINS	Signal input Cosine - (Segment)
2	PCINS	Signal input Cosine + (Segment)
3	NCINM	Signal input Cosine - (Master)
4	PCINM	Signal input Cosine + (Master)
5	NCINN	Signal input Cosine - (Nonius)
6	PCINN	Signal input Cosine + (Nonius)
7	MTB	iC-PNH dig. output B **(see SW4)**
8	GNDA	Sub-system ground output
9	MTA	iC-PNH dig. output A **(see SW4)**
10	VB	iC-PNH auxiliary supply voltage output **(see SW5)**
11	VDDA	Sub-system positive supply output
12	ACOS	Signal level controller output (Segment), VREFin ref. voltage input/output
13	PSINN	Signal input Sine + (Nonius)
14	NSINN	Signal input Sine - (Nonius)
15	PSINM	Signal input Sine + (Master)
16	NSINM	Signal input Sine - (Master)
17	PSINS	Signal input Sine + (Segment)
18	NSINS	Signal input Sine - (Segment)
19	LED_C	LED cathode **(see JP20)**
20	ACOM	Signal level controller output (Master)

J12: SPI interface (to PC Adapter)
10-pin WSL connector, male

Pin	Name	Function
1	SCLK	Serial clock input
2	n.c.	
3	EN_SPI	Enable I2C access through J12
4	VDD	+5 V supply input (JP5 closed)
5	n.c.	
6	n.c.	
7	MOSI	Master output, slave input
8	NCS	Chip select input, low active
9	MISO	Master input, slave output
10	GND	Ground

J13: SPI interface (iC-MNF)
5-pin, female

Pin	Name	Function
1	SCLK	Serial clock input
2	NCS	Chip select input, low active
3	MOSI	Master output, slave input
4	MISO	Master input, slave output
5	GND	Ground

J14: BiSS interface (for debugging)
5-pin, male

Pin	Name	Function
1	GND	Ground
2	MA	Clock input
3	NMA	Clock input (inverted)
4	SL	Data return line
5	NSL	Data return line (inverted)

J15: Sin/cos signal interface (e.g. to custom board)
20-pin

Pin	Name	Function
1-20	n.c.	

DESCRIPTION OF JUMPERS

OVERVIEW

JP1	NERR input/output to error LED D3
JP2	Board supply by BiSS master (J1)
JP3	VBAT supply by C6 (CR1025 battery)
JP4	Board supply to BiSS slaves (J2)
JP5	Board supply by SPI (J12)
JP6	Board supply to multiturn interface (J3)
JP7	EEPROM supply selector
JP8	EEPROM ground selector
JP9	SLI input selector
JP10	Data return link SL
JP11	Data return link NSL
JP12	ACOM solder option
JP13, JP17, JP18, JP19	BiSS/SPI separators
JP14	BiSS master (J1) shield to GND
JP15	BiSS slaves (J2) shield to GND
JP16	Multiturn interface (J3) shield to GND
JP20	LED cathode to GND
JP21	Multiturn interface (J3) MTMAO threshold to 1/2 VDD

Default	**Default settings are highlighted.**

Jumper JP1	**Function**
Closed	NERR input/output connected to error LED D3.
Open	Error LED D3 unconnected, no pull-up action on NERR.

Jumpers JP2, JP4, JP5, JP6	**Function**
JP2 closed	Board supplied by BiSS connector J1.
JP4 closed	BiSS slaves supplied by VDD.
JP5 closed	Board supplied by SPI connector J12.
JP6 closed	Multiturn sensor at J3 supplied by VDD.

Jumper JP3	**Function**
Closed	VBAT supplied by C6 (CR1025 battery).
Open	VBAT supplied by VBAT terminal or J6.

Jumpers JP7, JP8	**Function**
1-2 (down)	EEPROM supplied from external (J4).
2-3 (top)	EEPROM supplied from internal (VDDA, GNDA).

Jumper JP9	**Function**
1-2 (right)	SLI input set to GNDA.
2-3 (left)	SLI input connected to BiSS in (J1).

Jumpers JP10, JP11	**Function**
Closed	Normal operation: iC-MNF data output SLO/NSLO replies to the BiSS return lines (SL/NSL).
Open	Daisy chain operation: The BiSS slave connected at J3 replies to the BiSS return lines.

Solder option JP12	**Function**
Assembled	Direct connection from iC-MNF ACOM to J5, J11.

Jumpers JP13, JP17, JP18, JP19	**Function**
Closed	MAO, SLI, NSLO, SLO directly connected to J1/J2. SPI (J12) disabled.
Open	MAO, SLI, NSLO, SLO connected to J1/J2 by switch U6 and buffers U3, U4. SPI (J12) possible.

Solder option JP14, JP15, JP16	**Function**
JP14 closed (n.a.)	BiSS master (J1) shield connected to GND.
JP15 closed (n.a.)	BiSS slaves (J2) shield connected to GND.
JP16 closed (n.a.)	Multiturn interface (J3) shield connected to GND.
Note	n.a. = not assembled

Jumper JP20	**Function**
Closed	LED cathode (LED_C) directly connected to GND.
Open	LED cathode (LED_C) connected to GND via series resistor (R8 = 47 Ω).

Jumper JP21	**Function**
Closed	Multiturn interface (J3) MTNMAO = 1/2 VDD (MTMAO threshold).
Open	Multiturn interface (J3) MTNMAO floating.

DESCRIPTION OF SWITCHES

Default	Default settings are highlighted.

Switch SW1: PRES	Function
Pressed	PRES triggered: iC-MNF configurable command input.

Switch SW2: RES	Function
Pressed	RES triggered: iC-MNF reset input.

Switch SW3: DIR	Function
Top	DIR = low: Code direction normal.
Middle	DIR = open: Code direction normal (internal pull-down resistor).
Down	DIR = high: Code direction inverted.

Switch SW4: MTx (x = A, B)	Function
Top	MTx = MTA_MT, MTB_MT: MTx from sin/cos signal interface (J5, J11) to multiturn interface, ext. micro-controller (J6).
Middle	MTx = open.
Down	MTx = MTMA, MTSLI: MTx from sin/cos signal interface (J5, J11) to iC-MNF.

Switch SW5: VB	Function
Top	VB = VBATS_MT: VB from multiturn interface, ext. micro-controller (J6) to sin/cos signal interface (J5, J11).
Middle	VB = open.
Down	VB = VBATS: VB from iC-MNF (VBATS) to sin/cos signal interface (J5, J11).

CIRCUIT SCHEMATIC

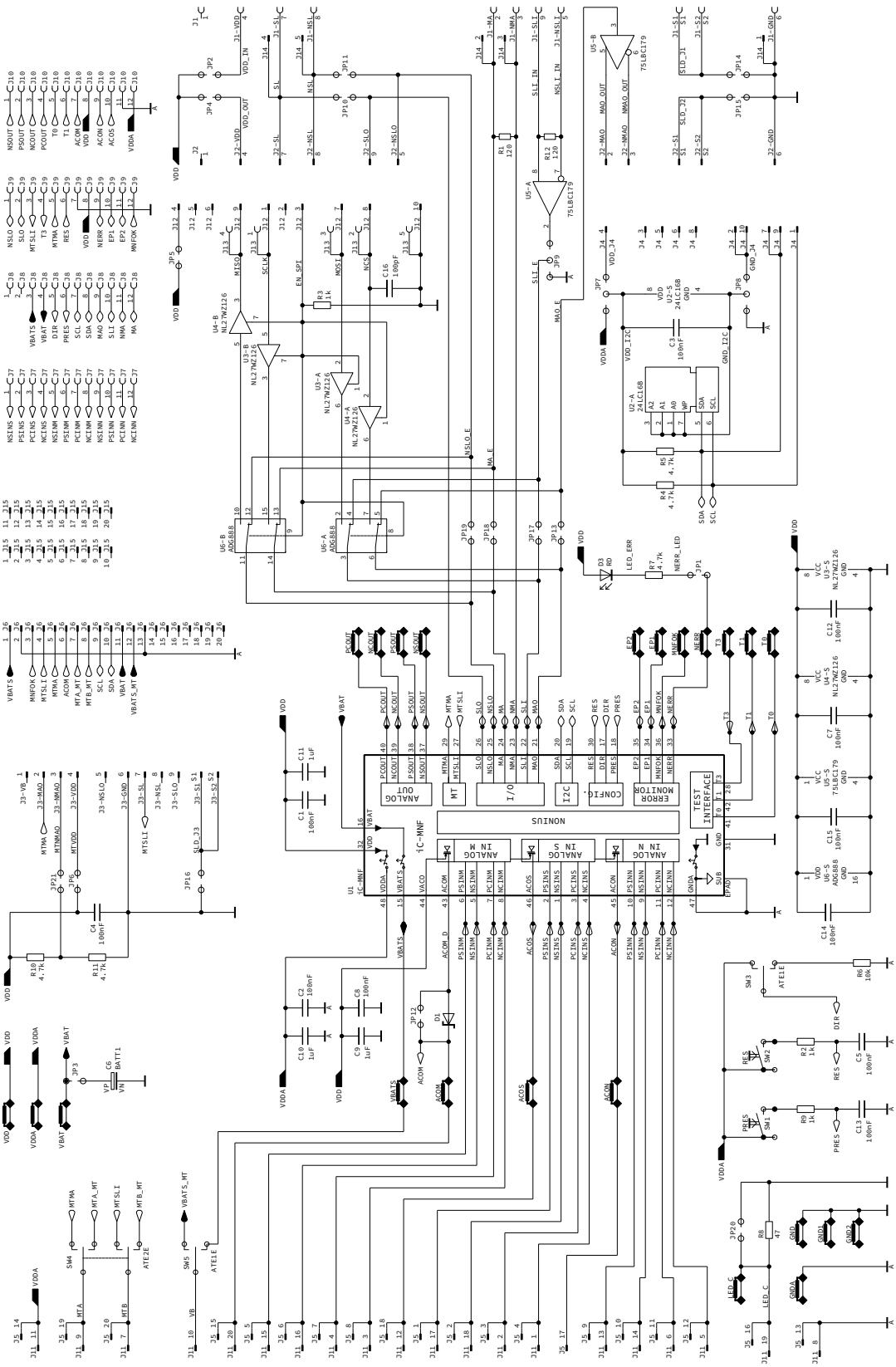

Figure 3: Circuit diagram.

BOARD LAYOUT

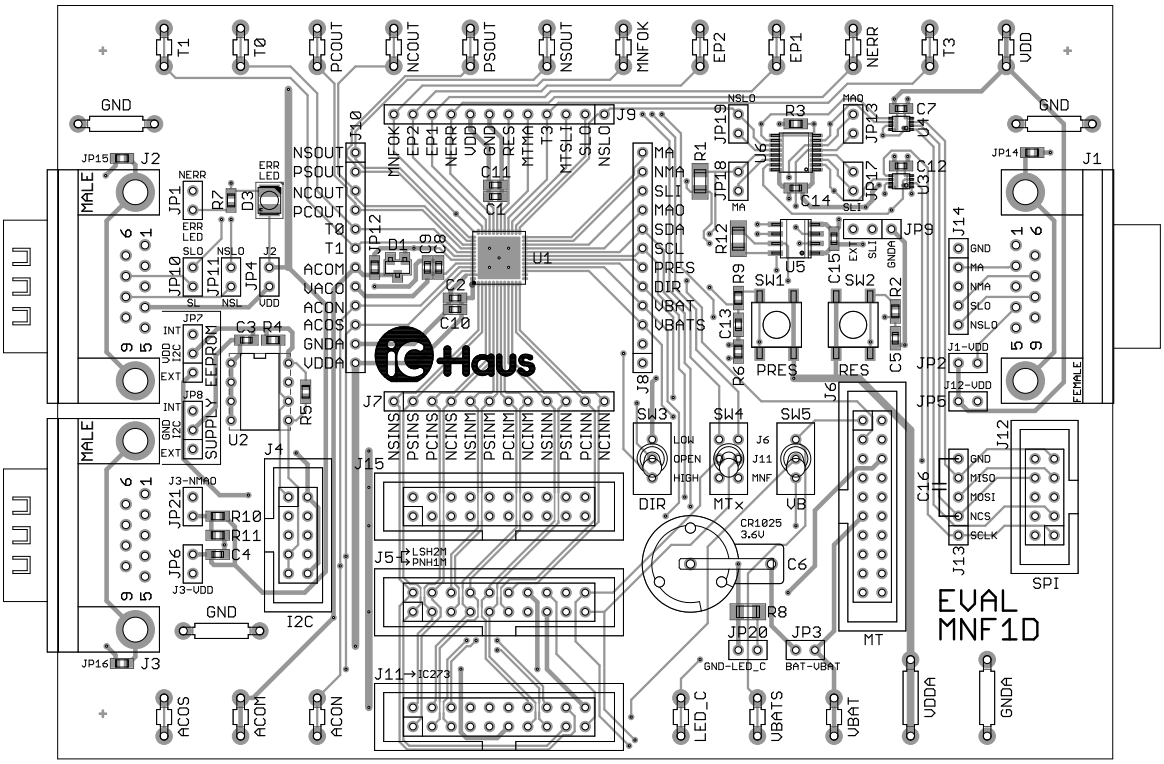

Figure 4: Board MNF1D (top side)

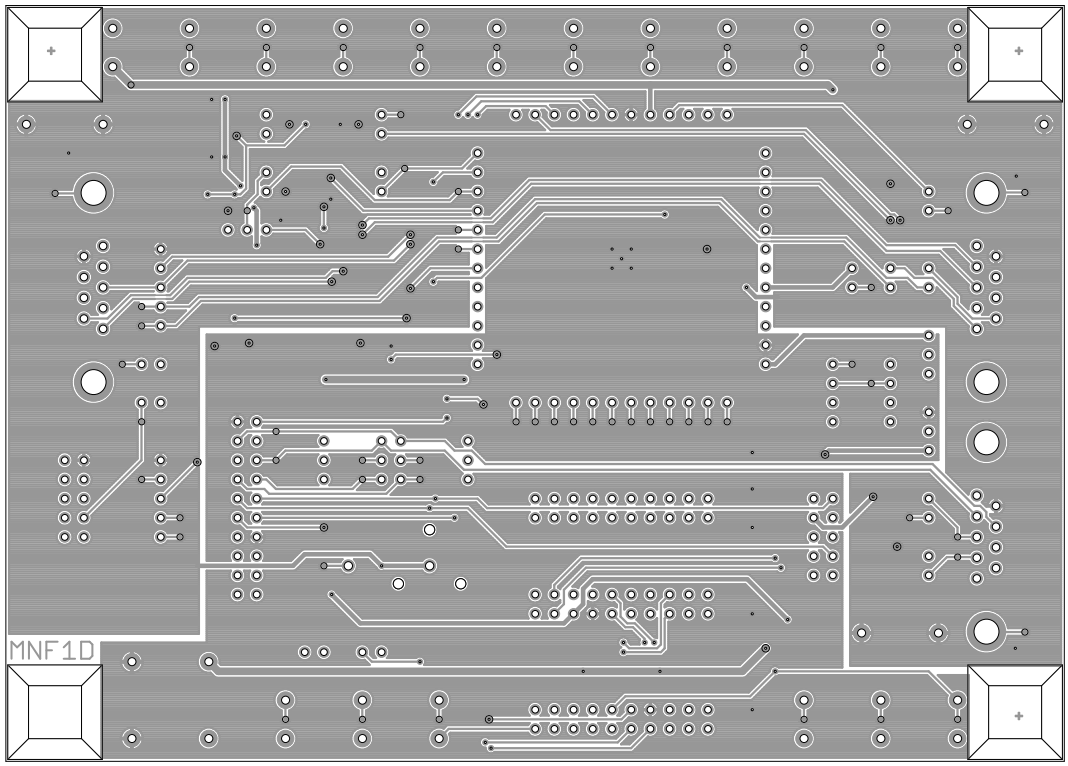

Figure 5: Board MNF1D (bottom side)

ASSEMBLY PARTS LIST

Components (top)	Typical Value	Comment
C1, C2, C3, C4, C5, C7, C8, C12, C13, C14, C15	100 nF, 10 %, X7R 16 V	
C6	CR1025 3.6 V	Coin cell holder
C9, C10, C11	1 µF, 20 %, X5R 6.3 V	
C16	100 pF	Capacitor between SPI line NCS and GND
D1 D3	n.a. LED red	 Error LED
J1 J2, J3 J4, J12 J6, J11 J7, J8, J9, J10 J13 J14	D-sub 9-pole, female D-sub 9-pole, male WSL10G (2x5-pin male) WSL20G (2x10-pin male) S12X1 W6X1 W6X1	BiSS interface (to master) BiSS interface (to slaves), multiturn interface SPI interface Multiturn interface, sin/cos signal interface Pin signals iC-MNF SPI interface (iC-MNF) BiSS interface (for debugging)
JP1 ... JP6, JP10, JP11, JP14, JP15, JP16, JP17, JP20, JP21 JP13, JP17, JP18, JP19 JP7, JP8, JP9 JP12	W2X1 n.a. W3X1 0 Ω	Jumpers Jumpers Jumpers ACOM reverse current prevention
R1, R12	120 Ω	Line termination
R2, R3, R9	1 kΩ, 1 %	
R5, R6, R7	120 Ω	Line termination
R4, R5, R7, R10, R11	4.7 kΩ, 1 %	
R6	10 kΩ, 1 %	
R8	47 Ω, 1 %	LED series resistor
SW1, SW2	B3S 1000	Preset button, reset button
SW3, SW5	ATE1E	Code direction, VB source
SW4	ATE2E	MTA, MTB destination setting
U1	iC-MNF (QFN48-7x7)	Interpolation IC
U2	24LC16B (DIL8)	16 Kbit serial I^2C EEPROM
U3, U4 U5 U6	NL27WZ126 (VSOP8) LTC490 (SO8) ADG888 (TSSOP16)	Buffer (2x) Driver (2x) Switch (4x)
Note	n.a. = not assembled	

FUNCTION NOTES

Note: When using the multiturn interface (J3), be aware that there is no differential transmission. Use a short cable as there is no RS422 line driver implemented on the evaluation board.

Note: When using the multiturn interface (J3), set a 1/2 VDD center potential using JP21, if the multiturn slave expects a differential clock.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2019-04-12	All	Initial release	

* Release Date format: *YYYY-MM-DD*