

# iC-ML EVAL ML1D

## EVALUATION BOARD DESCRIPTION



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### ORDERING INFORMATION

Type	Order Designation	Description/Options
iC-ML Evaluation Board	ML1D EVAL	Evaluation board for iC-ML with magnetic scale

### BOARD ML1D

(size 100 mm x 80 mm)

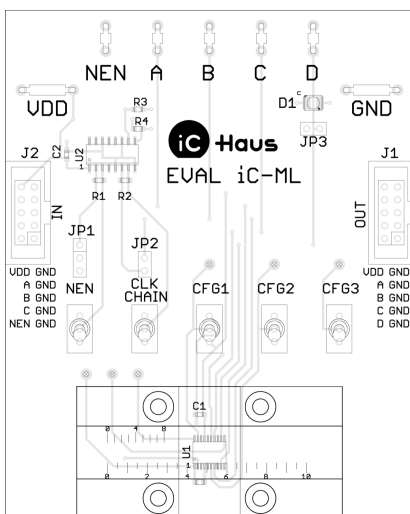


Figure 1: Component side of ML1D board

### TERMINAL DESCRIPTIONS

Name	Function
VDD	Supply Voltage
NEN	Not Enable
A	Port A
B	Port B
C	Port C
D	Port D
GND	Ground
CFG1	Configuration Input 1
CFG2	Configuration Input 2
CFG3	Configuration Input 3

### DESCRIPTION

PROJECT	REV	BLOCK	TITLE
ML1D	-	0	Demoboard

DESIGN CONTEXT	SHEET	TICKET	DATE	EDITION	VIS
S:\ml\pcb\ml1d\ml1d_060905r\pcb_des\en_v01	1		13.07.2007	1	BB

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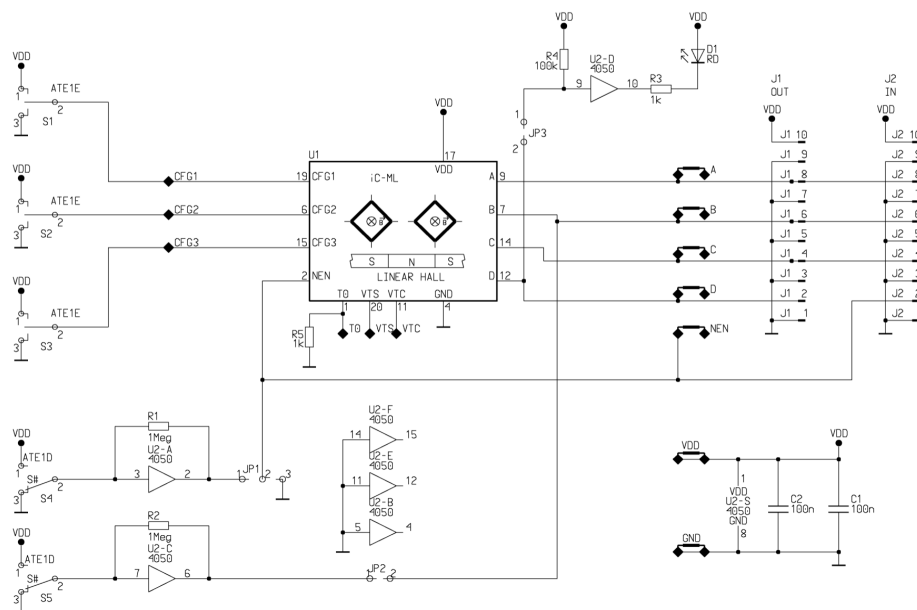


Figure 2: Schematic diagram of ML1D board

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### ASSEMBLY PART LIST

Device	Value (typ)	Comment
C1	100 nF	blocking capacitor
C2	100 nF	blocking capacitor
D1	SMD-LED	indicator lamp for Port D output of iC-ML
R1	1 M $\Omega$	feedback resistor
R2	1 M $\Omega$	feedback resistor
R3	1 K	current limiting resistor
R4	100 k $\Omega$	pull-up resistor
R5	1 K	pulldown resistor
U1	CD 4050	hex CMOS inverter, for debouncing switches S4 and S5 and driving indicator lamp D1
U2	iC-ML	hall sensor/encoder
J1	10 pin	output connector for cascading multiple demo boards
J2	10 pin	input connector for cascading multiple demo boards
JP1	jumper	connects S4 with NEN input; remove this jumper in chain modes when this board is not the first in a chain
JP2	jumper	connects S5 with CLK input in chain modes; used only in one board of a chain, remove on the rest
JP3	jumper	connects PORT D to indicator; remove this jumper to check tristate condition
S1	key switch	CFG1 level (high, open, low)
S2	key switch	CFG2 level (high, open, low)
S3	key switch	CFG3 level (high, open, low)
S4	key switch	NEN level (high, low)
S5	key switch	CLK level (high, low) (Port B of iC-MA when used in chain operation mode; otherwise remove jumper JP2)

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