iC-ME

DUAL LIGHT-GRID PULSE RECEIVER

preliminary

FEATURES

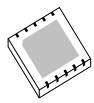
- Dual photo diode inputs with photoelectric amplifier
- Built-in bandpass filter with 300 kHz center frequency
- Differential current-signal output with open drain low-side drivers
- Nonlinear transfer function results in wide dynamic range of 100 nA to 1.5 mA for pulsed photocurrents
- Fast flash recovery time of max. 30 µs
- Recovery time below 10 µs for excessive photocurrents of up to 1.8 mA
- Shift register and control logic
- Compatible to CMOS levels
- Single 5 V supply
- Low standby current; circuit activation by input data
- Power-down reset
- ESD protection
- FMEA driven circuit and layout topology
- Suited for high-risk applications according to IEC 61496-1

Option: extended temperature range of -25 to 85 °C

APPLICATIONS

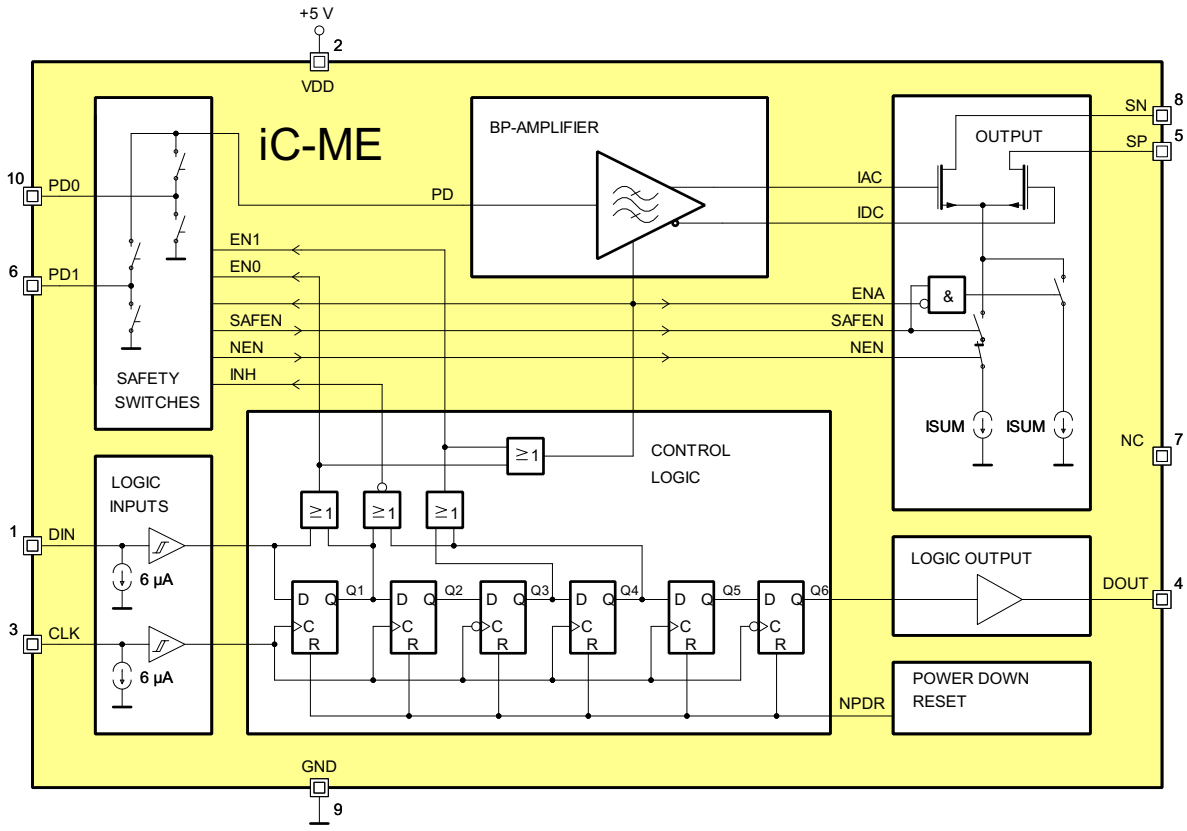
- Light curtains
- Light barriers
- Electro-sensitive protective equipment (ESPE)

PACKAGES



DFN10 4 mm x 4 mm

BLOCK DIAGRAM



DESCRIPTION

The iC-ME device is a dual light chain receiver IC. Typical applications cover light curtains, light barriers and electro-sensitive protective equipment in general.

Integrated on a single chip the iC-ME contains a bandpass amplifier with a center frequency of typically 300 kHz, a differential current output plus control logic to activate the amplifier and the output. Deactivated, the current consumption is very low and the current outputs SN and SP are switched to high impedance (zero current).

The control logic of the two cascaded channels consists of a three-stage shift register each, in which the first respective two flip-flops are triggered by the leading edge and the third flip-flop by the trailing edge of the clock input CLK. This produces an artificial delay in order to avoid race conditions when shifting the input from channel 0 to channel 1 and via the serial output to the next device in the chain.

The bandpass amplifier is activated when DIN reads a logical '1'. The current output still remains disabled (zero current) until the output of the first resp. forth flip-flop of the *Control Logic* changes to '1'. This activates the bias for the complete signal path from light detection to the differential current output. The differential outputs SP and SN are powered up to an equal current, as far as the attached photodiode does not receive any changes in light.

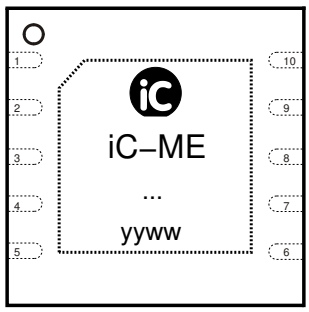
The leading edge of a received light pulse (which produces an increase of photocurrent), causes the output current at SP to increase and at SN to decrease by an equal value. The sum of I(SP) + I(SN) is kept constant. For light curtain applications in which only one device is activated at a time, the outputs SN and SP can be attached to a two-wire bus.

The amplifier and output automatically return to standby after processing the serial input data at DIN, whith the *Control Logic* receiving the fourth leading CLK edge. Therefore, a chain circuitry with multiple beams can be set up with just a single data bit within a shift cycle.

The IC contains protective diodes to prevent destruction by ESD. Control logic input pins feature Schmitt-trigger characteristics for high noise immunity. All pins are short-circuit proof.

PACKAGING INFORMATION DFN10 to JEDEC Standard

PIN CONFIGURATION DFN10



PIN FUNCTIONS

No.	Name	Function
1	DIN	Data Input
2	VDD	+5 V Supply Voltage
3	CLK	Clock Input
4	DOUT	Data Output
5	SP	Pos. Differential Current Output
6	PD1	Photo Diode #1, Input Cathode
7	n.c.	
8	SN	Neg. Differential Current Output
9	GND	Ground
10	PD0	Photo Diode #0, Input Cathode

Orientation of the package label (iC *iC-ME ... yyww*) may vary!

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.5	7	V
G002	V()	Voltage at DIN, CLK, DOUT, SN, SP, PD		-0.5	VDD + 0.5	V
G003	Vd()	ESD Susceptibility at DIN, CLK, DOUT, PD, SN, SP	HBM, 100 pF discharged through 1.5 kΩ		4	kV
G004	Tj	Junction Temperature		-40	150	°C
G005	Ts	Storage Temperature		-40	150	°C

THERMAL DATA

Operating Conditions: VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended temperature range of -25 to 85 °C on request)		0		70	°C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 5 V ±10 %, V(SN, SP) = 3.5 V...VDD, Tj = -25...85 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage Range		4.5		5.5	V
002	VDD	Required Supply Voltage for logic function	decreasing voltage VDD	1.7			V
003	I(VDD)	Supply Current in VDD (Standby)	DIN = lo, CLK = hi or lo: BP-amplifier and output stage disabled, logic levels: lo = 0...0.45 V, hi = VDD − 0.45 V...VDD			60	µA
004	I(VDD)	Supply Current in VDD	EN = hi: BP-amplifier activated, INH = hi: output stage disabled, I(PD) = -15...0 µA Tj = 27 °C		 0.3	0.5	mA mA
005	I(VDD)	Supply Current in VDD	EN = hi, INH = lo: BP-amplifier and output stage activated Tj = 27 °C		 1.1	3.0	mA mA
006	VDDon	Turn-on Threshold VDD (Power-on release)				4.2	V
007	VDDoff	Undervoltage Threshold at VDD (Power-down reset)	decreasing voltage VDD	2.6			V
008	VDDhys	Hysteresis	VDDhys = VDDon − VDDoff	200		500	mV
009	Vc()hi	Clamp Voltage hi at DIN, CLK, DOUT, PD, SN, SP	Vc()hi = V() − VDD, I() = 10 mA	0.4		1.25	V
010	Vc()lo	Clamp Voltage lo at DIN, CLK, DOUT, PD, SN, SP	I() = -10 mA, VDD = 0 V, other pins open	-1.25		-0.4	V
Bandpass Amplifier and Output Stage PD0, PD1, SN, SP							
101	C(PD)	Permissible capacitance at PD				100	pF
102	V(PD)	Voltage at PD			0.9		V
103	Idc(PD)	Permissible DC-photocurrent in PD (ambient light supression)		-15		0	µA
104	I(PD)mg	Monotone Gain Range of I(PD)pk	|Ipn()| increases or remains constant when |I(PD)pk| increases (see Fig. 3)	-1.5		0	mA
105	twhi	Permissible Photocurrent Pulse Duration	see Fig. 3 and 4	1.0			µs
106	twlo	Permissible Photocurrent Pause Duration	2^{nd} Gpk ≥ 90 % 1^{st} Gpk (resp. of single pulse, see Fig. 4)	2.0			µs
107	trec	Flash Recovery Time	I(PD)pk = -1.8 mA			10	µs
108	trec	Power-Flash Recovery Time	I(PD)pk = -5 mA, magnitude of photocurrent integral equal 15 mAs			30	µs
109	Gpk	Pulse Current Gain	Gpk = [Ipn() − IO * ISUM] / I(PD)pk, I(PD)dc = -15...0 µA, I(PD)pk = -1...-0.1 µA, tr = tf = 0.5 µs, twpk = 1 µs (see Fig. 3)	360	490	620	
110	fl	Lower Cut-off Frequency (-3dB)	I(PD)dc = -15...-2.5 µA, I(PD)ac = 5 µApp sinusoidal waveform	65	100	155	kHz
111	fh	Upper Cut-off Frequency (-3dB)	I(PD)dc = -15...-2.5 µA, I(PD)ac = 5 µApp sinussoidal waveform	380	530	750	kHz
112	fΔ	Bandwidth (-3dB)	fΔ = fh − fl	270	430	670	kHz
113	V(SN, SP)	Permissible Voltage at SN, SP		3.5		VDD	V
114	ISUM	Output currents I(SN) + I(SP)	V(SN, SP) = 4...5 V Tj = 27 °C	4.9	 7.5	9.7	mA mA
115	IO	Relative Current Offset	IO = [I(SN) − I(SP)] / ISUM, I(PD) = 0	-10		10	%
116	Ilk	Leakage Current I(SN) + I(SP)	output disabled			4.0	µA
117	Idlk()	Differential Leakage Current	Idlk() = I(SN) − I(SP), I(PD)pk = -600 µA, twhi = 3 µs, output stage disabled (see Fig. 3)	-0.1		0.1	µA
118	Ipn()	Differential Output Current	Ipn() = I(SN) − I(SP), I(PD)pk = -10 µA (see Fig. 3)	-7	-5	-3.0	mA
119	Ipn()	Differential Output Current	Ipn() = I(SN) − I(SP), I(PD)pk = -100 µA (see Fig. 3)	-9.7	-7.3	-4.0	mA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 5 V ±10 %, V(SN, SP) = 3.5 V...VDD, Tj = -25...85 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
120	INoise	Differential Output Current Noise (RMS)	I(PD)dc = -15 µA, RGen = 500 kΩ, no additional filter, Tj = 27 °C		5		µA
121	INoise	Differential Output Current Noise (RMS)	I(PD)dc = -15 µA, RGen = 500 kΩ, with BP-filter 50 kHz...1.2 MHz, Tj = 27 °C		3.5		µA
122	tp()IDCon	Output Stage Turn-on Delay: CLK lo → hi to 10 % I(SN), I(SP)	I(PD)dc = -15 µA...0, I(PD)ac = 0 (see Fig. 4)			3.0	µs
123	tp()IDCoff	Output Stage Turn-off Delay: CLK lo → hi to 10 % I(SN), I(SP)	I(PD)dc = -15 µA...0, I(PD)ac = 0 (see Fig. 4)			3.0	µs
124	Rsc()	On-Resistance of short circuiting switch at PD0, PD1	Input deselected (see Fig. 5)			40	Ω
Control Inputs DIN, CLK							
201	Vt()hi	Threshold Voltage hi				66	%VDD
202	Vt()lo	Threshold Voltage lo		33			%VDD
203	Vhys()	Schmitt-Trigger Input Hysteresis		400			mV
204	Ipd()	Pull-Down Current	V() = 1 V...VDD Tj = 27 °C	3	 6	12	µA µA
Output Buffer DOUT							
301	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(DOUT); I() = -4 mA			0.4	V
302	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	V
303	Isc()hi	Short-Circuit Current hi	V() = 0 V Tj = 27 °C	-100	 -40	-25	mA mA
304	Isc()lo	Short-Circuit Current lo	V() = VDD Tj = 27 °C	25	 40	100	mA mA
305	tr()	Rise Time	CL() = 50 pF Tj = 27 °C		 20	60	ns ns
306	tf()	Fall Time	CL() = 50 pF Tj = 27 °C		 20	60	ns ns
Switching Characteristics							
401	tplh(CLK-DOUT)	Propagation Delay: CLK hi → lo until DOUT lo → hi	CL(DOUT) = 50 pF (see Fig. 2) Tj = 27 °C		 25	60	ns ns
402	tphl(CLK-DOUT)	Propagation Delay: CLK hi → lo until DOUT hi → lo	CL(DOUT) = 50 pF (see Fig. 2) Tj = 27 °C		 25	60	ns ns

OPERATING REQUIREMENTS: Logic

Operating Conditions: VDD = 5 V ±10 %, Ta = 0...70 °C, CL() = 50 pF,
input levels lo = 0...0.45 V, hi = VDD - 0.45 V...VDD, see Fig. 1 for reference levels and waveforms

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I001	ten	Activation Time: DIN lo → hi to CLK lo → hi	standby to amplifier operation (see Fig. 4)	10		µs
I002	tinh	Output Activation Time: 1st CLK lo → hi until output ready to report	sufficient decay of transient differential output current: |I(SN) − I(SP) − IO * ISUM| ≤ 20 µA (see Fig. 4)	5		µs
I003	tset	Setup time: DIN stable before CLK lo → hi	see Fig. 2	50		ns
I004	thold	Hold time: DIN stable after CLK lo → hi	see Fig. 2	50		ns
I005	fo	Permissible Frequency at CLK			10	MHz

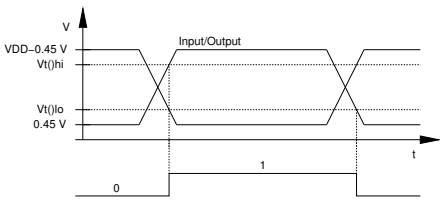


Figure 1: Reference levels

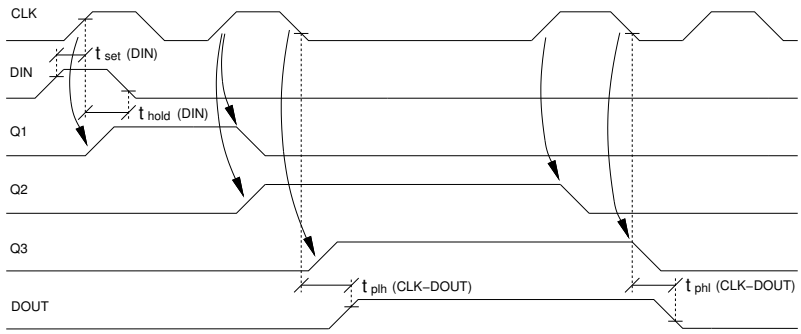


Figure 2: Timing characteristics

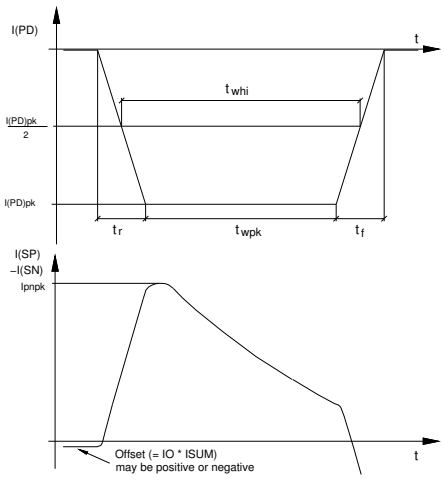


Figure 3: Differential output current pulse at SP and SN versus input current pulse at PD

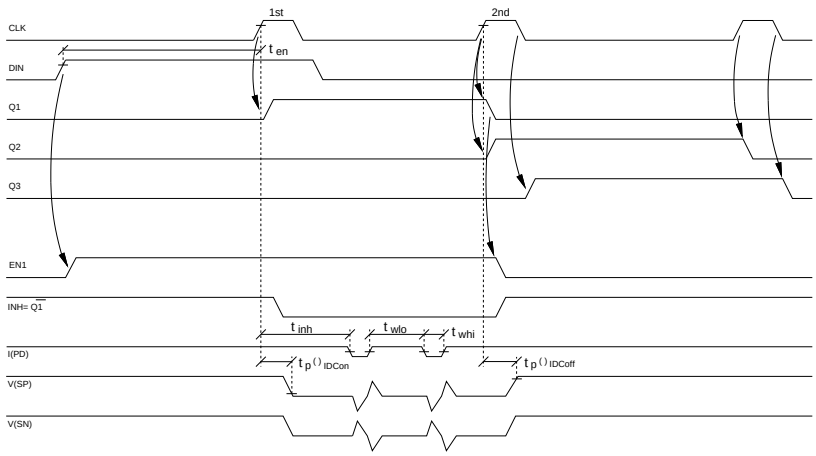


Figure 4: Timing characteristics (analogue section). Outputs SP and SN with resistors to VDD

INPUT SAFETY SWITCH

The FMEA driven schematic design and layout topology of the iC-ME ensures maximum safety and allows the utilisation of an input safety switch.

Figure 5 shows the schematic of the input safety switch. Given this particular topology in addition to the redundant layout (e.g. of ground switches) any single fault can either be detected by the evaluation circuitry or results in a safe state. Likewise external single failures (e.g. shortcircuit of PD0 to PD1) are safe or detectable even during an internal single failure.

Due to the redundancy of the layout, a ground breakage or a simultainous failure of the bypass switches is practically impossible.

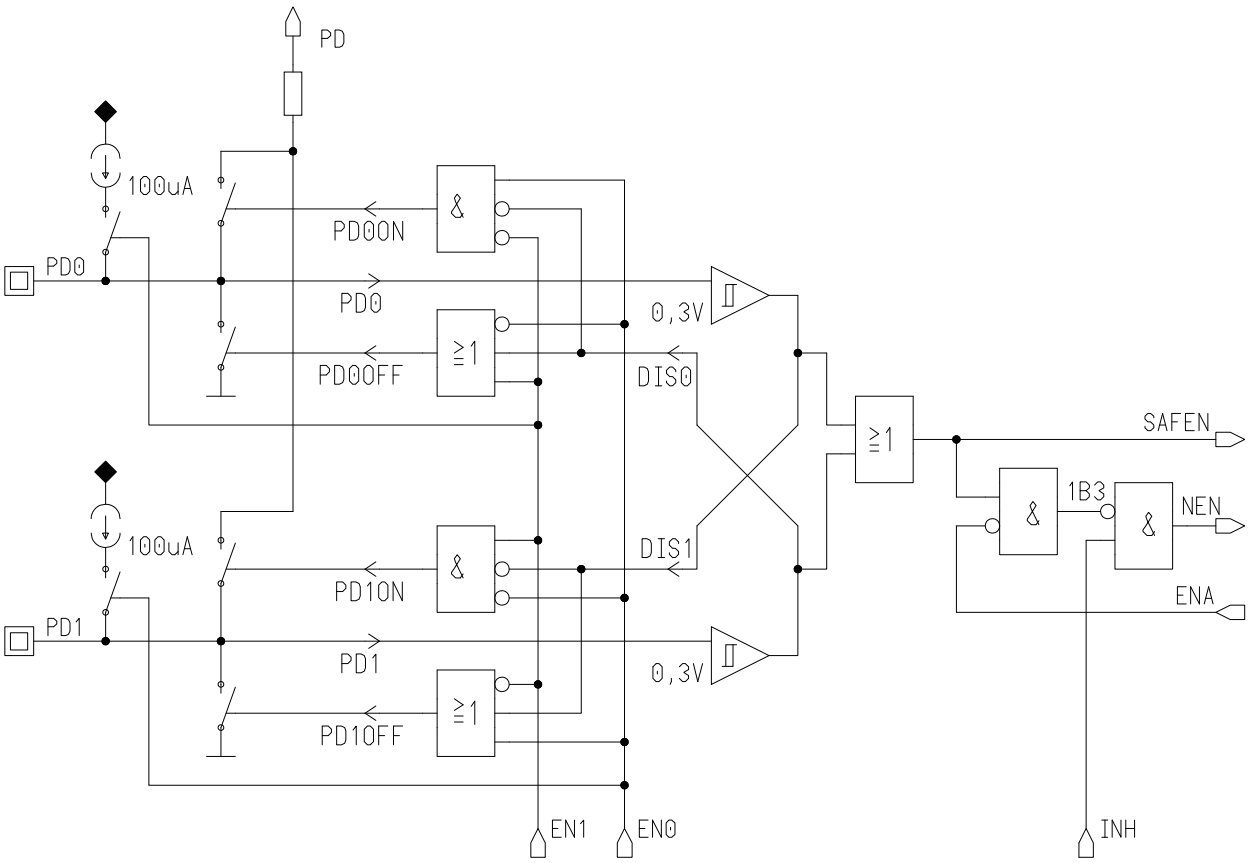


Figure 5: Input safety switch

APPLICATIONS INFORMATION

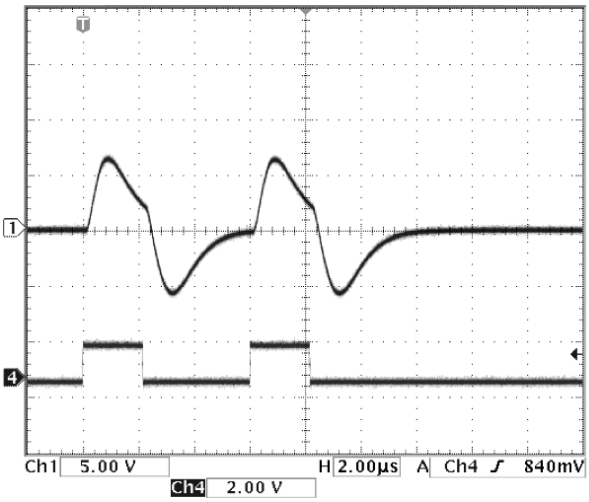


Figure 6: Regular input signals

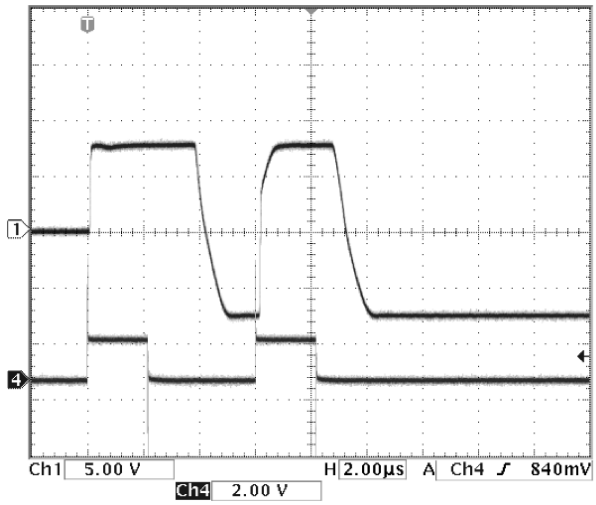


Figure 7: Excessive input signals

Signal Processing

Figures 6 and 7 show output signal I(SP) – I(SN) in *normal* drive and in extreme overdrive (with the photodiode and input amplifier in saturation).

It is clear from these diagrams that iC-ME, even when in overdrive, is not *blind* to a follow-on pulse.

For evaluation purposes the response to the rising edge of the light pulse (i.e. the rising edge of the output signal) is to be used as it is this edge alone, even in the most extreme overdrive, which yields definite results. Evaluating the falling edge of the output signal or the level of the negative output signal half-wave (the recovery process at the end of a light pulse) is generally not advised.

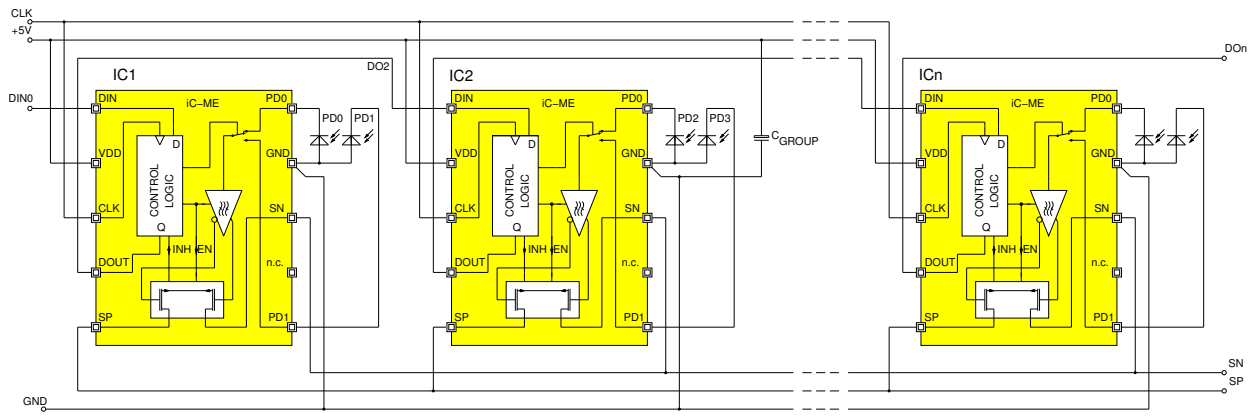


Figure 8: Schematic of a chain configuration

Light curtain

The circuit in Figure 8 shows iC-ME chained up to form a light curtain, where consecutive PIN diodes receive and evaluate clock-driven light pulses.

When discussing the function of iC-ME, it is assumed that all flip-flops in IC1 to ICn have been reset, for example after the operating voltage has been switched on. The signal DIN0 = hi activates the bandpass amplifier and the photo diode input PD0 of IC1. Outputs SP and SN remain tri-state until the rising CLK edge shifts in the input hi signal at input DIN0.

With no AC photocurrent fractions in the receiver photodiode, approximately equal currents are drawn in SP and SN. Within a time tinh $\geq$ 5 µs, the transient differ-

ential currents in the output stage, caused by switching the chip on, have decayed, and iC-ME is ready to receive.

Current is drawn from pin PD0 (IC1) by a light pulse on the photodiode PD0, and the currents at outputs SP and SN react as shown in Figure 9: I(SP) rises and returns to the initial value with a time constant determined by the lower bandpass amplifier cutoff frequency, as long as the photodiode is constantly illuminated. When the light pulse decays, the current in SP first sinks and then ramps up to the standby value.

The current in SN has a mirror-imaged time dependance, as the sum I(SP) + I(SN) is constant.

With DIN0 = 0, the next rising CLK edge resets FF1 and turns off the currents in the differential output. Simultaneously, FF1 sends the stored information to FF2. FF3 also accepts this information with the trailing CLK edge and switches the input safety switch from PD0 to PD1. With the next rising CLK edge the FF4 accepts the hi signal at its input and the differential output stage is activated again. Evaluation of the photo current of PD1 und forwarding of the control signal to output DOUT of IC1 works likewise as described above for PD0.

The hi signal now present at DOUT of IC1 activates the the bandpass amplifier and the bias of the next device, IC2. The pulse diagram is also valid for the subsequent components in the chain, i.e. the ICs arranged as a light curtain form a clock-driven shift register which passes on the input information.

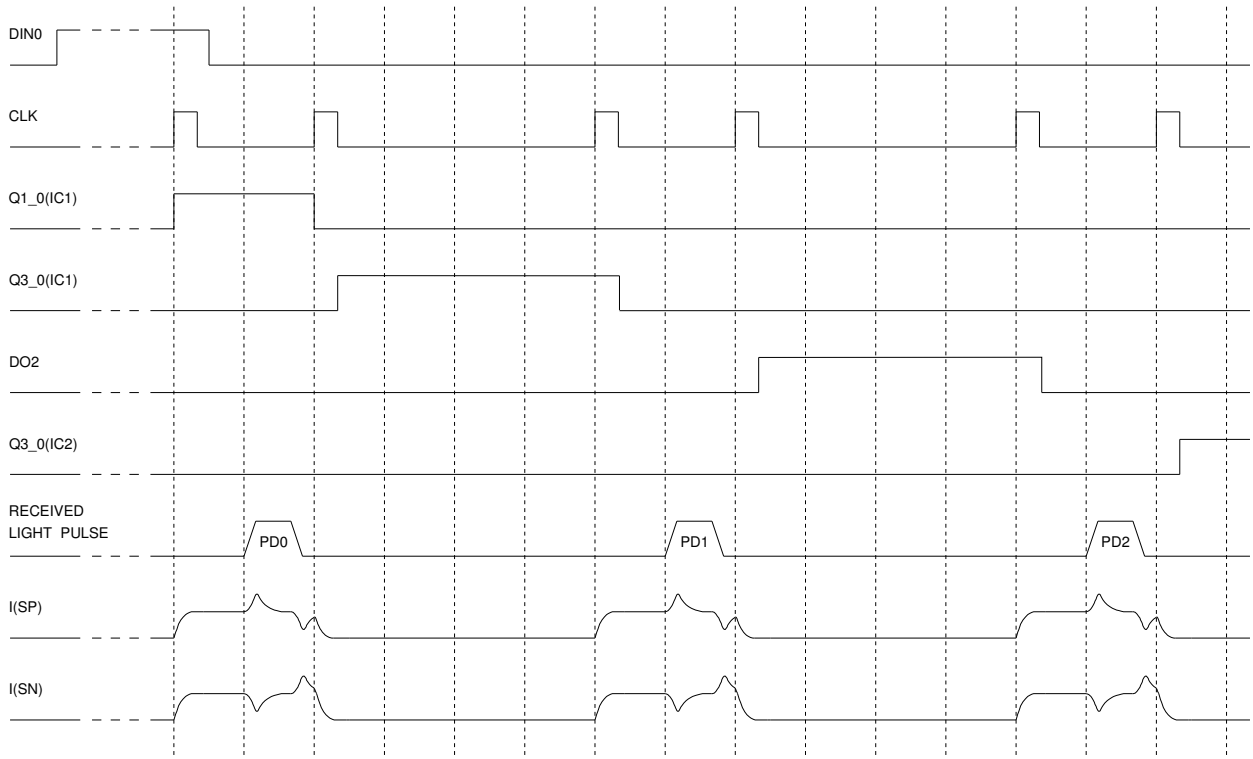


Figure 9: Signals for the chain configuration of Fig. 8

Light curtain PCB layout

The PCB layout for light curtain receivers is not critical. The photodiode anode should be directly connected to iC-ME's GND pin so that voltage drop caused by the chip's operating current is not coupled into the photocurrent signal.

As the power consumption is relatively small, only low-level back-up capacitors are required (typ. 1 µF electrolytic capacitor in parallel to 47 to 100 nF ceramic capacitor). The ceramic capacitors should be placed at a 7.5 cm distance, electrolytic capacitors at up to twice this distance. The number of receivers backed up as a group in this manner is irrelevant as only one device is activated drawing current at a time.

ORDERING INFORMATION

Type	Package	Order Designation
iC-ME	DFN10	iC-ME DFN10

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (0) 61 35 - 92 92 - 0
Fax: +49 (0) 61 35 - 92 92 - 192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: http://www.ichaus.com/sales_partners