iC-MB4

BiSS INTERFACE MASTER

iC-MB4 is a single chip BiSS/SSI interface master controller. BiSS C, BiSS B, SSI and extended SSI devices, sensors and actuators can be fully accessed by iC-MB4. Up to 8 devices can be connected, each with up to 64 bit single cycle data length and up to 16 bit CRC verification.

Features

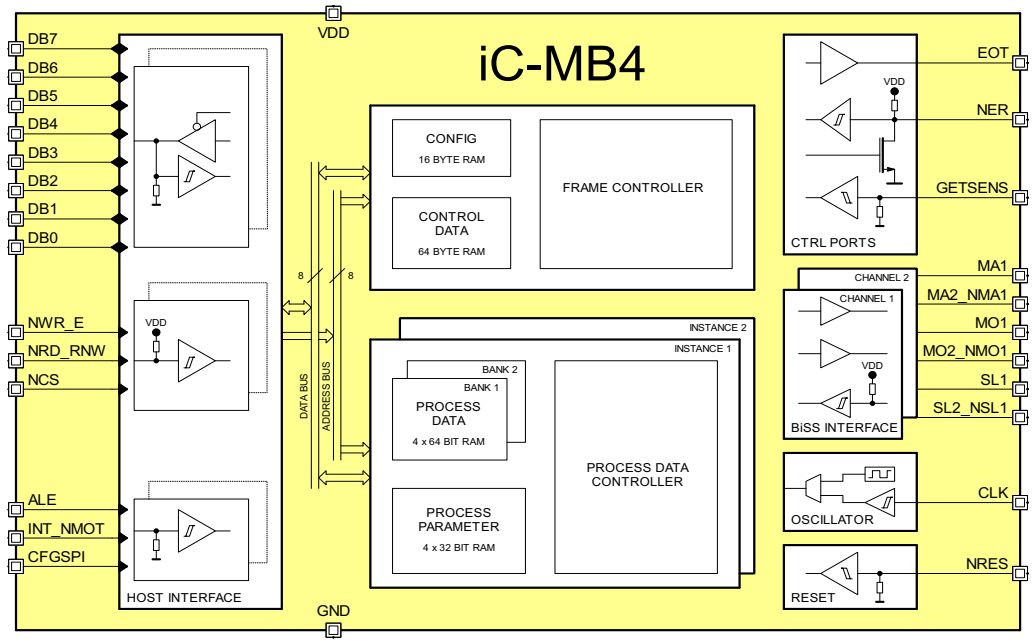
- Bidirectional BiSS communication with up to 8 slaves
- Supports BiSS C, BiSS B, SSI and extended SSI
- Synchronous acquisition with data rates up to 10 Mbit/s
- Configurable interface with TTL, CMOS, RS422 or LVDS
- Slave register operations during cyclic data transfers
- Automatic line delay compensation
- Data lengths of up to 64 bit for sensor data per slave
- CRC verification with up to 16 bits per slave
- Separate memory banks for free controller access during BiSS sensor data transfers
- 64 bytes memory for bidirectional register access
- SPI or parallel interface to host e.g. microcontroller
- Single 3 V to 5V supply

BiSS bus structures at two BiSS channels are accessible. iC-MB4 provides CMOS, TTL, RS422 or LVDS transceivers. A parallel interface or alternatively one or two SPI interfaces enable communication to the connected microcontroller. The sensor/actuator data transfer is started by a microcontroller command, via pin GETSENS or by automatic sensor data acquisition.

The sensor/actuator data transfer end and status is signaled at the pins EOT and NER. Status register provide details on single cycle data or register communication. An external clock or internal 20 MHz oscillator can be selected. The MA clock rate and the automatic sensor data request rate are configurable.

Applications

- Device communication in multi-sensor sytems
- Position acquisition with encoders
- Drives and motor-feedback systems
- Numeric controls
- Robotics



iC-Haus

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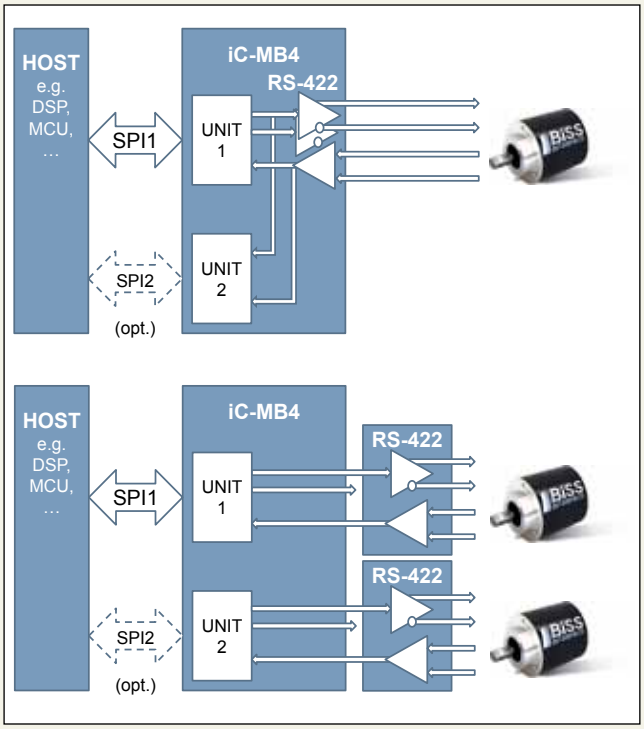
iC-MB4 BiSS INTERFACE MASTER

Pin Functions

TSSOP	QFN	Name	Function
3...10	1...8	DB0...7	Data Bus I/O, SPI 1/2
9	7	DB6	Data Bus I/O, SPI2 Serial Data Input
11	9	GND	Ground
12	10	VDD	+3 V...+5.5 V Supply Voltage
13	11	EOT	End-Of-Transmission Output
14	12	GETSENS	Sensor Data Request Input
15	13	NER	Error Message I/O, low active
16	15	MA1	Clock Line Output Channel 1
n.a.	16	MA2_NMA1	Clock Line Output Channel 2 / Inverted Clock Line Outp. Ch. 1
17	17	SL1	Data Line Output Channel 1
n.a.	18	SL2_NSL1	Data Line Input Channel 2 / Inverted Data Line Input Ch. 1
18	19	INT_NMOT	Mode Selection (Intel, Motorola)
19	20	CFGSPI	Ser./Par. Mode Selection Input
20	21	NRES	Reset Input, low active
21	22	CLK	External Clock Input
22	23	MO1	Data Line Output Channel 1
n.a.	24	MO2_NMO1	Data Line Output Channel 2 / Inverted Data Line Outp. Ch. 1
23	25	NWR_E	Write Input (low active) / Enable Inp.
24	26	NRD_RNW	Read Input low active / high active
1	27	NCS	Chip Select Input (low active)
2	28	ALE	Address Latch Enable Input / SPI Clock Input

Application Example



Key Specifications

General	
Supply Voltage	single 3 V to 5.5 V
On-Chip Clock Oscillator	20 MHz
Operational Temp. Range	-40 °C to +85 °C (+125 °C optional)
Package	TSSOP24, QFN28 5 mm x 5 mm

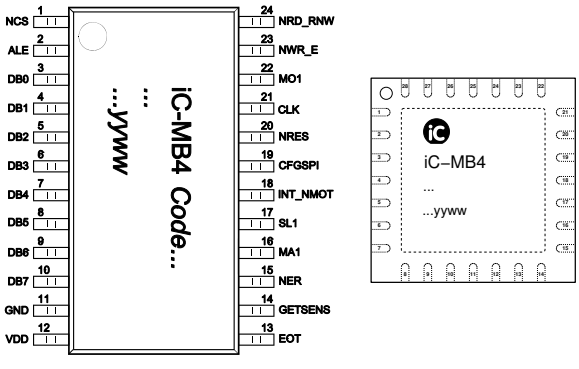
Interface Operating Modes	
Host Interfaces	10 MHz SPI, 40 ns parallel interface
With TSSOP24 Package	1 channel TTL/CMOS (pin compatible to iC-MB3)
With QFN28-5x5 Package	2 channel TTL/CMOS or 1 channel RS-422/LVDS/TTL/CMOS

BiSS Interfaces	
Compatible Sensors/ Actuators	BiSS C, BiSS B, SSI, extended SSI, 2-wire
I/O Interfaces Types	TTL, CMOS RS422, LVDS
I/O Interfaces Rates	BiSS/SSI 10 MHz
Slave Count	up to 8 slaves
SCD Interfaces Clock Range	62.5 kHz to 10 MHz
Automatic SCD Cycle Time	1 µs to 4 ms

RS-422 Interface (QFN28)	
Transceiver Performance	10 Mbit/s for BiSS/SSI
Differential RS-422 Output	to +/-50 mA push-pull, > 2.5 V at RL 100 Ω
Differential RS-422 Receiver	-7 V to +12 V tolerant (with external resistors)

Safety Functions	
Second SPI Interface	for redundant SCD data access
Position Data CRC; SCD	3...16 bit, optional CRC retention
Life Counter, Error, Warning	Covered by single cycle data CRC
Status Bytes	Error, warning, watchdog, individual sensor data valid, SCD valid, CDS channel 1 and 2, valid bytes for register access, CDM timeout, RAM bank monitoring

Packages TSSOP24, QFN28-5x5



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