iC-MB4 is a single chip BiSS/SSI interface master controller. BiSS C, BiSS B, SSI and extended SSI devices, sensors and actuators can be fully accessed by iC-MB4. Up to 8 devices can be connected, each with up to 64 bit single cycle data length and up to 16 bit CRC verification.

### Features
- Bidirectional BiSS communication with up to 8 slaves
- Supports BiSS C, BiSS B, SSI and extended SSI
- Synchronous acquisition with data rates up to 10 Mbit/s
- Configurable interface with TTL, CMOS, RS422 or LVDS
- Slave register operations during cyclic data transfers
- Automatic line delay compensation
- Data lengths of up to 64 bit for sensor data per slave
- CRC verification with up to 16 bits per slave
- Separate memory banks for free controller access during BiSS sensor data transfers
- 64 bytes memory for bidirectional register access
- SPI or parallel interface to host e.g. microcontroller
- Single 3 V to 5V supply

BiSS bus structures at two BiSS channels are accessible. iC-MB4 provides CMOS, TTL, RS422 or LVDS transceivers. A parallel interface or alternatively one or two SPI interfaces enable communication to the connected microcontroller. The sensor/actuator data transfer is started by a microcontroller command, via pin GETSENS or by automatic sensor data acquisition.

The sensor/actuator data transfer end and status is signaled at the pins EOT and NER. Status register provide details on single cycle data or register communication. An external clock or internal 20 MHz oscillator can be selected. The MA clock rate and the automatic sensor data request rate are configurable.

### Applications
- Device communication in multi-sensor systems
- Position acquisition with encoders
- Drives and motor-feedback systems
- Numeric controls
- Robotics
## Key Specifications

### General
- **Supply Voltage**: Single 3 V to 5.5 V
- **On-Chip Clock Oscillator**: 20 MHz
- **Operational Temp. Range**: -40 °C to +85 °C (+125 °C optional)
- **Package**: TSSOP24, QFN28 5 mm x 5 mm

### Interface Operating Modes
- **Host Interfaces**: 10 MHz SPI, 40 ns parallel interface
- **With TSSOP24 Package**: 1 channel TTL/CMOS (pin compatible to iC-MB3)
- **With QFN28-5x5 Package**: 2 channel TTL/CMOS or 1 channel RS-422/LVDS/TTL/CMOS

### BiSS Interfaces
- **Compatible Sensors/Actuators**: BiSS C, BiSS B, SSI, extended SSI, 2-wire
- **I/O Interfaces Types**: TTL, CMOS RS422, LVDS
- **I/O Interfaces Rates**: BiSS/SSI 10 MHz
- **Slave Count**: Up to 8 slaves
- **SCD Interfaces Clock Range**: 62.5 kHz to 10 MHz
- **Automatic SCD Cycle Time**: 1 µs to 4 ms

### RS-422 Interface (QFN28)
- **Transceiver Performance**: 10 Mbit/s for BiSS/SSI
- **Differential RS-422 Output**: to +/-50 mA push-pull, > 2.5 V at RL 100 Ω
- **Differential RS-422 Receiver**: -7 V to +12 V tolerant (with external resistors)

### Safety Functions
- **Second SPI Interface**: For redundant SCD data access
- **Position Data CRC, SCD**: 3...16 bit, optional CRC retention
- **Life Counter, Error, Warning**: Covered by single cycle data CRC
- **Status Bytes**: Error, warning, watchdog, individual sensor data valid, SCD valid, CDS channel 1 and 2, valid bytes for register access, CDM timeout, RAM bank monitoring

### Application Example

![Application Example Diagram](image)

This preliminary information is not a guarantee of device characteristics or performance. All rights to technical changes reserved.

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### Pin Functions

<table>
<thead>
<tr>
<th>TSSOP</th>
<th>QFN</th>
<th>Name</th>
<th>Function</th>
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<td>1...8</td>
<td>D80...7</td>
<td>Data Bus I/O, SPI 1/2</td>
</tr>
<tr>
<td>9</td>
<td>7</td>
<td>DB6</td>
<td>Data Bus I/O, SPI2 Serial Data Input</td>
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<tr>
<td>11</td>
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</tr>
<tr>
<td>12</td>
<td>11</td>
<td>EOT</td>
<td>End-Of-Transmission Output</td>
</tr>
<tr>
<td>14</td>
<td>12</td>
<td>GETSENS</td>
<td>Sensor Data Request Input</td>
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<tr>
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<td>13</td>
<td>NER</td>
<td>Error Message I/O, low active</td>
</tr>
<tr>
<td>16</td>
<td>15</td>
<td>MA1</td>
<td>Clock Line Output Channel 1</td>
</tr>
<tr>
<td>n.a.</td>
<td>16</td>
<td>MA2_NMA1</td>
<td>Clock Line Output Channel 2</td>
</tr>
<tr>
<td></td>
<td>17</td>
<td>SL1</td>
<td>Data Line Output Channel 1</td>
</tr>
<tr>
<td>n.a.</td>
<td>18</td>
<td>SL2_NSL1</td>
<td>Data Line Input Channel 2</td>
</tr>
<tr>
<td>18</td>
<td>19</td>
<td>INT_NM0T</td>
<td>Mode Selection (Intel, Motorola)</td>
</tr>
<tr>
<td>19</td>
<td>20</td>
<td>CFGSPI</td>
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<td>20</td>
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<tr>
<td>21</td>
<td>22</td>
<td>CLK</td>
<td>External Clock Input</td>
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<tr>
<td>22</td>
<td>23</td>
<td>M01</td>
<td>Data Line Output Channel 1</td>
</tr>
<tr>
<td>n.a.</td>
<td>24</td>
<td>M02_NM01</td>
<td>Data Line Output Channel 2</td>
</tr>
<tr>
<td>23</td>
<td>25</td>
<td>NWR_E</td>
<td>Write Input (low active) / Enable Inp.</td>
</tr>
<tr>
<td>24</td>
<td>26</td>
<td>NRD_RNW</td>
<td>Read Input low active / high active</td>
</tr>
<tr>
<td>1</td>
<td>27</td>
<td>NCS</td>
<td>Chip Select Input (low active)</td>
</tr>
<tr>
<td>2</td>
<td>28</td>
<td>ALE</td>
<td>Address Latch Enable Input / SPI Clock Input</td>
</tr>
</tbody>
</table>

### Packages TSSOP24, QFN28-5x5