iC-LA is an integrating light-to-voltage converter with 64x1 pixels at a 200 µm pitch. Each pixel consists of a 183 µm x 200 µm photodiode with integration capacitor and a track-and-hold circuit.

Photocurrent integration is started simultaneously for all pixels with the rising edge of the clock signal when DIN is high. If input DIN is still high at the end of a completed integration cycle, all integration capacitors are automatically reset and a new integration cycle is initiated (continuous operation).

In hold mode, the pixels are subsequently fed to the multiplexer which selects the odd or even bus line for the output buffer. This dual line configuration allows a high working speed. Input DNU determines the shift direction of the multiplexer. With DNU low the pixels are switched in ascending order to AOUT, starting at pixel 1; with DNU high in descending order starting at pixel 64.

Features

iC-LA
- 64 photosensors with 200 µm pitch (127 DPI)
- Internal bi-directional shift register
- Extendable data I/O supports cascading
- On-chip temperature sensor

iC-LF1401
- 128 active photo pixels with 63.5 µm pitch (400 DPI)
- Pin-to-pin compatible with TSL1401
- Only 128 clocks required for readout

iC-LF1402
- 256 active photo pixels with a gap and distortion free 63.5 µm pitch (400 DPI)
- Function equivalent to TSL1402 (serial mode)
- Only 256 clocks required for readout

iC-LF Series
- Shutter function enables flexible exposure times
- High pixel clock rate of up to 5 MHz
- Glitch-free push-pull output amplifier

Applications

- Optical linear sensors
- CCD substitute
- Distance measurement (triangulation)
- Spectroscopy
iC-LA, iC-LF 1401, iC-LFL 1402
CMOS LINEAR IMAGE SENSORS

iC-LF1401 and iC-LFL1402 are integrating light-to-voltage converters with 128x1 resp. 256x1 pixels at a 63.5 \( \mu \text{m} \) pitch. Due to the monolithic integration there is no pixel-gap or pitch distortion whatsoever. Each pixel consists of a 56.4 \( \mu \text{m} \times 200 \mu \text{m} \) photodiode, an integration capacitor and a sample-and-hold circuit.

The integrated control logic makes operation very simple, with only a start and clock signal necessary. A third control input (DIS) allows the integration to be halted at any time (electronic shutter).

With the start of integration signal (SI = hi) the hold mode is activated for all pixels simultaneously at the next rising clock edge; starting with pixel 1 the pixel voltages are sequentially switched to the push-pull output amplifier. The second clock pulse resets all integration capacitors and the integration period starts again in the background during the output phase.

iC-LF1401 and iC-LFL1402 are suitable for high clock rates of up to 5 MHz. If this is not required the supply current can be reduced via the external bias setting (current into pin RSET).

### Key Specifications

#### iC-LA
- Supply Voltage at VDDA, VDDD: 5 V ± 5%
- Supply Current in VDDA, VDDD
  - f(CLK) ≤ 5 MHz: 20 mA max.
- Sensitivity
  - typ. 4.19 V/pWs @ 880 nm
  - typ. 7.78 V/pWs @ 660 nm
- Spectral Sensitivity: typ. 0.335 A/W @ 680 nm
- Spectral Application Range: 400 to 950 nm
- Pixel Clock Rate: 5 MHz max.

#### iC-LF, iC-LFL
- Supply Voltage at VCC, VDD: 5 V ± 10%
- Supply Current in VDD
  - @ f(CLK) = 1 MHz
    - iC-LF: typ. 200 µA
    - iC-LFL: typ. 390 µA
- Supply Current in VCC
  - typ. 8 mA
  - typ. 11.5 mA
- Sensitivity: typ. 2.88 V/pWs @ 680 nm
- Spectral Sensitivity: 0.5 A/W @ 680 nm
- Spectral Application Range: 400 to 980 nm
- Pixel Clock Rate: 5 MHz max.

### Pin Functions iC-LA

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDDA</td>
<td>+5 V Analogue Supply Voltage</td>
</tr>
<tr>
<td>2</td>
<td>VDDD</td>
<td>+5 V Digital Supply Voltage</td>
</tr>
<tr>
<td>3</td>
<td>DIN</td>
<td>Data Input</td>
</tr>
<tr>
<td>4</td>
<td>VCMIN</td>
<td>Offset Voltage Input for Integration Capacitor</td>
</tr>
<tr>
<td>5</td>
<td>AOUT</td>
<td>Analog Output</td>
</tr>
<tr>
<td>6</td>
<td>CLK</td>
<td>Clock Input</td>
</tr>
<tr>
<td>7</td>
<td>DNU</td>
<td>Down-Not-Up Input</td>
</tr>
<tr>
<td>8</td>
<td>DOUT</td>
<td>Data Output</td>
</tr>
<tr>
<td>9</td>
<td>GNDD</td>
<td>Digital Ground</td>
</tr>
<tr>
<td>10</td>
<td>GNDA</td>
<td>Analog Ground</td>
</tr>
</tbody>
</table>

### Pin Functions iC-LF, iC-LFL

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SI</td>
<td>Start Integration Input</td>
</tr>
<tr>
<td>2</td>
<td>CLK</td>
<td>Clock Input</td>
</tr>
<tr>
<td>3</td>
<td>AO</td>
<td>Analog Output</td>
</tr>
<tr>
<td>4</td>
<td>VCC</td>
<td>+5 V Supply Voltage</td>
</tr>
<tr>
<td>5</td>
<td>RSET</td>
<td>Bias Current (connected to GND for internal bias = default; resistor from VCC to RSET for reduced current consumption)</td>
</tr>
<tr>
<td>6</td>
<td>AGND</td>
<td>Analog Ground</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>Digital Ground</td>
</tr>
<tr>
<td>8</td>
<td>DIS</td>
<td>Hold Integration Input</td>
</tr>
</tbody>
</table>

### Pin Configurations

![Pin Configuration Diagrams]