

iC-HT CONFIGURATION

The iC-HT is interfaced to the microcontroller with an SPI interface. The used configuration is just an example setup and needs to be modified to the individual users operating point and hardware setup including the GPIO_IO P0.20 for EC1 and P0.21 for EC2 control.

iC-HT EMBEDDED C CODE EXAMPLE

This is an example of using the iC-HT with an embedded system based on an NXP™ ARM® based microcontroller. It shows a simple possible iC-HT startup configuration sequence.

```

/*
|-----
|   Start of HT_LASER_DEMO application
|-----
*/

SpiWrite(HT_ADDRESS_MODE, HT_CONFIG_MODE);           // Place iC-HT in Configuration mode

HtStatus = SpiRead(HT_ADDRESS_STATUS_INITRAM_PDOVDD_MEMERR_OVT_OVC2_OVC1_OSCERR_CFGTIMO); // Read Status1
HtStatus = SpiRead(HT_ADDRESS_STATUS_MAPC1_MONC1_LDKSAT1_MAPC2_MONC2_LKDSAT2);           // Read Status2

HtConfiguration = ( // Configure configuration bits
    HT_EACC_ACC_MODE           |
    HT_ECIE_CI_CAP_OFF        |
    HT_DISP_PLR_OFF           |
    HT_DISC_EC1_ON            |
    HT_EOC_OFFSET_COMP_OFF    |
    HT_ADCC_ADC_OFF           |
);
SpiWrite(HT_ADDRESS_EACC1_ECIE1_DISP1_DISC1_EOC1_ADCC1, HtConfiguration); // Write Channel-1 configuration
SpiWrite(HT_ADDRESS_EACC2_ECIE2_DISP2_DISC2_EOC2_ADCC2, HtConfiguration); // Write Channel-2 configuration

HtConfiguration = HT_ILIM_MAX; // Configure configuration bits
SpiWrite(HT_ADDRESS_ILIM1, HtConfiguration); // Write Channel-1 configuration
SpiWrite(HT_ADDRESS_ILIM2, HtConfiguration); // Write Channel-2 configuration

HtConfiguration = HT_RMD_MAX; // Configure configuration bits
SpiWrite(HT_ADDRESS_RMD1, HtConfiguration); // Write Channel-1 configuration
SpiWrite(HT_ADDRESS_RMD2, HtConfiguration); // Write Channel-2 configuration

//-----
HtRefSetting = 0x000; // Set REF current level
HtRefSettingMsb = HtRefSetting >> 8; // Shift down bits 9 and 8
HtRefSetting98 = (unsigned char)HtRefSettingMsb; // Copy bits 9 and 8
HtRefSetting70 = (unsigned char)HtRefSetting & 0xFF; // Mask bits 7:0
// Configure configuration bits
HtConfiguration = ( // Configure configuration bits
    HT_COMP_MIN           |
    HT_RLDSK_LESS_500mV  |
    HtRefSetting98        |
);
SpiWrite(HT_ADDRESS_COMP1_RLDSK1_REF1bits98, HtConfiguration); // Write Channel-1 configuration
SpiWrite(HT_ADDRESS_COMP2_RLDSK2_REF2bits98, HtConfiguration); // Write Channel-2 configuration

HtConfiguration = HtRefSetting70; // Configure configuration bits
SpiWrite(HT_ADDRESS_REF1bits70, HtConfiguration); // Write Channel-1 configuration
SpiWrite(HT_ADDRESS_REF2bits70, HtConfiguration); // Write Channel-2 configuration
//-----

HtConfiguration = ( // Configure configuration bits
    HT_RACC1_LOW           |
    HT_ADSNF1_MDA          |
    HT_RACC2_LOW           |
    HT_ADSNF2_MDA          |
);
SpiWrite(HT_ADDRESS_RACC1_ADSNF1_RACC2_ADSNF2, HtConfiguration); // Write Channel-1 & Channel-2 configuration

SpiWrite(HT_ADDRESS_MODE, HT_OPERATION_MODE); // Place iC-HT in Configuration mode

GPIO_IOSET = P0_20_HT_EC1; // P0.20 High for EC1
GPIO_IOSET = P0_21_HT_EC2; // P0.21 High for EC2

HtStatus = SpiRead(HT_ADDRESS_STATUS_INITRAM_PDOVDD_MEMERR_OVT_OVC2_OVC1_OSCERR_CFGTIMO); // Read Status1
HtStatus = SpiRead(HT_ADDRESS_STATUS_MAPC1_MONC1_LDKSAT1_MAPC2_MONC2_LKDSAT2); // Read Status2

```

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iC-HT EMBEDDED C CODE HEADER FILE

This is an example header file for use with iC-HT with an embedded system base e.g. a microcontroller. It shows a simple possible iC-HT definition.

```

/*
|-----|
|           iC-HT definitions           |
|-----|
*/

// Status Addresses
#define HT_ADDRESS_STATUS_INITRAM_PDOVDD_MEMERR_OVT_OVC1_OSCERR_CFGTIMO      0x00    // Address 0x00, Read
  only
#define HT_ADDRESS_STATUS_MAPC1_MONC1_LDKSAT1_MAPC2_MONC2_LDKSAT2      0x01    // Address 0x01, Read only

// Measurement Addresses
#define HT_ADDRESS_STATS_TEMP      0x02    // Address 0x02, Read only
#define HT_ADDRESS_ADC1bits98      0x03    // Address 0x03, Read only
#define HT_ADDRESS_ADC1bits70      0x04    // Address 0x04, Read only
#define HT_ADDRESS_ADC2bits98      0x05    // Address 0x05, Read only
#define HT_ADDRESS_ADC2bits70      0x06    // Address 0x06, Read only

// Measurement Addresses
#define HT_ADDRESS_CHIP_REVISION      0x0F    // Address 0x0F, Read only

// Channel-1 Addresses
#define HT_ADDRESS_EACC1_ECIE1_DISP1_DISC1_EOC1_ADCC1      0x10    // Address 0x10, Read/Write
#define HT_ADDRESS_ILIM1      0x11    // Address 0x11, Read/Write
#define HT_ADDRESS_RMD1      0x12    // Address 0x12, Read/Write
#define HT_ADDRESS_COMP1_RLDKS1_REF1bits98      0x13    // Address 0x13, Read/Write
#define HT_ADDRESS_REF1bits70      0x14    // Address 0x14, Read/Write

// Channel-2 Addressses
#define HT_ADDRESS_EACC2_ECIE2_DISP2_DISC2_EOC2_ADCC2      0x15    // Address 0x15, Read/Write
#define HT_ADDRESS_ILIM2      0x16    // Address 0x16, Read/Write
#define HT_ADDRESS_RMD2      0x17    // Address 0x17, Read/Write
#define HT_ADDRESS_COMP2_RLDKS2_REF2bits98      0x18    // Address 0x18, Read/Write
#define HT_ADDRESS_REF2bits70      0x19    // Address 0x19, Read/Write

// Channel-1 & Channel-2 Addresses
#define HT_ADDRESS_RACC1_ADSNF1_RACC2_ADSNF2      0x1A    // Address 0x1A, Read/Write

// General Addresses
#define HT_ADDRESS_RDCC_MERGE      0x1B    // Address 0x1B, Read/Write
#define HT_ADDRESS_MODE      0x1C    // Address 0x1C, Read/Write
#define HT_ADDRESS_MOSCERR_MMONC_MLDKSAT1_MLDKSAT2_SOVT_SOVC1_SOVC2_SOSCERR      0x1D    // Address 0x1D, Read/Write

// Bit definitions
#define HT_SPI_READ      0x80    // SPI packet is for a Read
#define HT_SPI_WRITE      0x40    // SPI packet is for a Write

#define HT_OPERATION_MODE      0x01    // Operation mode
#define HT_CONFIG_MODE      0x02    // Config mode

#define HT_EACC_APC_MODE      0x00    // APC mode
#define HT_EACC_ACC_MODE      0x01    // ACC mode

#define HT_ECIE_CI_CAP_OFF      0x00    // Capacitor not on CI
#define HT_ECIE_CI_CAP_ON      0x02    // Capacitor on CI

#define HT_DISP_PLR_ON      0x00    // Programmable logarithmic monitor
  resistor for APC enabled
#define HT_DISP_PLR_OFF      0x04    // Programmable logarithmic monitor
  resistor for APC disabled

#define HT_DISC_EC1_ON      0x00    // EC1 enables channel
#define HT_DISC_EC1_OFF      0x08    // EC1 does not enable channel

#define HT_EOC_OFFSET_COMP_OFF      0x00    // Regulator offset compensation disabled
#define HT_EOC_OFFSET_COMP_ON      0x10    // Regulator offset compensation enabled

#define HT_ADCC_ADC_OFF      0x00    // ADC disabled
#define HT_ADCC_ADC_SOURCE_MDA_OR_PLR      0x80    // ADC sourced by V(MDA) when ADSNF=0 or
  sourced by V(PLR) when ADSNF=1
#define HT_ADCC_ADC_SOURCE_VB      0xA0    // ADC sourced by V(VB)
#define HT_ADCC_ADC_SOURCE_VDD      0xC0    // ADC sourced by V(VDD)
#define HT_ADCC_ADC_SOURCE_LDK      0xE0    // ADC sourced by V(LDK)

#define HT_ILIM_MIN      0x00    // Minimum overcurrent threshold
#define HT_ILIM_MAX      0xFF    // Maximum overcurrent threshold

#define HT_RMD_MIN      0x00    // PLR set to minimum resistance

```

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EMBEDDED EXAMPLE CODE AND HEADER FILE

preliminary



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```
#define HT_RMD_MAX 0xFF // PLR set to maximum resistance

#define HT_COMP_MIN 0x00 // Minimum compensation current
#define HT_COMP_MAX 0x70 // Maximum compensation current

#define HT_RLDSK_LESS_500mV 0x00 // V(LDK1)<0.5V sets LDKSAT1 alarm bit
#define HT_RLDSK_LESS_800mV 0x04 // V(LDK1)<0.8V sets LDKSAT1 alarm bit
#define HT_RLDSK_LESS_1000mV 0x08 // V(LDK1)<1.0V sets LDKSAT1 alarm bit
#define HT_RLDSK_LESS_1200mV 0x0C // V(LDK1)<1.2V sets LDKSAT1 alarm bit

#define HT_REFbits98_00 0x00 // Reference bits 9:8, 00
#define HT_REFbits98_01 0x01 // Reference bits 9:8, 01
#define HT_REFbits98_10 0x10 // Reference bits 9:8, 10
#define HT_REFbits98_11 0x11 // Reference bits 9:8, 11

#define HT_RACC1_HIGH 0x00 // Current range high for Channel-1
#define HT_RACC1_LOW 0x01 // Current range low for Channel-1
#define HT_ADSNF1_MDA Channel-1 // ADC measurement MDA pad (force) for
Channel-1
#define HT_ADSNF1_PLR 0x04 // ADC measurement PLR (sense) for
Channel-1

#define HT_RACC2_HIGH 0x00 // Current range high for Channel-2
#define HT_RACC2_LOW 0x10 // Current range low for Channel-2
#define HT_ADSNF2_MDA Channel-2 // ADC measurement MDA pad (force) for
Channel-2
#define HT_ADSNF2_PLR 0x40 // ADC measurement PLR (sense) for
Channel-2

//.....
```

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