iC-HG30
6 A LASER SWITCH

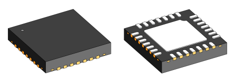
FEATURES

- Six channel laser switch from CW up to 250 MHz
- CW operation with up to 1 A per channel
- Pulsed operation with up to 5 A per channel
- Spike-free switching of the laser current
- 6 x 1 channels with TTL inputs
- 3 x 2 channels with LVDS inputs
- Operates as six independent voltage-controlled current sinks
- Outputs (LDKx) are 30 V capable for stacked laser diodes
- Simple current control at pins CIx
- CIx voltage < 3 V for full CW current
- Wide supply voltage range from 3 to 5.5 V
- All channels can be paralleled for up to 6 A CW and 30 A pulsed operation
- Open drain error output
- Thermal shutdown

APPLICATIONS

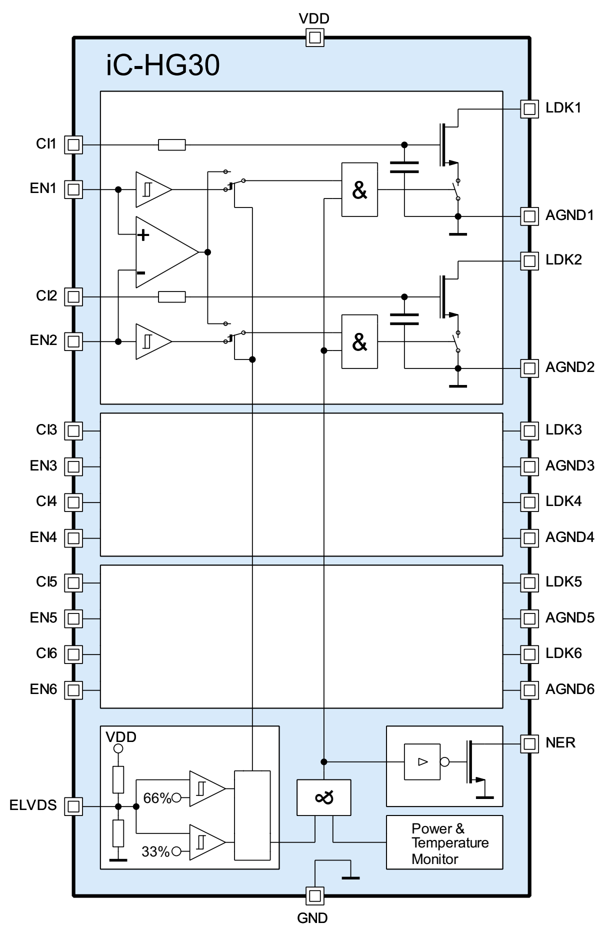
- TOF camera lighting
- LIDAR lighting
- Pump lasers
- Laser projection
- Laser TV
- Data transmission
- Camera lighting

PACKAGES



QFN28 5 mm x 5 mm

BLOCK DIAGRAM



DESCRIPTION

Six channel Laser Switch iC-HG30 enables the spike-free switching of laser diodes with well-defined current pulses at frequencies ranging from DC to 250 MHz.

The diode current is determined by the voltages at pins CIx.

The six fast switches are controlled independently via TTL inputs. Input ELVDS = hi selects LVDS type inputs and three channel mode.

The laser diode can thus be turned on and off or switched between different current levels (LDKx connected) defined by the voltages at CIx.

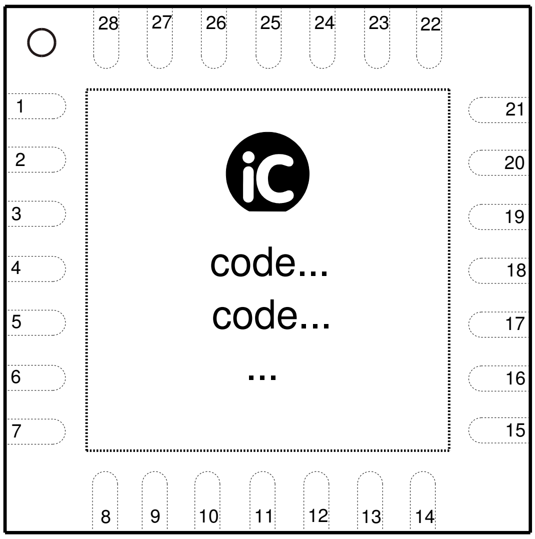
Each channel can be operated up to 1000 mA CW and 5000 mA pulsed current depending on the frequency, duty cycle and heat dissipation.

The integrated thermal shutdown feature protects the iC-HG30 from damage by excessive temperature.

iC-HG30 is compatible to iC-HG with LDKx voltages up to 30 V.

PACKAGING INFORMATION QFN28 5 mm x 5 mm to JEDEC

PIN CONFIGURATION QFN28 5 mm x 5 mm



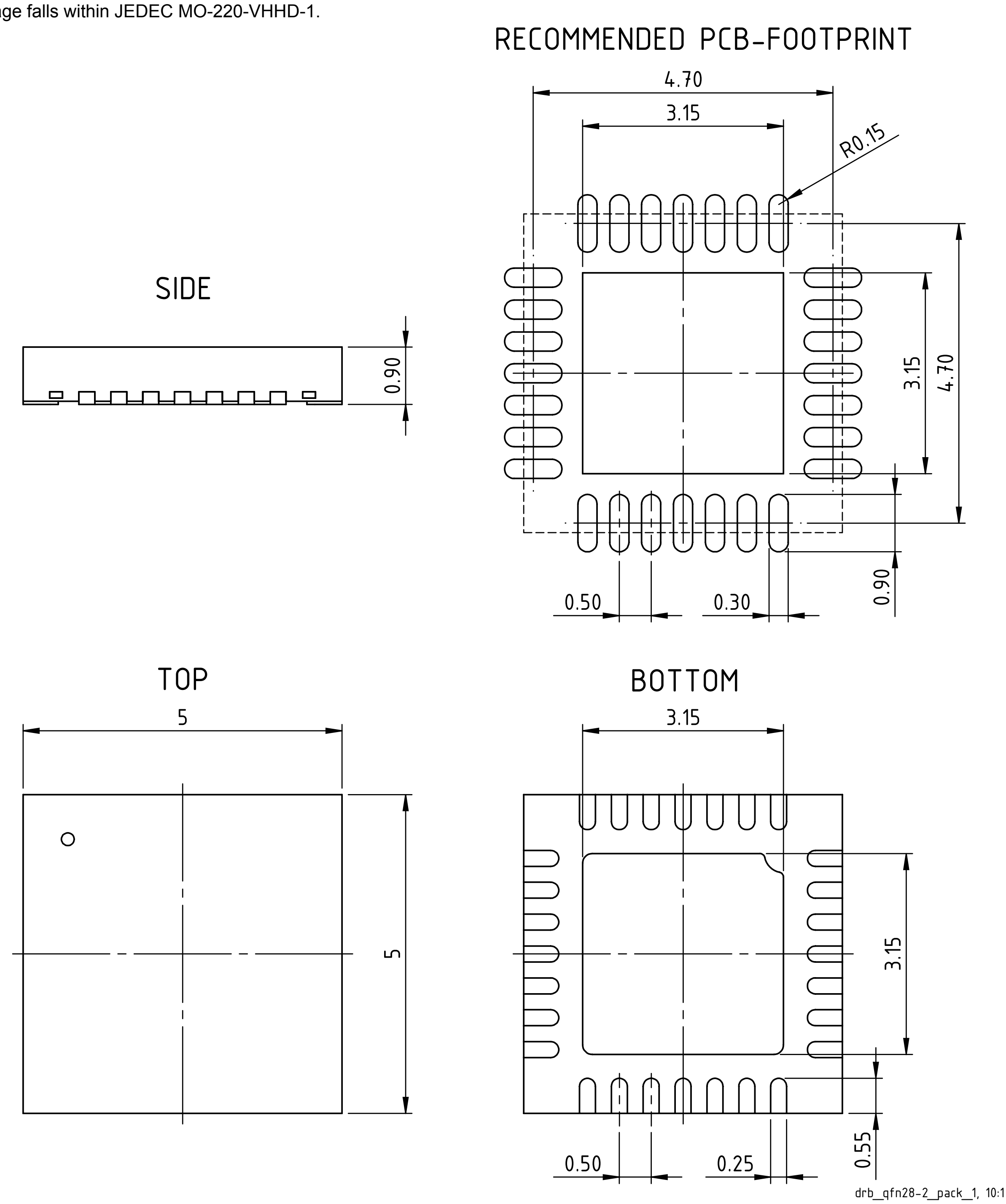
PIN FUNCTIONS

No.	Name	Function
1	CI1	Current control voltage channel 1
2	CI2	Current control voltage channel 2
3	CI3	Current control voltage channel 3
4	GND	Ground
5	CI4	Current control voltage channel 4
6	CI5	Current control voltage channel 5
7	CI6	Current control voltage channel 6
8	AGND6	Analog ground channel 6
9	LDK6	Laser diode cathode channel 6
10	AGND5	Analog ground channel 5
11	LDK5	Laser diode cathode channel 5
12	AGND4	Analog ground channel 4
13	LDK4	Laser diode cathode channel 4
14	EN6	TTL switching input channel 6 Negative LVDS Input channel 5 and 6
15	EN5	TTL switching input channel 5 Positive LVDS Input channel 5 and 6
16	EN4	TTL switching input channel 4 Negative LVDS Input channel 3 and 4
17	EN3	TTL switching input channel 3 Positive LVDS Input channel 3 and 4
18	VDD	Supply voltage
19	ELVDS	TTL/LVDS Fast/Slow Input selector
20	EN2	TTL switching input channel 2 Negative LVDS Input channel 1 and 2
21	EN1	TTL switching input channel 1 Positive LVDS Input channel 1 and 2
22	NER	Error monitor output
23	LDK3	Laser diode cathode channel 3
24	AGND3	Analog ground channel 3
25	LDK2	Laser diode cathode channel 2
26	AGND2	Analog ground channel 2
27	LDK1	Laser diode cathode channel 1
28	AGND1	Analog ground channel 1

The *Thermal Pad* is to be connected to a *Ground Plane* (GND, AGND1...6) on the PCB.
Only pin 1 marking on top or bottom defines the package orientation (iC HG30 label and coding is subject to change).

PACKAGE DIMENSIONS QFN28-5x5

All dimensions given in mm.
This package falls within JEDEC MO-220-VHHD-1.



ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.3	6	V
G002	I(VDD)	Current in VDD		-10	1200	mA
G003	V(CI)	Voltage at CI1...6		-0.3	6	V
G004	V()	Voltage at EN1...6, ELVDS, NER		-0.3	6	V
G005	V(LDK)	Voltage at LDK1...6		-0.3	30.5	V
G006	I(LDK)	Current in LDK1...6	DC current	-10	1000	mA
G007	I(AGND)	Current in AGND1...6	DC current	-1000	10	mA
G008	I()	Current in CI1...6, EN1...6, ELVDS		-10	10	mA
G009	I(NER)	Current in NER		-10	20	mA
G010	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G011	Tj	Operating Junction Temperature		-40	125	°C
G012	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended range on request)		-25		85	°C
T02	Rthja	Thermal Resistance Chip/Ambient	Mounted onto the Evaluation Board HG1D		25		K/W
T03	RthjTP	Thermal Resistance Chip/Thermal Pad			4		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0...5.5 V, AGND1...6 = GND, Tj = -40...125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device (x = 1...6)							
001	VDD	Permissible Supply Voltage		3		5.5	V
002	I(VDD)	Supply Current in VDD	CW operation			25	mA
003	I(VDD)	Supply Current in VDD	pulsed operation, f(ENx) = 250 MHz			1000	mA
004	V(LDKx)	Permissible Voltage at LDKx		-0.3		30	V
005	V(NER)	Permissible Voltage at NER		-0.3		5.5	V
006	Vc()hi	Clamp Voltage hi at LDKx	I(LDK) = 10 mA, t < 100 ms		35		V
007	Vc(NER)	Clamp Voltage hi at NER	I(NER) = 1 mA, t < 100 ms	7	8	9	V
008	Vc(CIx)hi	Clamp Voltage hi at CIx	I(CI) = 1 mA, t < 100 ms, other pins open	7	8	9	V
009	Vc()hi	Clamp Voltage hi at ENx, ELVDS	I() = 1 mA, t < 100 ms, other pins open	7	8	9	V
010	Vc()lo	Clamp Voltage lo at VDD, LDKx, CIx, ENx, ELVDS, NER	I() = -10 mA, other pins open	-1.6		-0.3	V
Laser Control LDK1...6, CI1...6 (x = 1...6)							
101	Icw(LDKx)	Permissible CW Current in LDKx (per channel)				1000	mA
102	Vs(LDKx)	Saturation Voltage at LDKx	I(LDKx) = 900 mA, V(CIx) = V(CIx)@I(LDKx) = 1000 mA			2	V
103	I0(LDKx)	Leakage Current in LDKx	ENx = lo, V(LDKx) < 30 V			200	µA
104	tr()	LDKx Current Rise Time Fast	Iop(LDKx) = 1000 mA, I(LDKx): 10% → 90% Iop, V(ELVDS) = 0 V or VDD			1*	ns
105	tf()	LDKx Current Fall Time Fast	Iop(LDKx) = 1000 mA, I(LDKx): 90% → 10% Iop, V(ELVDS) = 0 V or VDD			1*	ns
106	tp()	Propagation Delay V(ENx) → I(LDKx)	V(ELVDS) = 0 V or VDD, Differential LVDS Rise and Fall Time < 0.5 ns	3	5	14	ns
107	CR()	Current Matching all Channels		0.9		1.1	
108	V(CIx)	Permissible Voltage at CIx		-0.3		5.5	V
109	Vt(CIx)	Threshold Voltage at CIx	I(LDKx) < 5 mA	0.5		1.2	V
110	V(CIx)	Operating Voltage at CIx	I(LDKx) = 1000 mA, V(LDKx) > 2.3 V		2	2.9	V
111	R(CIx)	Pull-down resistor at CI		200	500	1250	kΩ
112	C(CIx)	Capacity at CIx	V(CIx) = 2 V		1100		pF
113	Vc(LDKx)	Clamp Voltage at LDKx	I(LDKx) = 100 mA, tclamp < 100 ms, tclamp/T < 1:100	30.5		45	V
114	tskc()	Channel to Channel Skew				160†	ps
115	tskp()	Part to Part Skew	best to worst			4†	ns
Input EN1...6 (x = 1...6)							
201	Vt(TTL)hi	Input Threshold Voltage hi	V(ELVDS) < 20% VDD, TTL			2	V
202	Vt(TTL)lo	Input Threshold Voltage lo	V(ELVDS) < 20% VDD, TTL	0.8			V
203	Vhys(TTL)	Hysteresis	Vhys() = Vt()hi − Vt()lo; V(ELVDS) < 20% VDD, TTL	50			mV
204	R(ENx)	Pull-Down Resistor	V(ELVDS) < 20% VDD, TTL	80	200	500	kΩ
205	R(EN1,3,5)	Pull-Down Resistor	V(ELVDS) > 80% VDD, LVDS	80	200	500	kΩ
206	R(EN2,4,6)	Pull-UP Resistor	V(ELVDS) > 80% VDD, LVDS	80	200	500	kΩ
207	Vdiff	Differential Voltage	Vdiff = |V(EN1,3,5) − V(EN2,4,6)|; V(ELVDS) > 80% VDD, LVDS	200			mV
208	V()	Input Voltage Range	V(ELVDS) > 80% VDD, LVDS	-0.2		VDD + 0.2	V
Input ELVDS							
301	V(ELVDS)	Voltage at ELVDS	ELVDS open	48	50	52	%VDD
302	Ri(ELVDS)			30	50	80	kΩ
303	Vt(ELVDS)	Threshold Voltage TTL to Error		25	33	40	%VDD

* Projected values by sample characterization
† Projected values by simulation

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0...5.5 V, AGND1. . . 6 = GND, Tj = -40...125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
304	Vt(ELVDS)	Threshold Voltage Error to LVDS		59	66	73	%VDD
305	Vhys()	Hysteresis		10	25	100	mV
Ouput NER							
401	Vsat(NER)	Saturation Voltage at NER	ELVDS open, I(NER) = 2 mA			0.6	V
402	I(NER)	Current in NER	ELVDS open, V(NER) > 0.6 V	3	9	20	mA
Overtemperature							
501	Toff	Overtemperature Shutdown	rising temperature	130		170	°C
502	Ton	Overtemperature Release	falling temperature	120		160	°C
503	Thys	Hysteresis	Toff – Ton	5			°C
Power On							
601	VON	Power On Voltage VDD	rising voltage			2.9	V
602	VOFF	Power Down Voltage VDD	falling voltage	1.2			V
603	Vhys	Hysteresis		50		800	mV

CONFIGURATION INPUT ELVDS

Pin ELVDS selects between *6 channel TTL mode* mode or *3 channel LVDS mode*. The unconnected pin ELVDS is an error condition signaled at pin NER with the laser current disabled.

Pin ELVDS connected to GND selects the six channel fast TTL mode. Pin ELVDS connected to VDD selects the three channel fast LVDS mode.

DIGITAL INPUTS EN1...6

EN1...6 are the digital switching inputs. With pin ELVDS set to *6 channel TTL mode*, each pin ENx enables the current sink at the respective LDKx. With pin ELVDS set to *3 channel LVDS mode*, the odd ENx pins are the positive and the even ENx pins are the negative LVDS inputs. EN1 and EN2 control LDK1 and LDK2, EN3 and EN4 control LDK3 and LDK4 and EN5 and EN6 control LDK5 and LDK6. For correct LVDS operation 100 Ω terminating resistors between the respective EPx and ENx pins, very close to the inputs, are strongly recommended. Input pins from unused channels have to be connected to GND (TTL operation) resp. EPx to GND and ENx to VDD (LVDS operation).

ANALOG CURRENT CONTROL VOLTAGE INPUTS CI1...6

The voltage at pins CI1...6 sets the current in pins LDK1...6. Figures 1 and 2 show the temperature dependency of the current in a single LDKx output versus the voltage at CIx for a *typical* device. Figures 3 and 4 show the min., typ. and max. variations between devices at 27 °C temperature. The voltage at pins LDKx is 2.5 V.

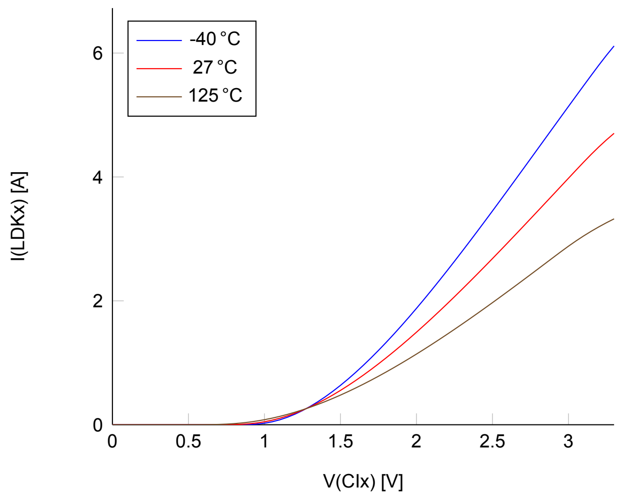


Figure 1: I(LDKx) vs. V(CIx) at VDD = 3.3 V

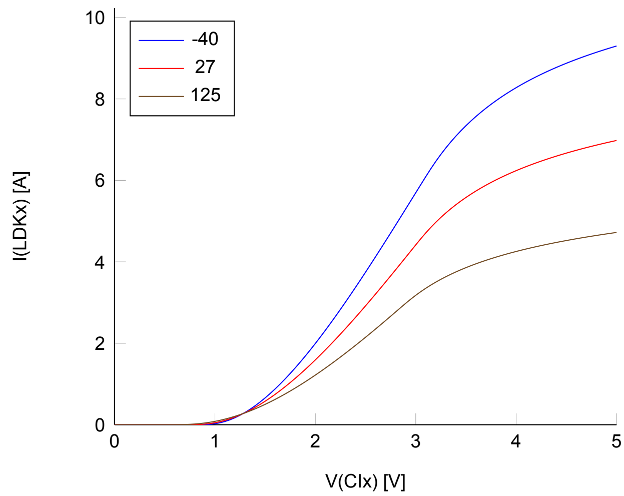


Figure 2: I(LDKx) vs. V(CIx) at VDD = 5 V

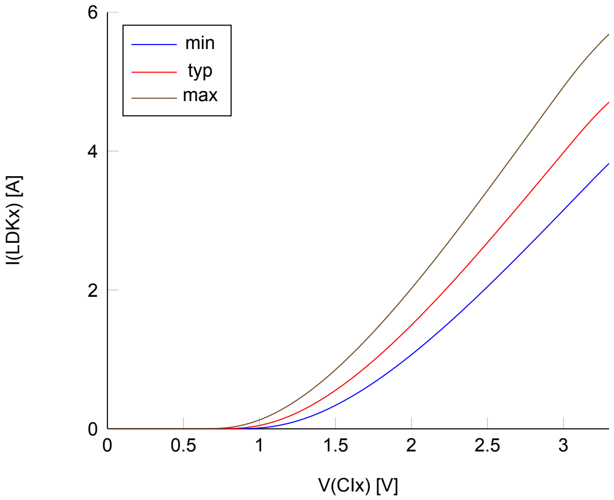


Figure 3: I(LDKx) vs. V(CIx) at VDD = 3.3 V

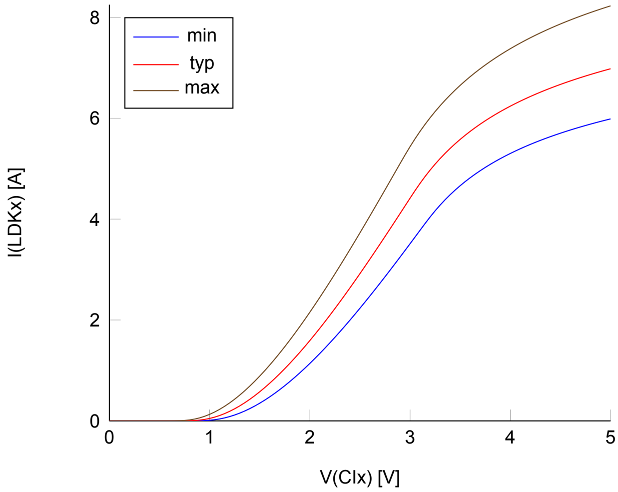


Figure 4: I(LDKx) vs. V(CIx) at VDD = 5 V

LASER OUTPUTS LDK1...6

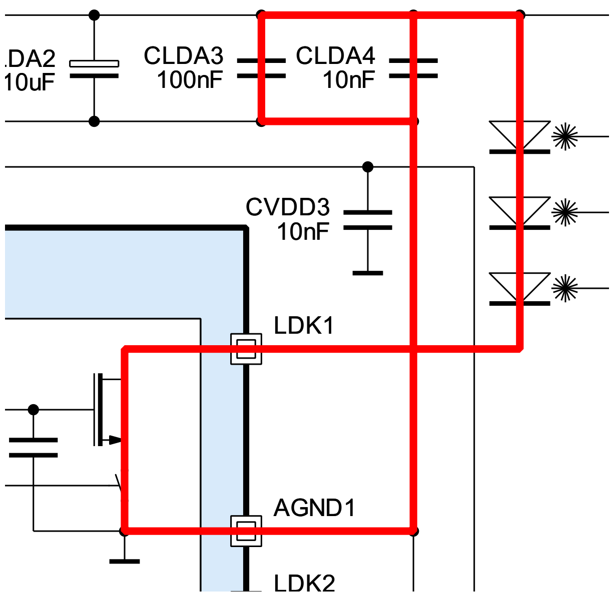


Figure 5: Current loop

LDK1...6 are the current outputs for the laser diode cathode. For high speed operation, connect the laser diode as close as possible to this pins to minimize the inductance. To ensure a high switching speed, it is important to minimise the inductance of the whole current loop (cf. Figure 5, marked red) consisting of iC-HG30 (pins LDKx and AGNDx), the laser diode (anode and cathode), the bypass capacitors as well as the enclosed area. It may still be necessary though to use an R/C snubber network for damping L/C oscillations.

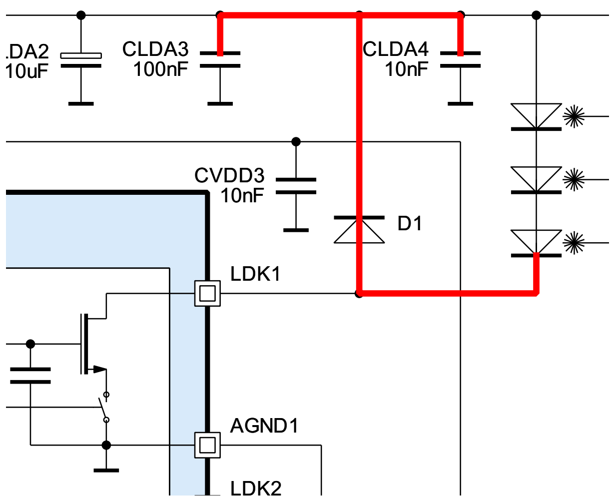


Figure 6: Free-wheeling diode

Depending on the residual inductance in the laser current path and the actual laser current, fast free-wheeling diodes from LDKx to VLDA may be required (cf. Figure 6, diode D1) to protect the outputs. The anode of the free-wheeling diode should be close to the to be protected LDKx output and the cathode close to the bypass capacitors at VLDA for the free-wheeling current to be dumped into, when switching the respective channel off.

Figure 7 shows the typical output characteristics of LDK. The left hand side of the diagram is the RDSon region where the current depends strongly on the voltage at LDK. The right hand side of the diagram is the current source region where the current depends only somewhat on the voltage at LDK. Only the current source region is to be used.

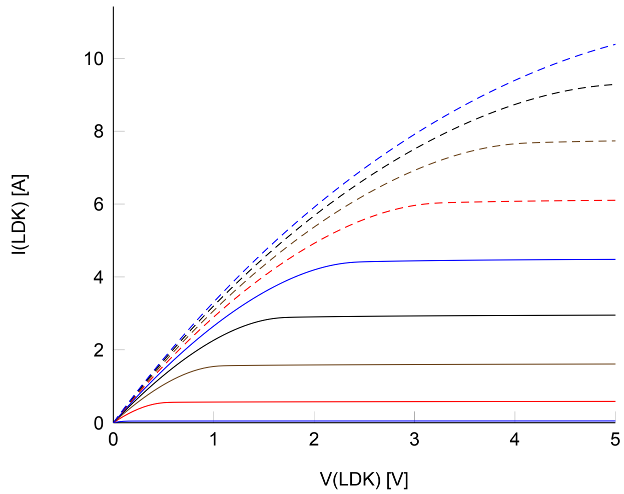


Figure 7: Output Characteristics of LDK

PULSED OPERATION

The current for pulsed operation may be higher than for CW operation. Therefore the RMS current of the pulse train has to be considered.

$$I_{pulse_{max}} = I_{CW_{max}} \cdot \sqrt{\frac{repetition\ time(T)}{pulse\ time(t)}} \qquad (1)$$

With $I_{CW_{max}}$ from Electrical Characteristics No. 101 and pulses < 10 µs. So for a single channel operated with a 50% duty cycle, the max. laser current becomes

$$I_{pulse_{max}} = 1000\,mA \cdot \sqrt{2} = 1414\,mA$$

ANALOG GROUNDS AGND1...6

AGND1...6 are the ground pins for the channels. It is recommended to connect all AGND1...6 pins to GND.

ERROR OUTPUT NER

The open drain pin NER is a low-active error output. Signalled errors are ELVDS open or at 50% VDD, VDD undervoltage and thermal shutdown.

THERMAL SHUTDOWN

iC-HG30 is protected by an integrated thermal shutdown feature. When the shutdown temperature is reached all channels are disabled. Falling temperature after this shutdown will unconditionally enable all channels again. Necessary precaution to prevent damage of the laser may be to also disable any external control circuits for the laser output power or current control during thermal shutdown. The error signal at pin NER can be used to e.g. disable the control circuit.

APPLICATION EXAMPLES

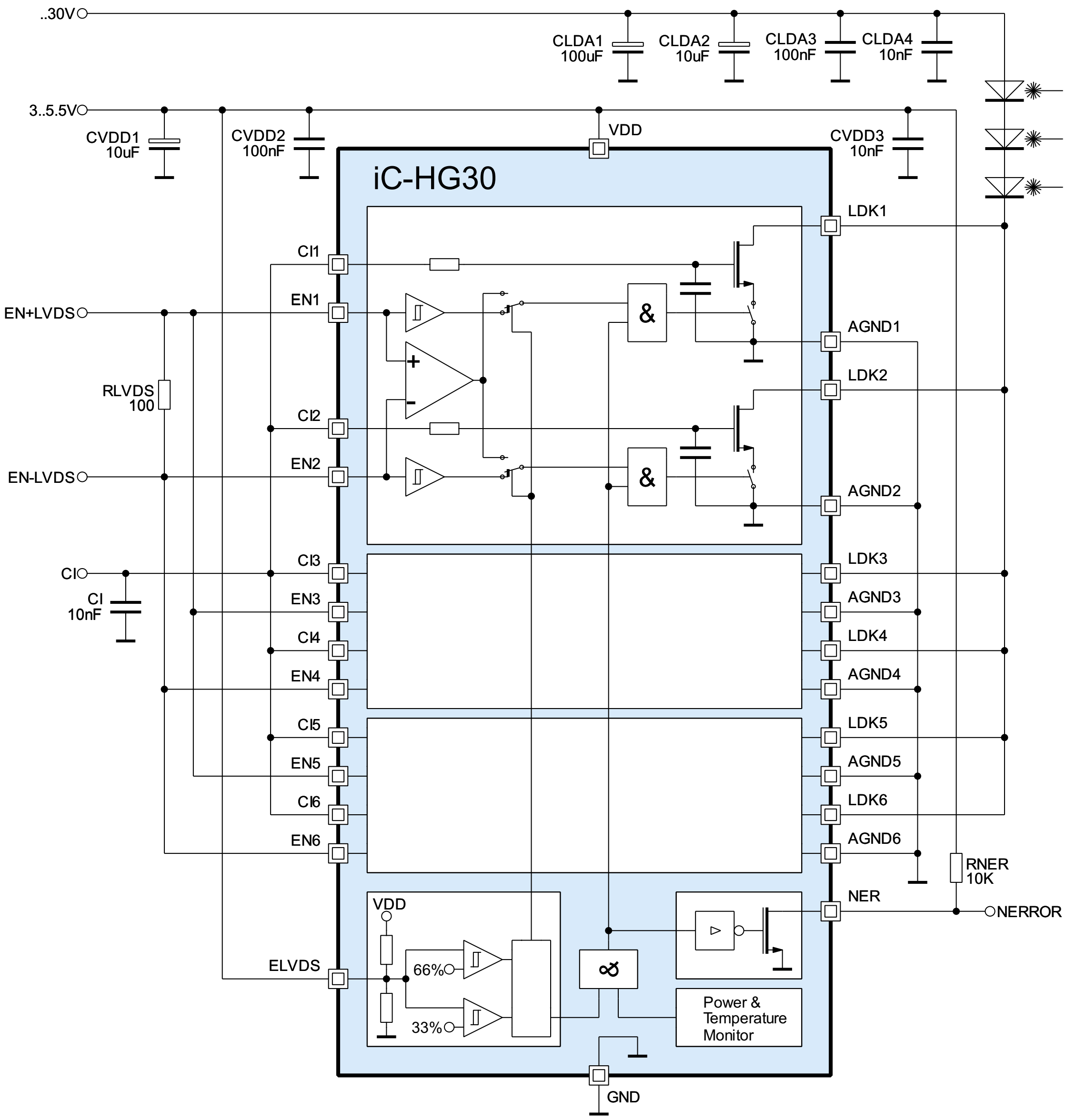


Figure 8: 1 channel LVDS

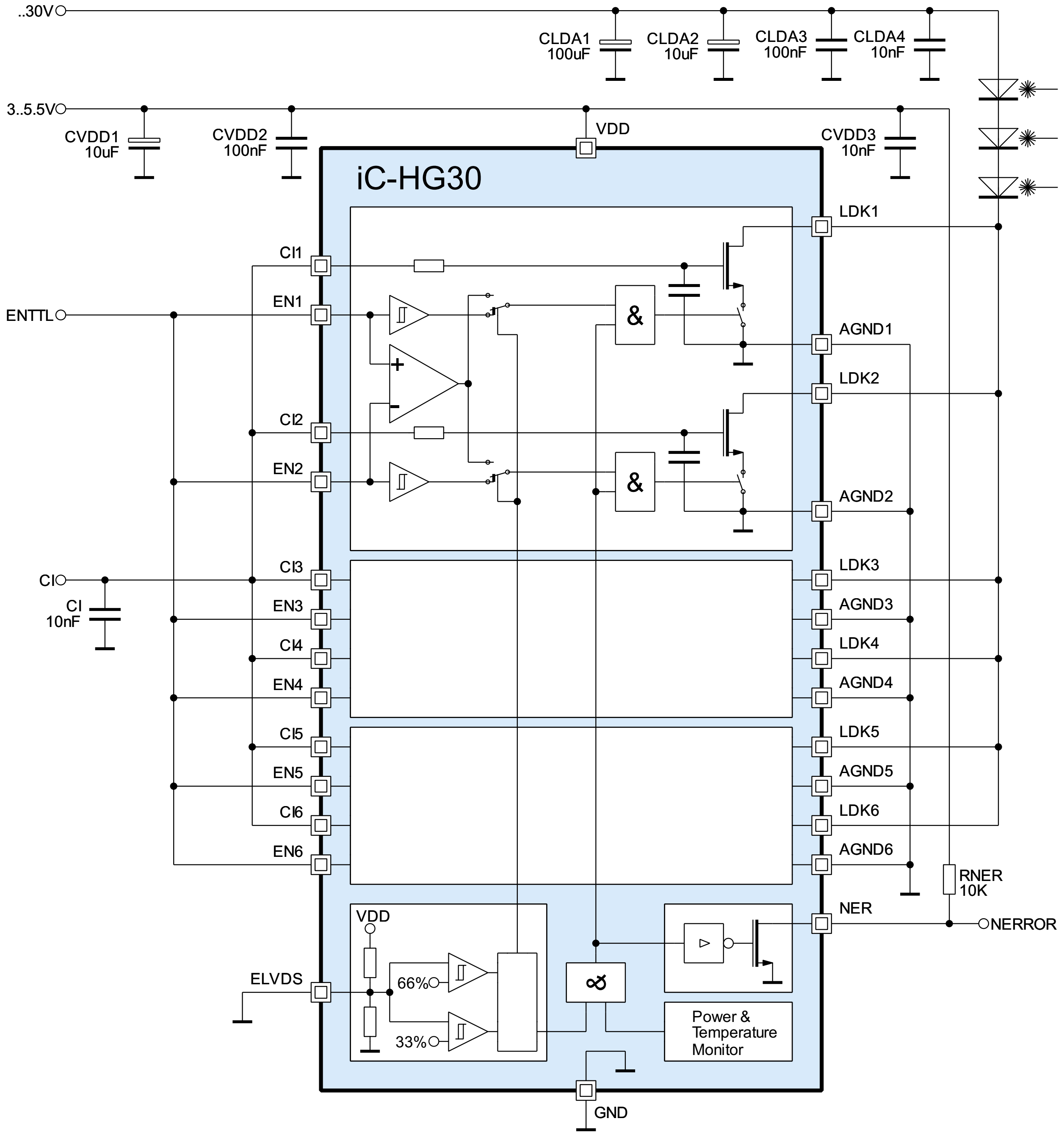


Figure 9: 1 channel TTL

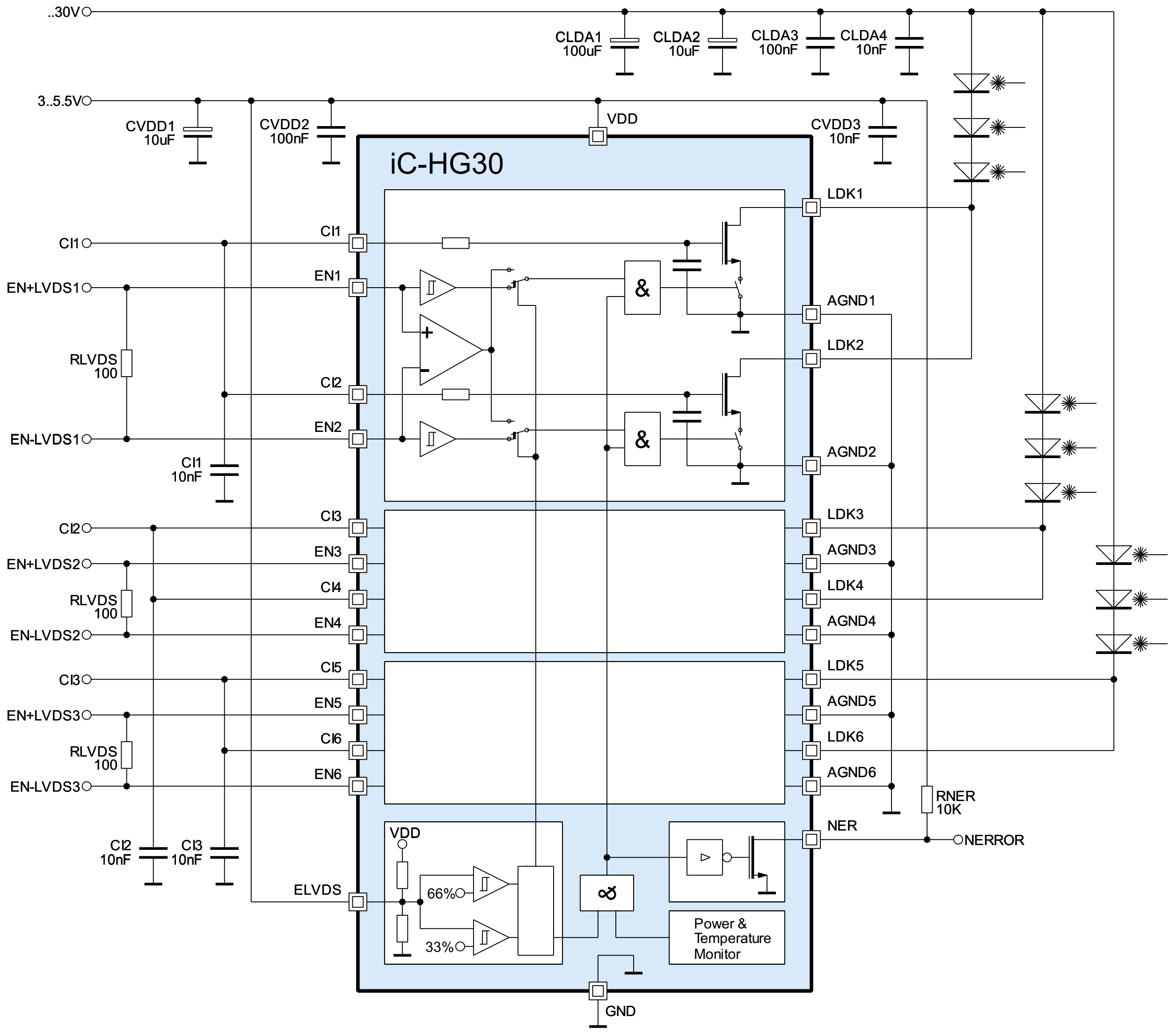


Figure 10: 3 channel LVDS

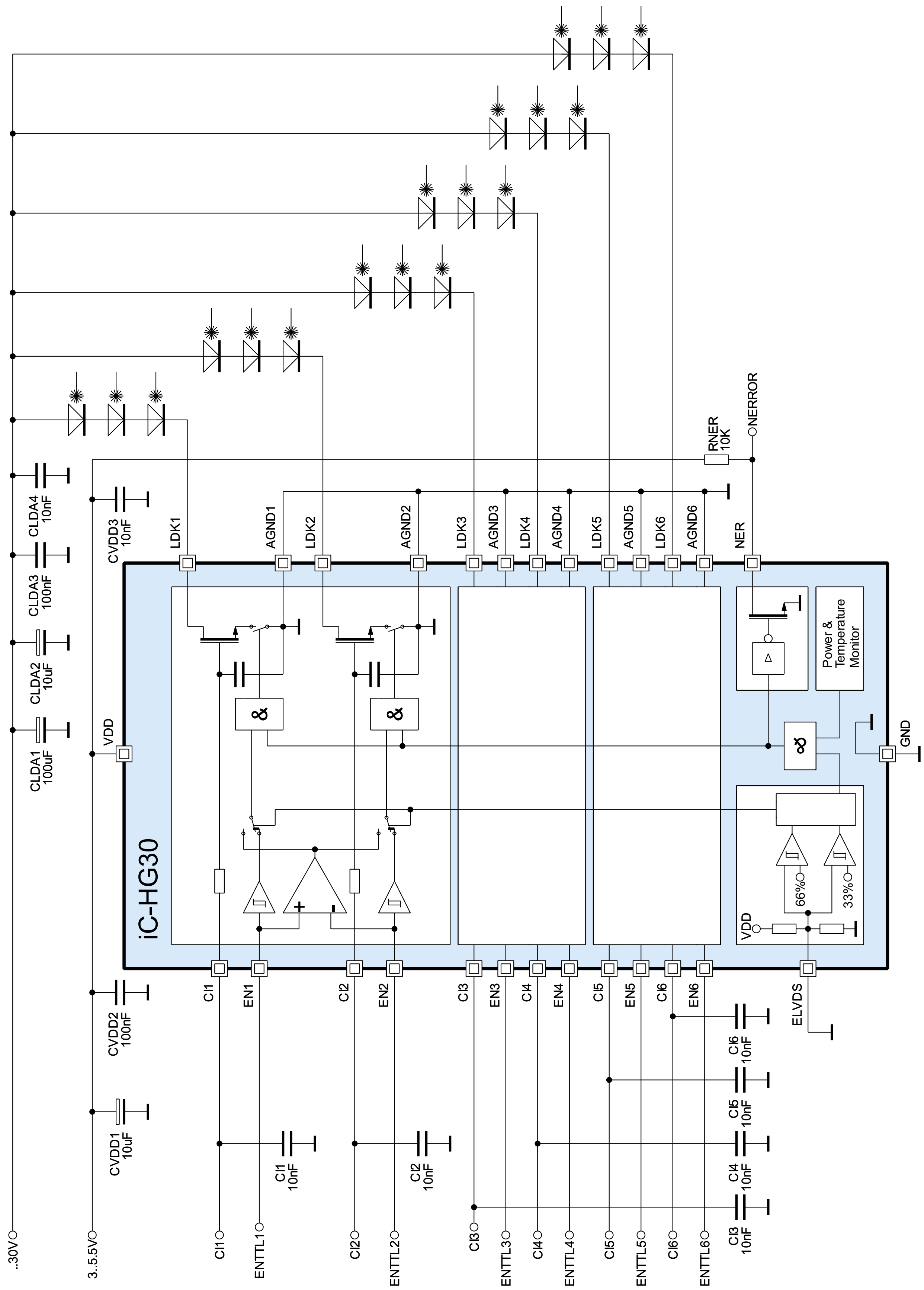


Figure 11: 6 channel TTL

EVALUATION BOARD

iC-HG30 comes with the iC-HG evaluation board for test purpose. Figures 12 and 13 show both the schematic and the component side of the evaluation board.

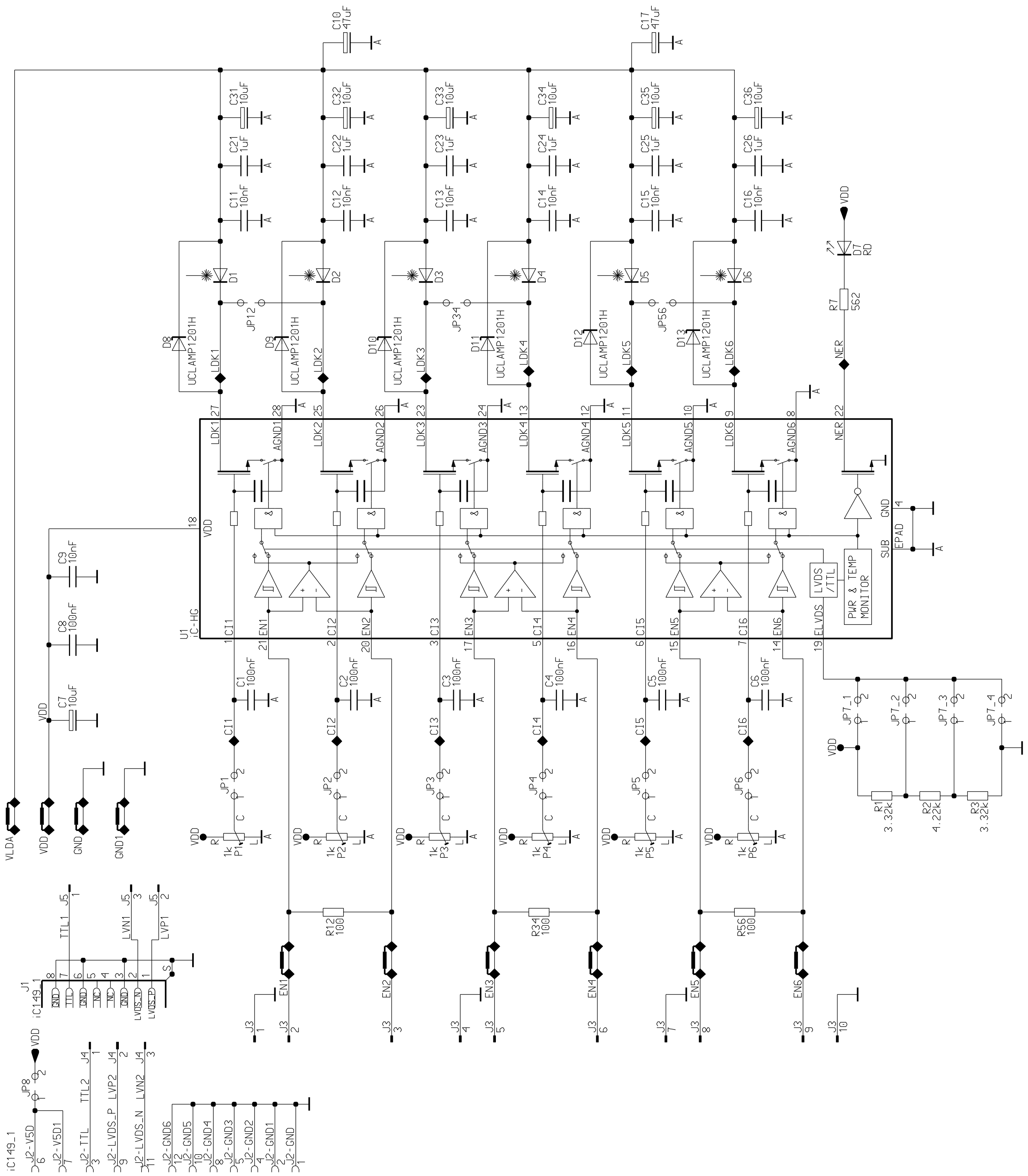


Figure 12: Schematic of the evaluation board

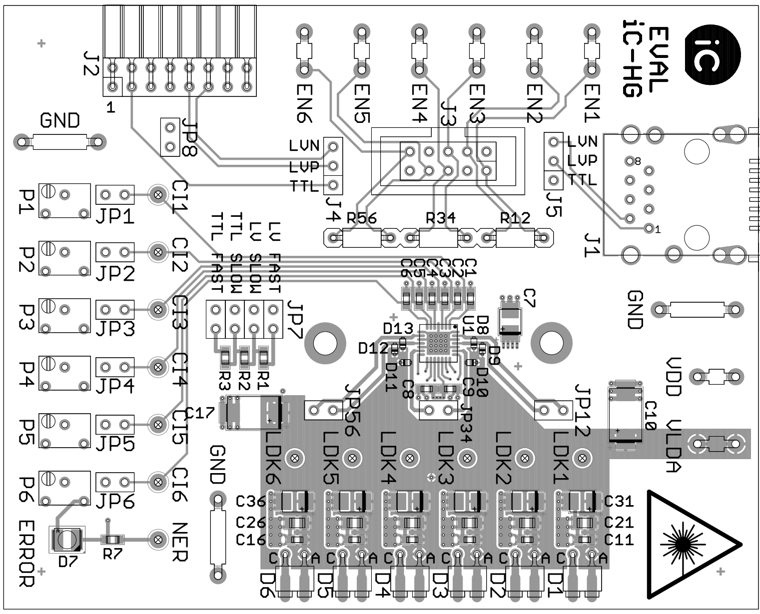


Figure 13: Evaluation board (component side)

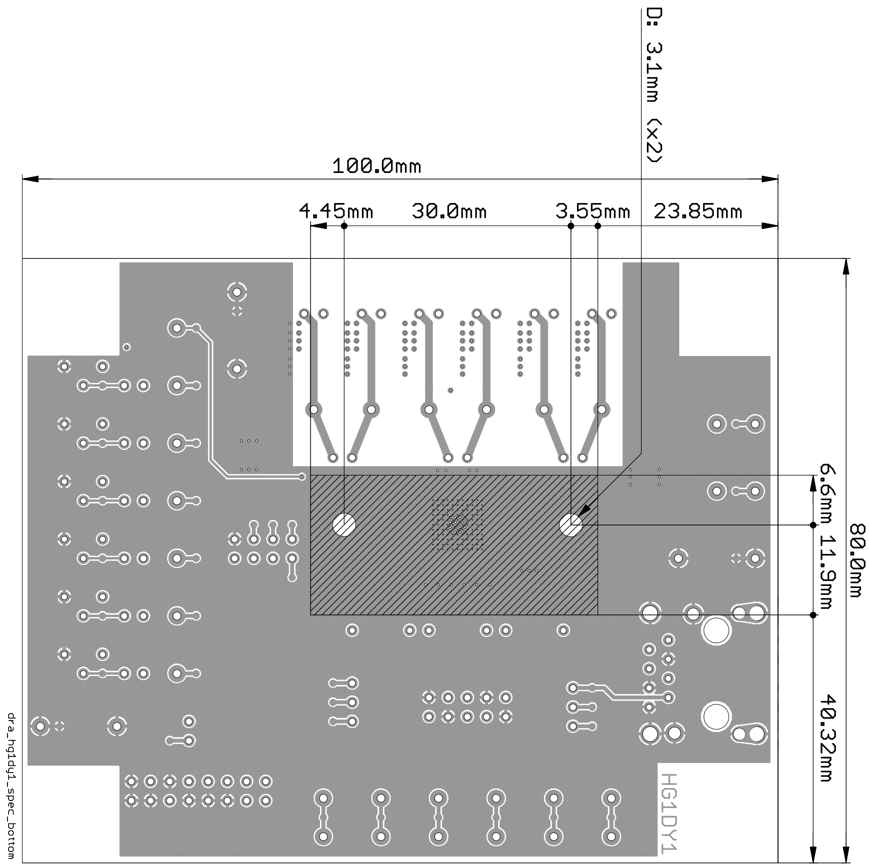


Figure 14: Evaluation board (solder side) with mounting option for heat sink

REVISION HISTORY

Rel.	Rel. Date‡	Chapter	Modification	Page
A1	2019-10-11		Initial release	all

‡ Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-HG30	QFN28 5 mm x 5 mm		iC-HG30 QFN28-5x5
	General Purpose Evaluation Board		iC-HG30 EVAL HG1D
	Host adapter for high-speed modules		iC-HG EVAL HG2D
	Host adapter for high-speed modules	heat-sink assembly kit	iC-HG EVAL HG2D-HSK
	High-speed module for C-mount laser diodes		iC-HG30 iCSY HG2M
	High-speed module for TO type laser diodes		iC-HG30 iCSY HG8M
	High-speed module for SMD type VCSEL arrays, laser diodes or LEDs		iC-HG30 iCSY HG20M
	High-speed module for SMD type VCSEL arrays, laser diodes or LEDs (alternative pad layout)		iC-HG30 iCSY HG21M

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