

iC-HF EVAL HF1D

EVALUATION BOARD DESCRIPTION

ORDERING INFORMATION

Type	Order Designation	Description Options
Evaluation Board	iC-HF EVAL HF1D	iC-HF Evaluation Board
ready to operate: <i>Encoder Link Sequence</i> and power down available through on-board microcontroller and buttons.		

BOARD HF1D AND TERMINAL DESCRIPTION

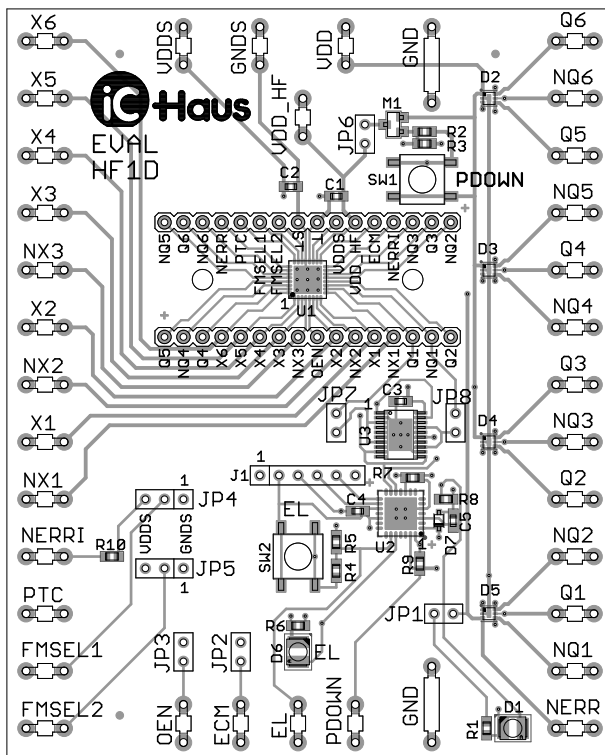


Figure 1: Component side (size 100 mm x 80 mm)

TERMINAL DESCRIPTION

J1	<i>Encoder Link</i> generator programming interface
J2	iC-HF device signals
J3	iC-HF device signals
VDD	Digital Supply
GND	Digital Ground
VDDDS	Switched Power Supply output
GNDS	Switched Ground output
X1	Channel 1 positive input
NX1	Channel 1 negative input
X2	Channel 2 positive input
NX2	Channel 2 negative input
X3	Channel 3 positive input
NX3	Channel 3 negative input
X4	Channel 4 positive input
X5	Channel 5 positive input
X6	Channel 6 positive input
Q1	Channel 1 positive output
NQ1	Channel 1 negative output
Q2	Channel 2 positive output
NQ2	Channel 2 negative output
Q3	Channel 3 positive output
NQ3	Channel 3 negative output
Q4	Channel 4 positive output
NQ4	Channel 4 negative output
Q5	Channel 5 positive output
NQ5	Channel 5 negative output
Q6	Channel 6 positive output
NQ6	Channel 6 negative output
NERR	Error Output (low active)
NERRI	Error Input (low active)
PTC	PT configuration output
FMSEL1	Function Mode Select 1 input
FMSEL2	Function Mode Select 2 input
OEN	Output Enable input
ECM	Enable <i>Encoder Link state</i> input

CIRCUIT DESCRIPTION

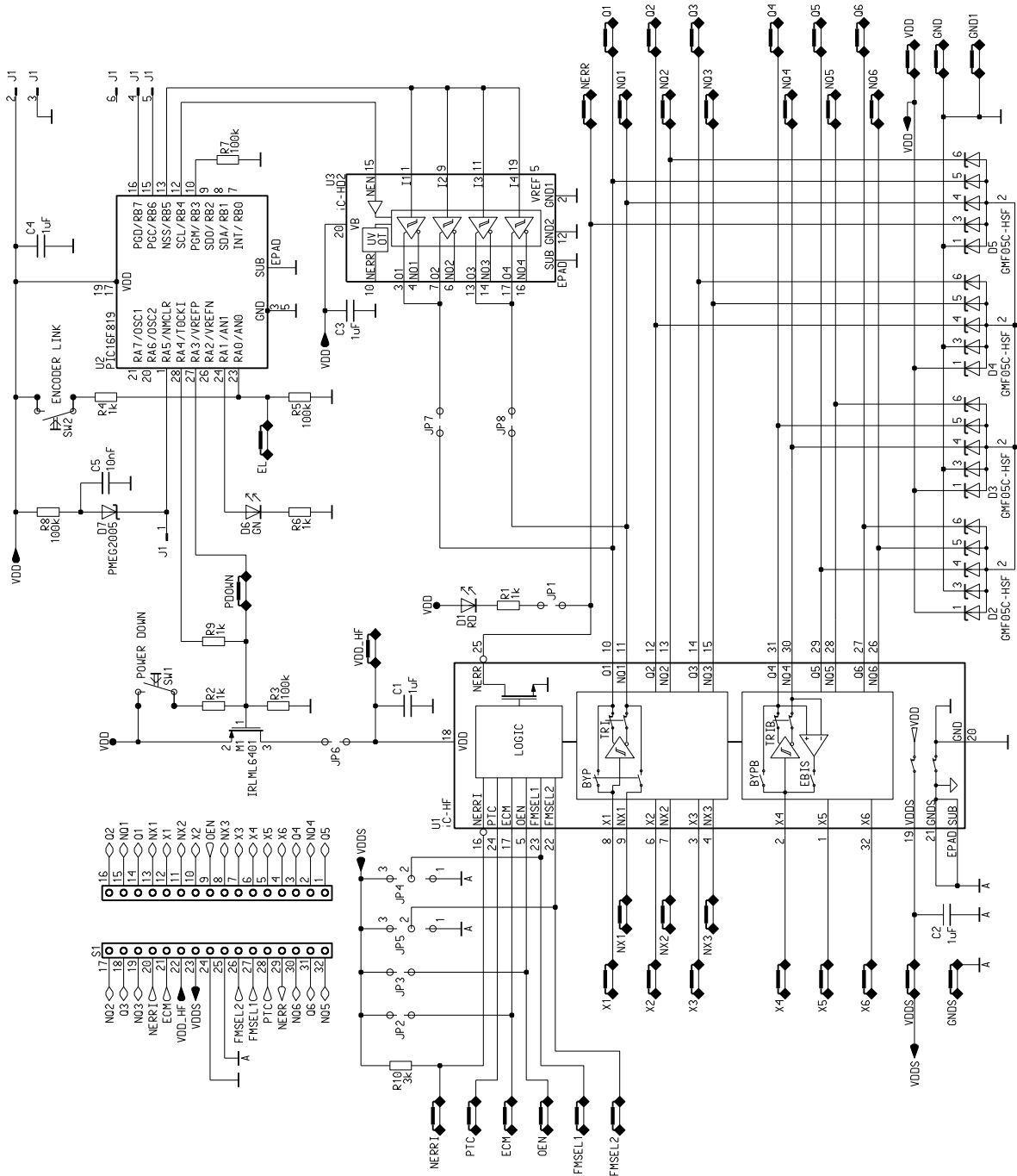


Figure 2: Circuit diagram

Note:HF1D is only designed to handle 5V RS422 signals on the serial BiSS interface. Please see chapter "BiSS INTERFACE LINE TRANSCEIVER" on page 7.

iC-HF EVAL HF1D

EVALUATION BOARD DESCRIPTION



Rev B2, Page 3/8

ASSEMBLY PART LIST

Device	Value (typical)	Comment
PCB	HF1D	
C1, C2, C3, C4	1 μ F	Tolerance 10% X7R 16V SMD 0603
C5	10 nF	Tolerance 10% X7R 16V SMD 0603
D1	LS-T67K	NERR LED red, SMD PLCC2
D2, D3, D4, D5	GMF05C-HSF	TVS array SMD SOT363
D6	LG-T67K	<i>Encoder Link</i> LED green, SMD PLCC2
D7	PMEG2005A	SMD SOD323
M1	IRLML6401	VDD Switch SMD SOT23
R1, R2, R4, R6, R9	1k Ω	Tolerance 1% SMD 0603
R3, R5, R7, R8	100k Ω	Tolerance 1% SMD 0603
R10	3k Ω	Tolerance 1% SMD 0603
SW1, SW2	Switch B3S	Push button SMD
U1	iC-HF	6-CHAN. RS422 Encoder Link SMD QFN32
U2	PIC16F819	PIC Microcontroller SMD QFN28
U3	iC-HD2	Line driver SMD TSSOP20
ECM, EL, FMSEL1, FMSEL2, GNDS, NERR, NERRI, Q1...6, NQ1...6, X1...6, NX1...3, OEN, PDOWN, PTC, VDD, VDDS, VDD_HF	Jumperlink 34	TH 200mil
GND, GND1	Jumperlink 2	TH 400mil
JP1, JP2, JP3	CONN 3 SLLP10972G	TH W2X1
JP4, JP5, JP6, JP7, JP8	CONN 2 SLLP10973G	TH W3X1
J1	CONN 0	TH W6X1
S1_1, S1_2	CONN 0	TH S16X1
RF1, RF2, RF3, RF4	12,7 mm x 12,7 mm x 5,6 mm	Rubberfoot

iC-HF EVAL HF1D

EVALUATION BOARD DESCRIPTION

BOARD AND CONNECTOR PINOUT

J1: PIC programmer interface

6-pin Connector pads

PIN	Name	Function
1 ... 6		PIC programmer interface

J2: iC-HF signals

16-pin Connector - female

PIN	Name	Function
29	Q5	Channel 5 positive output
30	NQ4	Channel 4 negative output
31	Q4	Channel 4 positive output
32	X6	Channel 6 positive input
1	X5	Channel 5 positive input
2	X4	Channel 4 positive input
3	X3	Channel 3 positive input
4	NX3	Channel 3 negative input
5	OEN	Output Enable input
6	X2	Channel 2 positive input
7	NX2	Channel 2 negative input
8	X1	Channel 1 positive input
9	NX1	Channel 1 negative input
10	Q1	Channel 1 positive output
11	NQ1	Channel 1 negative output
12	Q2	Channel 2 positive output

J3: iC-HF signals

16-pin Connector - female

PIN	Name	Function
13	NQ2	Channel 2 negative output
14	Q3	Channel 3 positive output
15	NQ3	Channel 3 negative output
16	NERRI	Error Input (low active)
17	ECM	Enable <i>Encoder Link state</i> input
18	VDD	Power Supply Voltage
19	VDDS	Switched Power Supply output
20	GND	Ground
21	GNDS	Switched Ground output
22	FMSEL2	Function Mode Select 2 input
23	FMSEL1	Function Mode Select 1 input
24	PTC	PT configuration output
25	NERR	Error Output (low active)
26	NQ6	Channel 6 negative output
27	Q6	Channel 6 positive output
28	NQ5	Channel 5 negative output

JUMPER DESCRIPTION

Jumper	Pin 1	Pin 2	Pin 3	Default Setting
JP1	NERR	D1 LED	n.a.	1-2 jumpered
JP2	ECM	VDDS	n.a.	1-2 open
JP3	OEN	VDDS	n.a.	1-2 jumpered
JP4	GNDS	FMSEL1	VDDS	1-2 jumpered
JP5	GNDS	FMSEL2	VDDS	1-2 jumpered
JP6	VDDS iC-HF	VDD	n.a.	1-2 jumpered
JP7	Q1	Q1+2 of iC-HD2	n.a.	1-2 jumpered
JP8	NQ1	Q3+4 of iC-HD2	n.a.	1-2 jumpered

BUTTON DESCRIPTION

Button	Label	Default Setting
SW1	PDOWN	Interrupts iC-HF VDD supply through transistor M1
SW2	EL	Triggers <i>Encoder Link Sequence</i> generated through the microcontroller U2

ENCODER LINK SEQUENCE GENERATOR

The eval board HF1D has an on board **Encoder Link** generator. This generator creates the precise timing sequence on Q1 and NQ1 to switch into the *Encoder Link state*.

Startup indication

The *Encoder Link Sequence* Generator indicates its startup by a short blink sequence on LED D6 after the power up.

The *Encoder Link Sequence* Generator is based on a microcontroller (MCU) and the iC-HD2 line driver.

The microcontroller does detect the power up cycle and the power down.

Multiple *Encoder Link Sequence* can be executed with the **Encoder Link** generator.

Even with the iC-HF in the *Encoder Link state* the *Encoder Link Sequence* can still be executed with the **Encoder Link** generator.

Encoder Link Sequence Execution indication

The *Encoder Link Sequence* LED D6 indicates the executed *Encoder Link Sequence* by permanent light after the power up. A power down will reset the LED D6.

Encoder Link Sequence Execution

The *Encoder Link Sequence* is manually started by user pushing and releasing the **EL** button (magenta signal 3). The on board MCU does generate the *Encoder Link Sequence* circa 330 msec after the falling edge/release of the button (to prevent key bouncing).

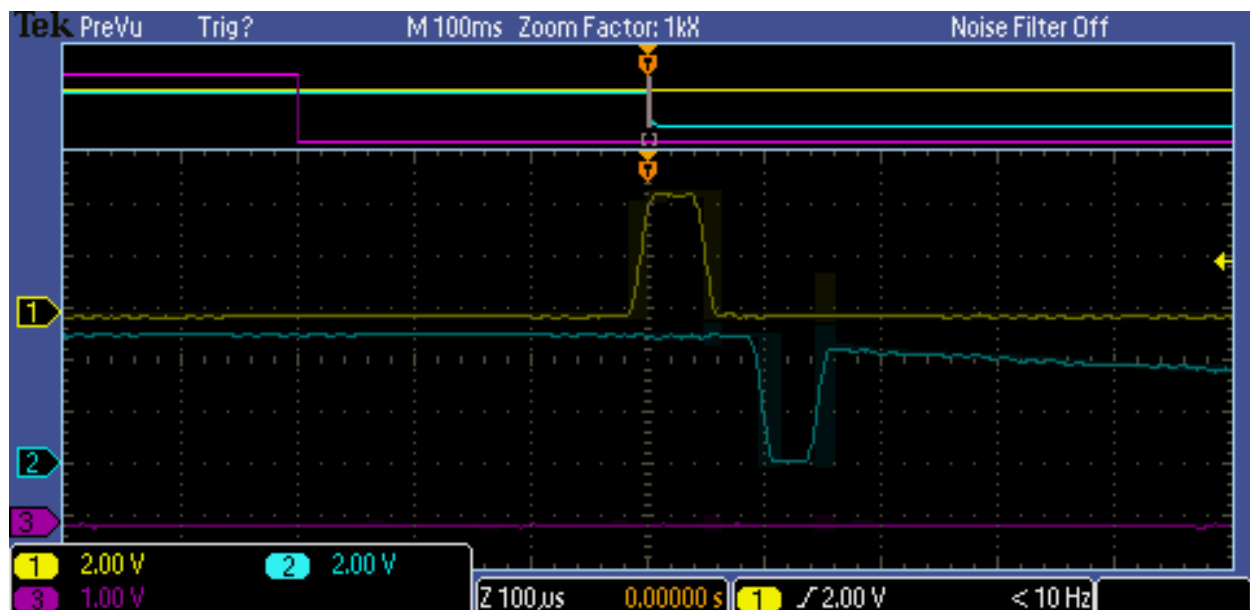


Figure 3: Falling edge of EL button triggers *Encoder Link Sequence*

Encoder Link Sequence Execution with Q1 = 0

The *Encoder Link Sequence* forces both output pins Q1 (yellow signal 1) and NQ1 (blue signal 2) to a high, disabled and low state with a dedicated timing.

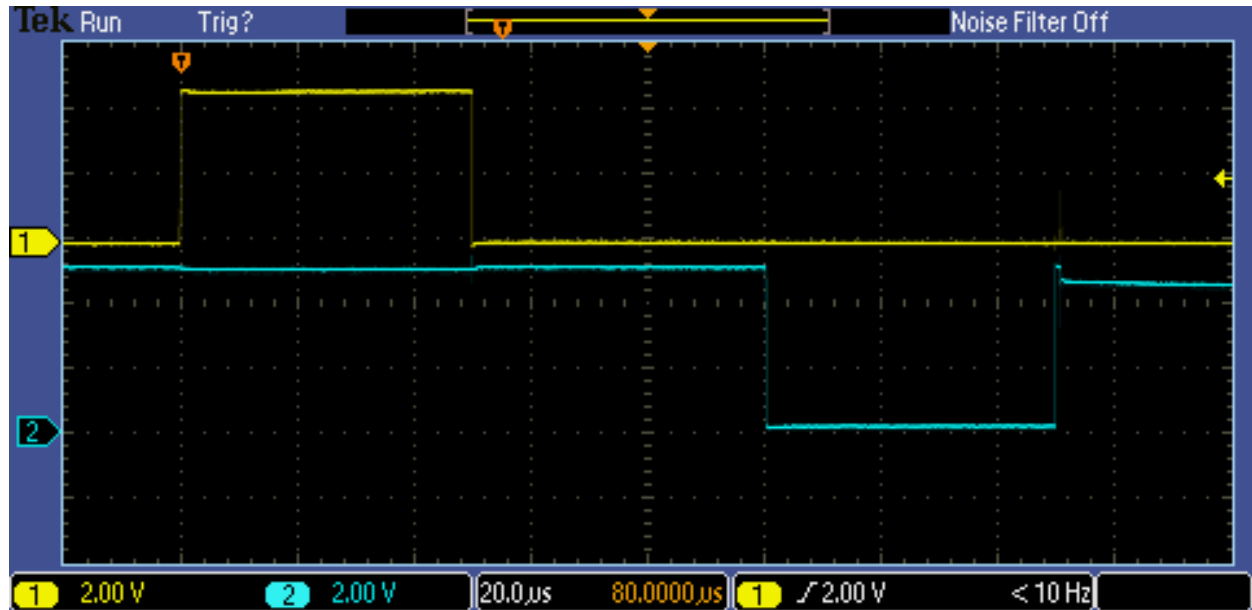


Figure 4: *Encoder Link Sequence* with a prior X1 = Q1 = 0

Encoder Link Sequence Execution with Q1 = 1

The *Encoder Link Sequence* forces both output pins Q1 (yellow signal 1) and NQ1 (blue signal 2) to a high, disabled and low state with a dedicated timing.

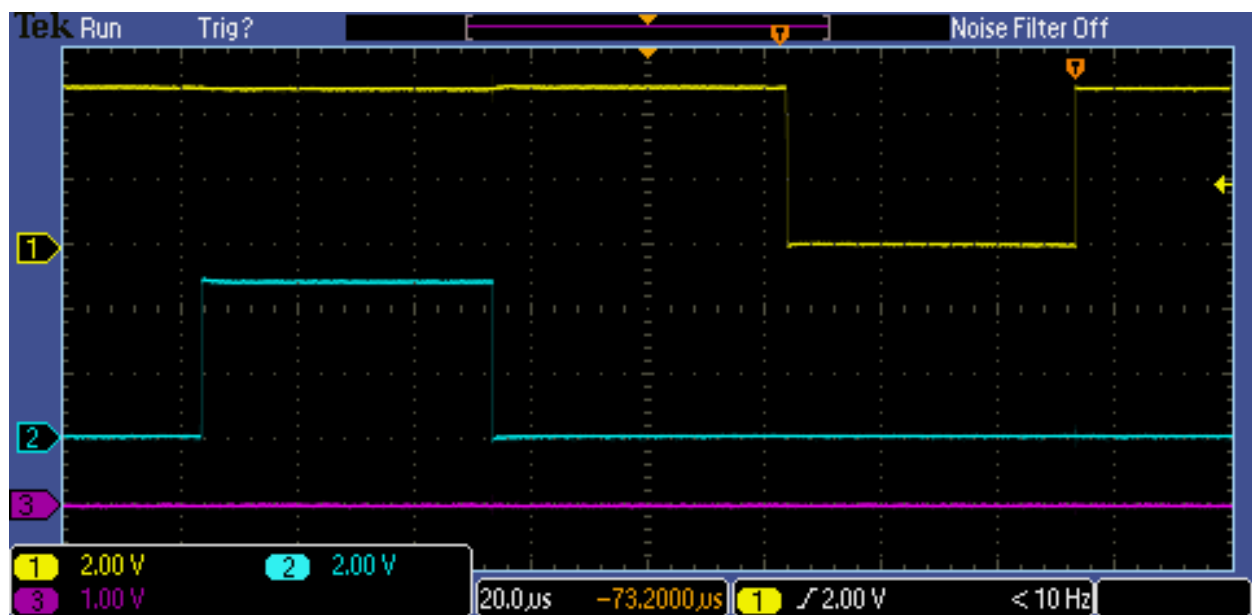


Figure 5: *Encoder Link Sequence* with a prior X1 = Q1 = 1

iC-HF EVAL HF1D

EVALUATION BOARD DESCRIPTION



Rev B2, Page 7/8

Encoder Link Sequence Execution for external iC-HF

To use the *Encoder Link Sequence* Generator for an external iC-HF device and not with the on board present iC-HF You need to remove or deactivate the iC-HF on board.

To deactivate the on board iC-HF use the following jumper configuration:

Jumper	Pin 1	Pin 2	Pin 3	Default Setting
JP2	ECM	VDDS	n.a.	1-2 open
JP3	OEN	VDDS	n.a.	1-2 open

The on-chip pull-down resistors will deactivate the output and disable the *Encoder Link* sensitivity of the on-board iC-HF.

Reverse polarity protection test setup

The *Encoder Link Sequence* Generator is on board and can be deactivated and protected for a reverse polarity protection test:

- Do connect the VDD pin with GND and provide the supply at VDD_HF.
- A reverse polarity supply may only be provided at the iC-HF related pins.
- A reverse polarity supply may not be provided at the iC-HF related pin VDD.
- A reverse polarity supply may not be provided at the *Encoder Link Sequence* Generator related pins:
 - EL
 - PDOWN

BISS/SSI INTERFACE LINE TRANSCEIVER

The HF1D is only designed to handle 5V RS422 signals on the serial BiSS/SSI interface.

Operating HF1D at full RS422 operational voltage levels will cause permanent damage to the device. In order to utilize the full RS422 operational voltage range the TVS Diodes D2-D5 need to be removed (no additional ESD protection) or changed to RS422 compatible types.

For more details please check the iC-HF datasheet http://www.ichaus.de/HF_datasheet_en , chapter RS-422 RECEIVER CONFIGURATION.

For sole 5V RS422 operation the RS422 receiver input resistor networks as described in the iC-HF datasheet are not present in this HF1D design.

RELATED DOCUMENTS

- iC-HF description and documentation → <http://www.ichaus.com/HF>

DESIGN REVIEW

iC-HF EVAL HF1D Redesign Z		
No.	Function, Parameter/Code	Description and Application Notes
1	PCB color	PCB color changed to blue
2	JP6	Jumper 6 added
3	JP7	Jumper 7 added
4	JP8	Jumper 8 added

Table 1: Notes on HF1D redesign Z functions regarding: blue PCB, JP6, JP7, JP8.

iC-HF EVAL HF1D

EVALUATION BOARD DESCRIPTION



Rev B2, Page 8/8

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2014-03-21		First Release	all

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2016-09-23		HF1D Redesign Z updated	
		BOARD HF1D AND TERMINAL DESCRIPTION	Figure 1: component side updated	1
		CIRCUIT DESCRIPTION	Figure 2:Circuit diagram updated	2
		ASSEMBLY PART LIST	JP6, JP7, JP8 added	3
		JUMPER DESCRIPTION	JP6, JP7, JP8 added	4
		ENCODER LINK SEQUENCE GENERATOR	Sequence details added	6
		DESIGN REVIEW	Chapter added	7

Rel.	Rel. Date*	Chapter	Modification	Page
B2	2018-10-09	CIRCUIT DESCRIPTION	5V RS422 design info added	2
		BISS/SSI INTERFACE LINE TRANSCEIVER	Chapter added	7

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* Release Date format: YYYY-MM-DD