iC-MN 25-BIT NONIUS ENCODER
WITH 3-CH. SAMPLING 13-BIT Sin/D INTERPOLATION

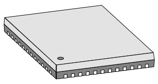
FEATURES

- 3 chan. simultaneous sampling 13 bit sine-to-digital conversion
- Differential and single-ended PGA inputs to 200 kHz
- Input adaptation to current or voltage signals
- Adjustable signal conditioning for offset, amplitude and phase
- Input signal stabilization by LED or MR bridge supply tracking (via controlled 50 mA and 2 x 10 mA highside sources)
- 2 or 3 track nonius calculation of up to 25 bit singleturn position
- Data update within 7 µs supported by flash period counting
- Serial 2-wire interface to multiturn sensors (BiSS, SSI, 2-bit)
- Fast, serial I/O interface with fail-safe RS422 transceiver (SSI to 4 MHz, BiSS C to 10 MHz)
- Differential 1 Vpp sin/cos outputs to 100 Ω, short-circuit-proof
- Position preset function, selectable up/down code direction
- Signal and system monitoring with configurable error/warning messaging and diagnosis memory
- Device setup via I/O interface (BiSS) or serial EEPROM
- Reverse-polarity-proof and tolerant against faulty output wiring
- Power-good switch protecting the peripheral circuitry
- Single 5 V supply, operation from -40 to +95 (+110) °C

APPLICATIONS

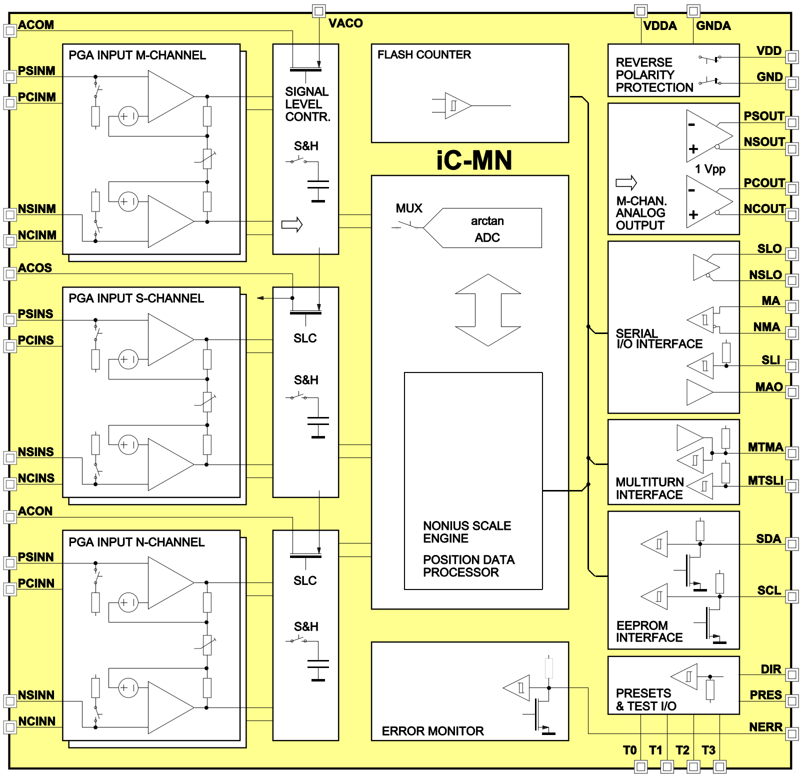
- Multi-channel sine-to-digital converter
- Optical and magnetic position sensors
- Singleturn and multiturn absolute encoders
- Linear scales for absolute position
- Resolver systems

PACKAGES



QFN48 7x7

BLOCK DIAGRAM



DESCRIPTION

Encoder device iC-MN is a 3-channel, simultaneous sampling sine-to-digital converter which interpolates sine/cosine sensor signals using a high precision SAR converter with a selectable resolution of up to 13 bits. Each input has a separate sample-and-hold stage which halts the track signal for the subsequent sequential digitization. Various 2- and 3-track Vernier scale computations (after Nonius) can be configured for the calculation of high resolution angle positions; these computations permit angle resolutions of up to 25 bits.

The absolute angle position is output via the serial Interface with clock rates of up to 4 Mbit/s (SSI compatible; up to 10 Mbit/s with BiSS C protocol). The RS422 transceiver required to this end is integrated on the chip and has both a differential clock input and a differential line driver for data output.

Programmable instrumentation amplifiers with a selectable gain and offset and phase correction can be adjusted separately for each channel; these allow differential or single-ended input signals. At the same time the inputs can either be set to high impedance for voltage signals from magneto resistor sensor bridges, for example, or to low impedance for adaptation and use with photosensors which provide current signals, for instance. This enables the device to be directly connected up to a number of different optical and magnetic sensors.

For the purpose of input signal stabilization the conditioned signals are fed into signal level controllers featuring current source outputs of up to 50 mA (master channel) and of up to 10 mA (for the nonius and segment channels each). These ACOx source pins either power the LEDs of an optical encoder or the magneto resistor bridges of a magnetic encoder. If the control thresholds are reached this event can be released for alarm messaging using the serial interface or the NERR output.

Both major chip functions and sensor errors are also monitored and can be enabled for alarm indication. In this manner typical sensor errors, such as signal loss due to wire breakage, short circuiting, dirt or aging, for example, can be signaled by alarms.

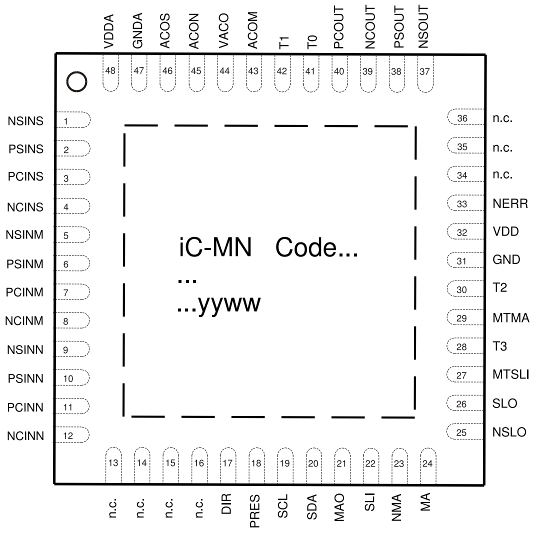
The device features further digital encoder functions covering the correction of phase errors between the tracks, for example, or the zeroing or presetting of a specific position offset for data output. Using the SSI master also integrated on the chip position data from multiturn sensors, provided by a second iC-MN, for example, can be read in and synchronized.

iC-MN is protected against a reversed power supply voltage; the integrated supply switch for loads of up to 20 mA extends this protection to cover the overall system. The device is configured via an external EEPROM.

CONTENTS

PACKAGES

PIN CONFIGURATION QFN48



PIN FUNCTIONS

No.	Name	Function
1	NSINS	Signal Input Sine - (Segment)
2	PSINS	Signal Input Sine + (Segment)
3	PCINS	Signal Input Cosine + (Segment)
4	NCINS	Signal Input Cosine - (Segment)
5	NSINM	Signal Input Sine - (Master)
6	PSINM	Signal Input Sine + (Master)
7	PCINM	Signal Input Cosine+ (Master)
8	NCINM	Signal Input Cosine - (Master)
9	NSINN	Signal Input Sine - (Nonius)
10	PSINN	Signal Input Sine + (Nonius)
11	PCINN	Signal Input Cosine + (Nonius)
12	NCINN	Signal Input Cosine - (Nonius)
13	n.c.	
14	n.c.	
15	n.c.	
16	n.c.	
17	DIR	Sense of Rotation Preselection Input, Calibration Signal IPB
18	PRES	Preset Input
19	SCL	EEPROM Interface, clock line
20	SDA	EEPROM Interface, data line
21	MAO	I/O Interface, clock output
22	SLI	I/O Interface, data input
23	NMA*	I/O Interface, clock input -
24	MA*	I/O Interface, clock input +
25	NSLO*	I/O Interface, data output -
26	SLO*	I/O Interface, data output +
27	MTSLI	Multiturn Interface, data input
28	T3	External Trigger Input, Test Signal Input
29	MTMA	Multiturn Interface, clock output
30	T2	Test Signal Input
31	GND*	Ground
32	VDD*	+4.5 to 5.5 V Supply Voltage
33	NERR*	Error Message Output, System Error Message Input
34	n.c.	
35	n.c.	
36	n.c.	
37	NSOUT*	Analog Output Sine - (Master)
38	PSOUT*	Analog Output Sine + (Master)
39	NCOUT*	Analog Output Cosine - (Master)
40	PCOUT*	Analog Output Cosine + (Master)
41	T0	Test Signal Output
42	T1	Test Signal Output
43	ACOM*	Signal Level Controller Outp. (Master)
44	VACO*	+4.5 to 5.5 V Signal Level Controller Supply
45	ACON*	Signal Level Controller Output
46	ACOS*	Signal Level Controller Output, VREFin Ref. Voltage Input/Output
47	GNDA	Sub-System Ground Output
48	VDDA	Sub-System Positive Supply Output

* :	Pin is immune against faulty output or supply connection.
n.c. :	Pin is not connected.

Wiring unused input pins can be recommended, especially for pins SLI, DIR, PRES and T2 (to GNDA). For calibrating the internal bias current source a pull-down resistor of 5 kΩ ±1 % connected from pin DIR to GNDA is useful (see Figure 10).

To improve heat dissipation the *thermal pad* of the QFN package (bottom side) should be joined to an extended copper area which must have GNDA potential.

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD, GND, NSLO, SLO, NERR, PSOUT, NSOUT, PCOUT, NCOUT, VACO	referenced to GND	-6	6	V
G002	V()	Voltage at MA, NMA	referenced to GND	-9	14	V
G003	V()	Pin-to-Pin Voltage vs. VDD, GND, NSLO, SLO, NERR, PSOUT, NSOUT, PCOUT, NCOUT, VACO			6	V
G004	V()	Voltage at NSINS, PSINS, PCINS, NCINS, NSINM, PSINM, PCINM, NCINM, NSINN, PSINN, PCINN, NCINN, DIR, PRES, SCL, SDA, MAO, SLI, MTSLI, T2, MTMA, T3, T0, T1, ACOM, ACON, ACOS, GNDA, VDDA	referenced to AGND, V() < VDD + 0.3 V	-0.3	6	V
G005	I(VDD)	Current in VDD		-100	400	mA
G006	I()	Current in VDDA, GNDA, PSOUT, NSOUT, PCOUT, NCOUT		-50	50	mA
G007	I()	Current in PSINM, NSINM, PCINM, NCINM, PSINS, NSINS, PCINS, NCINS, PSINN, NSINN, PCINN, NCINN, DIR, PRES, SCL, SDA, MAO, SLI, T3, T2, NERR, T0, T1		-20	20	mA
G008	I()	Current in SLO, NSLO, VACO		-120	120	mA
G009	I()	Current in MA, NMA		-0.6	1	mA
G010	I(ACOM)	Current in ACOM		-100	20	mA
G011	I()	Current in ACOS, ACON		-50	20	mA
G012	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G013	Tj	Junction Temperature		-40	150	°C
G014	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating conditions: VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	package QFN48	-40		110	°C
T02	Rthja	Thermal Resistance Chip to Ambient; QFN48	QFN48 surface mounted to PCB according to JEDEC 51		30		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...125 °C,
IBP calibrated to 200 µA, reference point GNDA (GND for digital I/O pins), unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD, VACO	Permissible Supply Voltage		4.5		5.5	V
002	I(VDD)	Supply Current in VDD	Tj = 27 °C, no load		45	60	mA
003	I(VDDA)	Permissible Load Current at VDDA		-20		0	mA
004	Vc()hi	Clamp Voltage hi (all pins with the exception of MA, NMA)	Vc()hi = V() − VDD, I() = 1 mA	0.4		1.5	V
005	Vc()hi	Clamp Voltage hi MA, NMA	Vc()hi = V() − VDD, I() = 10 mA	12.5		16	V
006	Vc()lo	Clamp Voltage lo (all pins with the exception of VDDA, MA, NMA)	I() = -1 mA	-1.5		-0.3	V
007	Vc()lo	Clamp Voltage lo at VDDA	I() = -1 mA	-1.5		-0.2	V
008	Vc()lo	Clamp Voltage lo at MA, NMA	I() = -10 mA	-17		-10	V
Signal Conditioning and Inputs: PSINx, NSINx, PCINx, NCINx (x = M, S, N)							
101	Vin()sig	Permissible V-Mode Input Voltage	UIN = 1, TUIN = 0 UIN = 1, TUIN = 1, DCPOS = 1	0.75 -0.1		VDDA − 1.5 VDDA + 0.1	V V
102	Iin()	V-Mode Input Current	UIN = 1, TUIN = 0	-100		100	nA
103	Rin()	V-Mode Input Resistance	vs. VREFin, Tj = 27 °C, UIN = 1, TUIN = 1	16.4	20	23.6	kΩ
104	Iin()sig	Permissible I-Mode Input Current	UIN = 0; DCPOS = 0 DCPOS = 1	 -10 10		 -300 300	 µA µA
105	SCR()	Permissible Signal Contrast Ratio	ratio of Iin()pk vs. Iin()dc	0.125		1	
106	Rin()	I-Mode Input Resistance	Tj = 27 °C, vs. VREFin; UIN = 0, RIN = 00 UIN = 0, RIN = 01 UIN = 0, RIN = 10 UIN = 0, RIN = 11	 1.1 1.6 2.2 3.2	 1.6 2.3 3.2 4.6	 2.1 3.0 4.2 6.0	 kΩ kΩ kΩ kΩ
107	TCRin	Temperature Coefficient Rin			0.15		%/K
108	VREFin	Input Reference Voltage	DCPOS = 1 DCPOS = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
109	Vin()os	Input Offset Voltage	referred to side of input			150	µV
110	Vin()diff	Recommended Differential Input Voltage	Vin()diff = V(PSINx) − V(NSINx), Vin()diff = V(PCINx) − V(NCINx); TUIN = 0 TUIN = 1	 20 80		 1000 4000	 mVpp mVpp
111	Vcore()	Recommended Internal Signal Level	G * Vin()diff		6		Vpp
112	GF, GC	Selectable Gain Factors	TUIN = 0 TUIN = 1	6 1.5		300 75	
113	ΔGFdiff	Differential Gain Accuracy (Master)	referenced to fine gain range	-1		1	LSB
114	ΔGFdiff	Differential Gain Accuracy (Segment, Nonius)	referenced to fine gain range	-2		2	LSB
115	ΔGFSabs	Absolute Gain Accuracy Sine (Master)	referenced to fine gain range, guaranteed monotony	-20		20	LSB
116	ΔGFCabs	Absolute Gain Accuracy Cosine (Master)	referenced to fine gain range, guaranteed monotony	-1		1	LSB
117	ΔGFSabs	Absolute Gain Accuracy Sine (Segment, Nonius)	referenced to fine gain range, guaranteed monotony	-20		20	LSB
118	ΔGFCabs	Absolute Gain Accuracy Cosine (Segment, Nonius)	referenced to fine gain range, guaranteed monotony	-1		1	LSB
119	ΔGCabs	Gain Accuracy	referenced to coarse gain range	-8		8	%

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...125 °C,
IBP calibrated to 200 µA, reference point GNDA (GND for digital I/O pins), unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
120	VOScal	Offset Calibration Range	measured at output, source V(ACOx) = 3 V, REFVOS = 00; ORS_x/ORC_x = 00 ORS_x/ORC_x = 01 ORS_x/ORC_x = 10 ORS_x/ORC_x = 11		±450 ±900 ±2700 ±5400		mV mV mV mV
121	VOScal2	Offset Calibration Range	measured at output, source V05, REFVOS = 01; ORS_x/ORC_x = 00 ORS_x/ORC_x = 01 ORS_x/ORC_x = 10 ORS_x/ORC_x = 11		±1500 ±3000 ±9000 ±18000		mV mV mV mV
122	VOScal3	Offset Calibration Range	measured at output, source V025, REFVOS = 10; ORS_x/ORC_x = 00 ORS_x/ORC_x = 01 ORS_x/ORC_x = 10 ORS_x/ORC_x = 11		±750 ±1500 ±4500 ±9000		mV mV mV mV
123	VOScal4	Offset Calibration Range	measured at output, source VDC = 125 mV, REFVOS = 11; ORS_x/ORC_x = 00 ORS_x/ORC_x = 01 ORS_x/ORC_x = 10 ORS_x/ORC_x = 11		±375 ±750 ±2250 ±4500		mV mV mV mV
124	ΔVOSdiff	Differential Linearity Error of Offset Correction Master		-0.5		0.5	LSB
125	ΔVOSdiff	Differential Linearity Error of Offset Correction Segment, Nonius		-2		2	LSB
126	ΔVOSint	Integral Linearity Error of Offset Correction Master		-100		100	LSB
127	ΔVOSint	Integral Linearity Error of Offset Correction Segment, Nonius		-100		100	LSB
128	PHIcal	Phase Correction Range	sine vs. cosine signal		±10.4		°
129	ΔPHIdiff	Differential Linearity Error of Phase Correction Master		-0.25		0.25	LSB
130	ΔPHIdiff	Differential Linearity Error of Phase Correction Segment, Nonius		-2		2	LSB
131	ΔPHIint	Integral Linearity Error of Phase Correction Master		-20		20	LSB
132	ΔPHIint	Integral Linearity Error of Phase Correction Segment, Nonius		-20		20	LSB
133	fin()max	Permissible Input Frequency	angle accuracy better 8 bit	200			kHz
134	fhc()	Input Amplifier Cut-off Frequency (-3 dB)		250			kHz

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...125 °C,
IBP calibrated to 200 µA, reference point GNDA (GND for digital I/O pins), unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Signal Level Controller: ACOM							
401	Vs()hi	Saturation Voltage hi	Vs()hi = V(VACO) - V();				
			ACOR_M(6:5) = 00, I() = -5 mA			1	V
			ACOR_M(6:5) = 01, I() = -10 mA			1	V
			ACOR_M(6:5) = 10, I() = -25 mA			1	V
			ACOR_M(6:5) = 11, I() = -50 mA			1	V
402	Isc()hi	Short-circuit Current hi	V() = 0...V(VACO) – 1 V;				
			ACOR_M(6:5) = 00	-9.5	-7	-5	mA
			ACOR_M(6:5) = 01	-19	-14.5	-10	mA
			ACOR_M(6:5) = 10	-46	-36	-25	mA
			ACOR_M(6:5) = 11	-85	-73	-50	mA
403	Ilk()	Residual Current With Reversed Supply				50	µA
404	Tctrl	Control Time Constant	quadratic or sum regulation		1.6		ms
405	Vscq()avg	Controlled Average S/C Signal Amplitude: SQRT of [V(PSOUT)-V(NSOUT)]^2 + [V(PCOUT)-V(NCOUT)]^2	quadratic regulation: ACOT_M(8:7) = 00, Op.mode ANA_M	2.7	3	3.3	V
406	Vt()min	Signal Monitoring AM_Min	referred to Vscq()		40		%
407	Vt()max	Signal Monitoring AM_Max	referred to Vscq()		135		%
408	It()min	Control Monitoring ACM_Min	referenced to range ACOR_M()		3		%Isc
409	It()max	Control Monitoring ACM_Max	referenced to range ACOR_M()		90		%Isc
Signal Level Controller: ACOS, ACON							
501	Vs()hi	Saturation Voltage hi	Vs()hi = V(VACO) – V();				
			ACOR_x(5) = 0, I() = -5 mA			1	V
			ACOR_x(5) = 1, I() = -10 mA			1	V
502	Isc()hi	Short-circuit Current hi	V() = 0...V(VACO) – 1 V;				
			ACOR_x(5) = 0	-9.5	-7	-5	mA
			ACOR_x(5) = 1	-19	-14.5	-10	mA
503	Ilk()	Residual Current with Reverse Polarity				50	µA
504	Tctrl	Control Time Constant	control to sine square or sum		1.6		ms
505	Vscq()avg	Controlled Average S/C Signal Amplitude: SQRT of [V(PSOUT)-V(NSOUT)]^2 + [V(PCOUT)-V(NCOUT)]^2	quadratic regulation: ACOT_x(7:6) = 00, operating mode ANA_x	2.7	3	3.3	V
506	Vt()min	Signal Monitoring AN_Min, AS_Min	referred to Vscq()		40		%
507	Vt()max	Signal Monitoring AN_Max, AS_Max	referred to Vscq()		135		%
508	It()min	Control Monitoring ACN_Min, ACS_Min	referenced to range ACOR_x()		3		%Isc
509	It()max	Control Monitoring ACN_Max, ACS_Max	referenced to range ACOR_x()		90		%Isc
510	Vin(ACOS)	Permissible Ref. Input Voltage at ACOS	CVREF = 11	0.75		VDDA – 2	V

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...125 °C,
IBP calibrated to 200 µA, reference point GNDA (GND for digital I/O pins), unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Sample-&-Hold Stage, Signal Filter and Sine-To-Digital Conversion							
601	fc1()	Cut-off Frequency of M/S/N Channel Signal Filter (-3 dB lowpass filter)	ENF(1) = 1; fin (master channel) < 20 Hz fin (master channel) > 1300 Hz		 4 300		 kHz kHz
602	amax	Permissible Angle Acceleration for 3(2) track nonius calculation	ENF(1) = 1		1000		Mrad/s^2
603	AAabs	Absolute Angular Accuracy	Used bit length UBL_x = 0x0D: 13 bit		±2		LSB
604	AAR	Repeatability			±1		LSB
605	tcnv	Conversion Time (1 Channel)	Used bit length UBL_x: 0x0D: 13 bit 0x0C: 12 bit 0x0B: 11 bit 0x0A: 10 bit 0x09: 9 bit 0x08: 8 bit 0x07: 7 bit 0x06: 6 bit 0x05: 5 bit 0x04: 4 bit		 4.25 3.88 3.5 3.13 2.75 2.5 2.25 2.0 1.75 1.5		 µs µs µs µs µs µs µs µs µs µs
606	trec()	Recovery Time Sampling-to-Sampling	termination of calculation and synchronization (Nonius or MT modes) to follow-up S&H trigger			1.25	µs
Analog Line Driver Outputs: PSOUT, NSOUT, PCOUT, NCOUT							
701	Vout()	Output Amplitude	RLdiff = 100 Ω, VDD = 4.5 V, DC level = VDD/2			300	mV
702	fc2()	Cut-off Frequency of Line Driver Signal Filter (-3 dB lowpass filter)	ENF(0) = 1; fin (master channel) < 20 Hz fin (master channel) > 1300 Hz		 8 600		 kHz kHz
703	fc3()	Cut-off Frequency of Line Driver (-3 dB)	CL = 500 pF, Vpp = 0.5 V, ENF0 = 1	500			kHz
704	Voffs()	Offset Voltage		-8		8	mV
705	Isc()hi	Short-circuit Current hi	V() = GND	-40	-20	-15	mA
706	Isc()lo	Short-circuit Current lo	V() = VDD	15	20	40	mA
707	SR()	Slew Rate	RLdiff = 100 Ω, CL = 25 pF		5		V/µs
708	Ilk()	Residual Current with Reverse Polarity		-50		50	µA
709	Vout()err	Output Signal with Temperature Error	VTs > VTth		50		%VDD
710	Rout()	Output Impedance	Op.Mode ANA_M, ANA_N, ANA_S		5		kΩ
711	fout()cal	Permissible Output Frequency During Calibration	Op.Mode ANA_M, ANA_N, ANA_S; CL = 200 pF			2	kHz
Bias Current Source and Reference Voltages							
801	IBP	Bias Current Source	IBP calibrated to 200 µA	92.5	100	107.5	%
802	VPAH	Reference Voltage VPAH	referenced to GNDA	48	50	52	%VDD
803	V05	Reference Voltage V05	referenced to GNDA	460	512	570	mV
804	V025	Reference Voltage V025	referenced to GNDA		50		%V05

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...125 °C,
IBP calibrated to 200 µA, reference point GNDA (GND for digital I/O pins), unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power-Down-Reset							
901	VDDon	Turn-on Threshold VDD (power on release)	increasing voltage VDD	3.6	3.9	4.3	V
902	VDDoff	Turn-off Threshold VDD (power down reset)	decreasing voltage VDD	3.1	3.4	3.8	V
903	VDDhys	Hysteresis	VDDhys = VDDon – VDDoff	400			mV
904	tready()cfg	Operation Start-Up Time	includes tbusy()cfg; MODE_MT = 00 MODE_MT ≠ 00		21 29		ms ms
Clock Oscillator							
A01	fosc	Clock Frequency			8		MHz
Supply Switch and Reverse Polarity Protection: VDDA, GNDA							
B01	Vs()	Switch Drop-Off Voltage vs. VDD (unloaded)	V() = V(VDD) – V(VDDA), I(VDDA) = 0		115		mV
B02	Rs()	VDDA Switch On-Resistance	VDD vs. VDDA, load current to 20 mA	5	10	20	Ω
B03	Vs()	Switch Drop-Off Voltage vs. GNDA (unloaded)	V() = V(GNDA) – V(GND), I(GNDA) = 0		105		mV
B04	Rs()	GNDA Switch On-Resistance	ground current to 20 mA	1	3.8	7	Ω
Temperature Monitoring							
C01	VTSw	Sensor Voltage for Warning Temperature	VTSw() = VDDA – V(T1), Tj = 27 °C, operating mode TWIB	610	640	670	mV
C02	VTSe	Sensor Voltage for Shutdown Temperature	VTSe() = VDDA – V(T1), Tj = 27 °C, operating mode TEIB	635	665	695	mV
C03	TCs	Sensor Voltage Temperature Coefficient			-1.95		mV/K
C04	VTth	Activation Threshold Temperature Warning	VTth() = VDDA – V(T0), Tj = 27 °C; CFGTA(4:0) = 0x00 CFGTA(4:0) = 0x0F CFGTA(4:0) = 0x1F	225 400 585	285 498 725	355 615 895	mV mV mV
C05	TCth	Activation Threshold Temperature Coefficient			1.32		‰/K
C06	$Thys_W$	Warning Temperature Hysteresis		4	15	19	°C
C07	ΔT	Relative Shutdown Temperature	ΔT = Te – Tw	5	15	20	°C
C08	$Thys_e$	Shutdown Temperature Hysteresis		9	30	39	°C
EEPROM Interface: SCL, SDA							
D01	Vs()lo	Saturation Voltage lo	I() = 4 mA			450	mV
D02	Isc()lo	Short-circuit Current lo		4		60	mA
D03	Vt()hi	Input Threshold Voltage hi				2	V
D04	Vt(lo)	Input Threshold Voltage lo		800			mV
D05	Vt()hys	Input Hysteresis	Vt(hys) = Vt()hi – Vt()lo	150	250		mV
D06	Ipu()	Input Pull-up Current	V() = 0...VDD – 1 V	-750	-300	-60	µA
D07	Vpu()	Input Pull-up Voltage	Vpu() = VDD – V(), I() = -5 µA			400	mV
D08	fclk(SCL)	Clock Frequency		45	62.5	80	kHz
D09	tbusy()cfg	Duration Of Startup Configuration	error free EEPROM access		13	15	ms

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...125 °C,
IBP calibrated to 200 µA, reference point GNDA (GND for digital I/O pins), unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I/O Interface: RS442 Line Driver Outputs SLO, NSLO							
E01	Vs()hi	Saturation Voltage hi	Vs() = VDD − V();				
			DSC(1:0) = 00, I() = -1.2 mA			200	mV
			DSC(1:0) = 01, I() = -4 mA			200	mV
			DSC(1:0) = 10, I() = -20 mA			400	mV
			DSC(1:0) = 11, I() = -50 mA			900	mV
E02	Vs()lo	Saturation Voltage lo	DSC(1:0) = 00, I() = 1.2 mA			200	mV
			DSC(1:0) = 01, I() = 4 mA			200	mV
			DSC(1:0) = 10, I() = 20 mA			400	mV
			DSC(1:0) = 11, I() = 50 mA			900	mV
E03	Isc()hi	Short-circuit Current hi	V() = 0 V;				
			DSC(1:0) = 00	-3		-1.2	mA
			DSC(1:0) = 01	-10		-4	mA
			DSC(1:0) = 10	-45		-20	mA
			DSC(1:0) = 11	-120		-50	mA
E04	Isc()lo	Short-circuit Current lo	V() = VDD				
			DSC(1:0) = 00	1.2		3	mA
			DSC(1:0) = 01	4		10	mA
			DSC(1:0) = 10	20		45	mA
			DSC(1:0) = 11	50		120	mA
E05	Ilk()tri	Tristate Leakage Current	DTRI(1:0) = 11	-10		10	µA
E06	tr()	Rise Time hi	RL = 100 Ω to GND, DSC(1:0) = 11;				
			DSR(1:0) = 00	10		30	ns
			DSR(1:0) = 01	22		40	ns
			DSR(1:0) = 10	60		140	ns
			DSR(1:0) = 11	250		350	ns
E07	tf()	Fall Time lo	RL = 100 Ω to VDD, DSC(1:0) = 11;				
			DSR(1:0) = 00	5		15	ns
			DSR(1:0) = 01	22		40	ns
			DSR(1:0) = 10	60		140	ns
			DSR(1:0) = 11	250		350	ns
E08	Ilk()	Residual Current with Reverse Polarity		-100		100	µA
I/O Interface: RS442 Line Receiver MA, NMA							
F01	Vin()	Permissible Input Voltage		-7		12	V
F02	Rin()	Input Resistance	MA vs. GND, NMA vs. GND	15	20	25	kΩ
F03	Vhys()	Differential Input Hysteresis	Vhys() = (V(MA) - V(NMA)) / 2	50		200	mV
F04	Vt()hi	Input Threshold Voltage hi at MA	pin NMA open			2	V
F05	Vt()lo	Input Threshold Voltage lo at MA	pin NMA open	800			mV
F06	fclk()	Permissible Clock Frequency: SSI protocol	MODE_ST = 0x05 to 0x0B, 0x0D to 0x0F			4	MHz
F07	fclk()	Permissible Clock Frequency: BiSS protocol	NBISS = 0			10	MHz
F08	tp(MA-SLO)	Propagation Delay: MA edge vs. SLO output	RL(SLO/NSLO) = 120 Ω	10		50	ns
F09	tbusy_s	Processing Time Singlecycle Data (delay of start bit)	Nonius modes:				
			MODE_ST = 0x00 to 0x02		tcnv *1		µs
			MODE_ST = 0x03 to 0x04, 2 track		tcnv *2		µs
			MODE_ST = 0x03 to 0x04, 3 track		tcnv *3		µs
			MODE_ST = 0x05 to 0x0B		0		µs
			MT modes:				
			MODE_ST = 0x0C, 3 track		tcnv *3		µs
			MODE_ST = 0x0D to 0x0F		0		µs
F10	tbusy_r	Processing Time Register Access (delay of start bit)	with read access to EEPROM			2	ms
F11	tidle	Interface Blocking Time	powering up without EEPROM			2	ms

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...125 °C,
IBP calibrated to 200 µA, reference point GNDA (GND for digital I/O pins), unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I/O Interface: Clock Line Output MAO							
G01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(), I() = -4 mA			450	mV
G02	Vs()lo	Saturation Voltage lo	I() = 4 mA			450	mV
G03	Isc()hi	Short-circuit Current hi		-85		-30	mA
G04	Isc()lo	Short-circuit Current lo		20		65	mA
Test Signal Inputs: T2, T3							
H01	Vt()hi	Input Threshold Voltage hi				2	V
H02	Vt()lo	Input Threshold Voltage lo		800			mV
H03	Vt()hys	Input Hysteresis		150	250		mV
H04	Ipd()	Input-Pull-Down-Current at T2	V() = 1 V...VDD	4	30	75	µA
H05	Vpd()	Input-Pull-Down-Voltage at T2	I() = 5 µA			650	mV
H06	Ipu()	Input Pull-up Current at T3	V() = 0...VDD − 1 V	-65	30	-5	µA
H07	Vpu()	Input Pull-up Voltage at T3	Vpu() = VDD − V(), I() = -5 µA			650	mV
Test Signal Outputs: T0, T1							
I01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(), I() = -4 mA			500	mV
I02	Vs()lo	Saturation Voltage lo	I() = 4 mA			600	mV
I03	Isc()hi	Short-circuit Current hi		-60		-15	mA
I04	Isc()lo	Short-circuit Current lo		15		60	mA
I05	Voffs()	Analog Buffer Offset Voltage at T0	Vos() = V(T1) − V(T0), operating mode TBOS	-25		25	mV
I/O Interface: Input SLI							
J01	Vt()hi	Input Threshold Voltage hi				2	V
J02	Vt()lo	Input Threshold Voltage lo		0.8			V
J03	Vt()hys	Input Hysteresis		150	250		mV
J04	Ipd()	Input Pull-down Current	V() = 1 V...VDD	4	30	75	µA
J05	Vpd()	Input Pull-Down Voltage	I() = 5 µA			650	mV
Digital Inputs: DIR, PRES							
K01	Vt()hi	Input Threshold Voltage hi				2	V
K02	Vt()lo	Input Threshold Voltage lo		0.8			V
K03	Vt()hys	Input Hysteresis		150	250		mV
K04	Ipd()	Input Pull-down Current	V() = 1 V ... VDD	20.5	120	296	µA
K05	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); I() = 1.6 mA			295	mV
K06	Vs()lo	Saturation Voltage lo	during test function, I() = 1.6 mA			275	mV
K07	Vpd()	Input Pull-down Voltage	during test function, I() = 5 µA			600	mV

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...125 °C,
IBP calibrated to 200 µA, reference point GNDA (GND for digital I/O pins), unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Error Message Input/Output: NERR							
L01	Vs()lo	Saturation Voltage lo	I() = 4 mA			450	mV
L02	Isc()lo	Short-circuit Current lo		4		60	mA
L03	Vt()hi	Input Threshold Voltage hi				2	V
L04	Vt()lo	Input Threshold Voltage lo		0.8			V
L05	Vt()hys	Input Hysteresis	Vt(hys) = Vt()hi - Vt()lo	150	250		mV
L06	Ipu()	Input Pull-up Current	V() = 0... VDD - 1 V	-750	-300	-60	µA
L07	Vpu()	Input Pull-up Voltage	Vpu() = VDD - V(), I() = -5 µA			400	mV
L08	Ilk()	Residual Current with Reverse Polarity		-100		100	µA
Multiturn Interface: MTMA, MTSLI							
M01	Vt()hi	Input Threshold Voltage hi	MODE_MT = 11			2	V
M02	Vt()lo	Input Threshold Voltage lo	MODE_MT = 11	0.8			V
M03	Vt()hys	Input Hysteresis	MODE_MT = 11	150	250		mV
M04	Ipd()	Input Pull-down Current MTSLI	V() = 1 V ... VDD	4	30	75	µA
M05	Vpd()	Input Pull-down Voltage MTSLI	I() = 5 µA			650	mV
M06	Ipu()	Input Pull-up Current MTMA	V() = 0 V ... VDD - 1 V	-296	-120	-20.5	µA
M07	Vpu()	Input Pull-up Voltage MTMA	Vpu() = VDD - V(), I() = -5 µA			600	mV
M08	Vs()hi	Saturation Voltage hi at MTMA	Vs()hi = VDD - V(), I() = 4 mA			450	mV
M09	Vs()lo	Saturation Voltage lo at MTMA	I() = 4 mA			450	mV
M10	Isc()hi	Short-circuit Current hi at MTMA		-85		-30	mA
M11	Isc()lo	Short-circuit Current lo at MTMA		20		65	mA
M12	fclk()	SSI Clock Frequency at MTMA			0.125		MHz
M13	fclk()	BiSS Clock Frequency at MTMA	MODE_MT = 01		1		MHz
M14	t_{cycle}	Max. BiSS Read Cycle Duration	MODE_MT = 01			256	µs
M15	t_{cycle}	MT Data Update Interval	MODE_MT = 01 or 10, CHK_MT = 1		8		ms

OPERATING REQUIREMENTS: I/O Interface

Operating conditions: VDD = 5 V ±10 %, Ta = -40...95(110) °C,
IBP calibrated for fosc = 8 MHz, reference point GNDA (GND for digital I/O pins), unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI Protocol						
I001	T_{MAS}	Permissible Clock Period	t_{out} selected in accordance to Table 50	250	2x t_{out}	ns
I002	t_{MASh}	Clock Signal Hi Level Duration		25	t_{out}	ns
I003	t_{MASl}	Clock Signal Lo Level Duration		25	t_{out}	ns
I004	t_{cycle}	Permissible Cycle Time: Example for 19-bit ST data from 3-track nonius calculation	MODE_ST = 0x05...0x07, UBL_M = 13 bit, UBL_N + SBL_N = 7 bit, UBL_S + SBL_S = 7 bit	11.25		µs
BiSS C Protocol (NBISS = 0x0)						
I005	T_{MAS}	Permissible Clock Period	t_{out} selected in accordance to Table 58	100		ns
I006	t_{MASh}	Clock Signal Hi Level Duration		25	t_{out}	ns
I007	t_{MASl}	Clock Signal Lo Level Duration		25		ns
I008	t_{busy}	Minimum Data Output Delay	MODE_ST = 0x05...0x0B, 0x0D...0x0F, MA lo→hi until SLO lo→hi	2x T_{MAS}		µs
I009	t_{busy}	Maximum Data Output Delay: Example for 19-bit ST data from 3-track nonius calculation	MODE_ST = 0x00...0x02, fclk(MA) = 10 MHz, UBL_x and SBL_x see I004		5.3	µs
I010	t_{busy}	Maximum Data Output Delay: Example for 19-bit ST data from 3-track nonius calculation	MODE_ST = 0x03...0x04, fclk(MA) = 10 MHz, UBL_x and SBL_x see I004		10	µs
I011	t_{busy}	Maximum Data Output Delay: Example for 39-bit ST data from 3-track interpolation without synchronization	MODE_ST = 0x0C, fclk(MA) = 10 MHz, UBL_M 13 bit, UBL_N 13 bit, UBL_S 13 bit		14	µs
I012	t_{cycle}	Permissible Cycle Time: Example for 19-bit ST data from 3-track nonius calculation	MODE_ST = 0x05...0x07, UBL_x and SBL_x see I004	11.25		µs

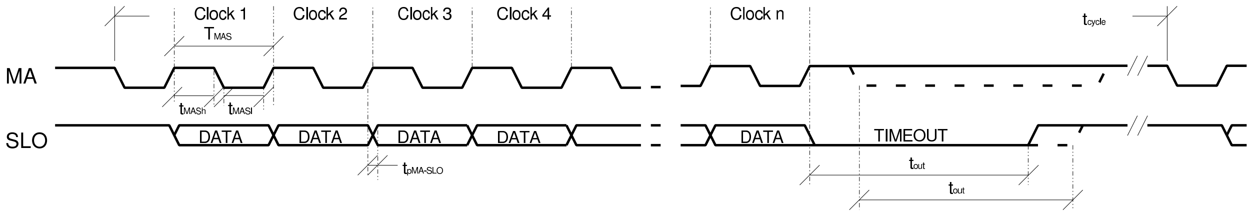


Figure 1: I/O Interface timing with SSI protocol

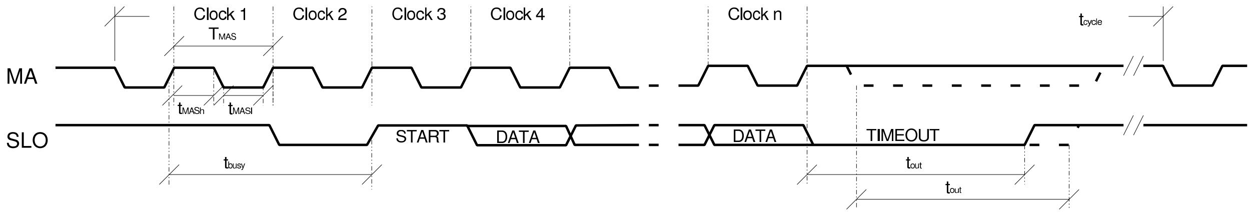


Figure 2: I/O Interface timing with BiSS C protocol

CONFIGURATION PARAMETERS

Analog Parameters (valid for all channels)
CFGIBP: Bias Trimming (P. 28)
CFGTA: Temperature Sensor Calib. (P. 28)
DCPOS: Input Current Polarity (P. 23)
ENF: Noise Filter Enable (P. 28)
CVREF: VREF Source Selection (P. 23)
REFVOS: Offset Reference Source (P. 24)
RIN: Input Resistance (P. 23)
TUIN: Input Voltage Divider (P. 23)
UIN: Signal Mode (P. 23)

Signal Conditioning
x = M, S, N (for master, segment, nonius channel)
ACOC_x: Signal Level Control: Current (P. 27)
ACOR_x: Signal Level Control: Range (P. 27)
ACOT_x: Signal Level Control: Op. Mode (P. 27)
GFC_x: Gain Factor Cosine (P. 24)
GR_x: Gain Range (P. 24)
GFS_x: Gain Factor Sine (P. 24)
MPS_x: Intermediate Voltage Sine (P. 25)
MPC_x: Intermediate Voltage Cosine (P. 25)
OFC_x: Offset Factor Cosine (P. 26)
ORC_x: Offset Range Cosine (P. 25)
OFS_x: Offset Factor Sine (P. 25)
ORS_x: Offset Range Sine (P. 25)
PH_x: S/C Phase Correction (P. 26)

Operating Modes
TRACMODE: Op. Mode Parameter (P. 21)
CALMODE: Op. Mode Parameter (P. 21)
BYP: Bypass Switch (P. 21)

Sine-To-Digital Conversion
MODE_ST: S/D Conversion Mode (P. 30)
UBL_M: Bit Length Master (P. 29)
UBL_N: Used Bit Length Nonius (P. 29)
SBL_N: Synch. Bit Length Nonius (P. 29)
UBL_S: Used Bit Length Segment (P. 29)
SBL_S: Synch. Bit Length Segment (P. 29)
FRQ_TH: Signal Frequency Monitoring (P. 32)
SPO_N: Offset Nonius Track (P. 35)
SPO_S: Offset Segment Track (P. 35)

I/O Interface
TOS: Timeout (P. 36)
DL_ST: ST Data Length (P. 36)
M2S: MT Data Output (P. 39)
ESSI: Error Bit (P. 37)
GRAY_SCD: Data Format (P. 37)
RSSI: Ring Operation (P. 37)
DIR: Inversion Of Code Direction (P. 37)

I/O Interface With Extended Functions
NBISS: Interface Protocol (P. 38)
TOS: Timeout (S. 38)
DL_ST: ST Data Length (P. 39)
M2S: MT Data Output (P. 39)
DIR: Inversion Of Code Direction (P. 39)
GRAY_SCD: Data Format (P. 39)
CID_SCD: CRC Start Value (P. 39)
NC_BISS: Communication Disable (S. 39)
ELC: Lifecounter (P. 40)

Driver Settings
DSC: Driver Short-Circuit Current (P. 41)
DTRI: Driver Output Mode (P. 41)
DSR: Driver Slew Rate (P. 41)

Command And Status Register
STATUS: Status Register (P. 43)
MN_CMD: Implemented Commands (P. 42)
AUTORES: Automatic Reset Function (S. 42)

Error And Warning Bit
CFGEW: Error And Warning Bit Config. (P. 44)
S2ERR: Visibility For Warning Bit (P. 45)
S2WRN: Visibility For Error Bit (P. 45)
E2EPR: Diagnosis Memory Enable (P. 43)

MT Interface
MODE_MT: MT Interface Operating Mode (P. 46)
DL_MT: MT Data Length (P. 46)
SBL_MT: MT Synch. Bit Length (P. 47)
LNT_MT: Leading/Trailing Gear Box Assembly (P. 47)
CHK_MT: Period Counter Verification (P. 47)
GRAY_MT: MT Interface Data Format (P. 47)

MT Interface with Extended Functions
MODE_MT: MT Interface Operating Mode (P. 46)
GET_MT: Direct BiSS Communication Enable for MT Sensor via I/O Interface (P. 49)
NCRC_MT: MT Interface CRC Verification (P. 49)
SWC_MT: MT Interface CRC Polynomial (P. 49)

Preset Function
OFFS_ST: Position Offset for ST Data Output (P. 50)
PRES_ST: Preset Value for ST Data Output (P. 50)
OFFS_MT: Position Offset for MT Data Output (P. 50)
PRES_MT: Preset Value for MT Data Output (P. 50)

EEPROM Interface
CFG_E2P: Config. Of External Memory (P. 52)
CRC_E2P: EEPROM Data Check Sum (P. 52)
PROT_E2P: Register Access Control (P. 53)

REGISTER MAP (EEPROM)

<table>
<tr><th colspan="9">OVERVIEW</th></tr>
<tr><th>Adr</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td colspan="9">Signal Conditioning Master Channel</td></tr>
<tr><td>0x00</td><td colspan="5">GFC_M</td><td colspan="3">GR_M</td></tr>
<tr><td>0x01</td><td colspan="8">GFS_M(7:0)</td></tr>
<tr><td>0x02</td><td colspan="5">MPS_M(4:0)</td><td colspan="3">GFS_M(10:8)</td></tr>
<tr><td>0x03</td><td colspan="3">MPC_M(2:0)</td><td colspan="5">MPS_M(9:5)</td></tr>
<tr><td>0x04</td><td>ORS_M(0)</td><td colspan="7">MPC_M(9:3)</td></tr>
<tr><td>0x05</td><td colspan="7">OFS_M(6:0)</td><td>ORS_M(1)</td></tr>
<tr><td>0x06</td><td colspan="2">OFC_M(1:0)</td><td colspan="2">ORC_M</td><td>OFS_M(10)*</td><td colspan="3">OFS_M(9:7)</td></tr>
<tr><td>0x07</td><td colspan="8">OFC_M(9:2)</td></tr>
<tr><td>0x08</td><td colspan="7">PH_M(6:0)</td><td>OFC_M(10)*</td></tr>
<tr><td>0x09</td><td></td><td></td><td></td><td></td><td></td><td>PH_M(9)*</td><td colspan="2">PH_M(8:7)</td></tr>
<tr><td colspan="9">Signal Conditioning Master Channel and Analog Parameters</td></tr>
<tr><td>0x0A</td><td>1</td><td>DCPOS</td><td colspan="2">REFVOS</td><td>TUIN</td><td colspan="2">RIN</td><td>UIN</td></tr>
<tr><td>0x0B</td><td></td><td></td><td></td><td colspan="2">CVREF</td><td>0</td><td>BYP</td><td>1</td></tr>
<tr><td>0x0C</td><td>ACOT_M(0)</td><td colspan="2">ACOR_M(1:0)</td><td colspan="5">ACOC_M(4:0)</td></tr>
<tr><td>0x0D</td><td colspan="3">CFGTA(2:0)</td><td colspan="4">CFGIBP(3:0)</td><td>ACOT_M(1)</td></tr>
<tr><td>0x0E</td><td></td><td></td><td colspan="2">ENF(1:0)</td><td></td><td></td><td colspan="2">CFGTA(4:3)</td></tr>
<tr><td>0x0F</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="9">*) MSB and signum respectively.</td></tr>
</table>

Table 5: Register layout

<table>
<tr><th colspan="9">OVERVIEW</th></tr>
<tr><th>Adr</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td colspan="9">Signal Conditioning Segment Channel</td></tr>
<tr><td>0x10</td><td colspan="5">GFC_S</td><td colspan="3">GR_S</td></tr>
<tr><td>0x11</td><td colspan="8">GFS_S(7:0)</td></tr>
<tr><td>0x12</td><td colspan="5">MPS_S(4:0)</td><td colspan="3">GFS_S(10:8)</td></tr>
<tr><td>0x13</td><td colspan="3">MPC_S(2:0)</td><td colspan="5">MPS_S(9:5)</td></tr>
<tr><td>0x14</td><td>ORS_S(0)</td><td colspan="7">MPC_S(9:3)</td></tr>
<tr><td>0x15</td><td colspan="7">OFS_S(6:0)</td><td>ORS_S(1)</td></tr>
<tr><td>0x16</td><td colspan="2">OFC_S(1:0)</td><td colspan="2">ORC_S</td><td>OFS_S(10)*</td><td colspan="3">OFS_S(9:7)</td></tr>
<tr><td>0x17</td><td colspan="8">OFC_S(9:2)</td></tr>
<tr><td>0x18</td><td colspan="7">PH_S(6:0)</td><td>OFC_S(10)*</td></tr>
<tr><td>0x19</td><td></td><td></td><td></td><td></td><td></td><td>PH_S(9)*</td><td colspan="2">PH_S(8:7)</td></tr>
<tr><td>0x1A</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0x1B</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0x1C</td><td>ACOT_S(0)</td><td></td><td>ACOR_S</td><td colspan="5">ACOC_S(4:0)</td></tr>
<tr><td>0x1D</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>ACOT_S(1)</td></tr>
<tr><td>0x1E</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0x1F</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="9">Signal Conditioning Nonius Channel</td></tr>
<tr><td>0x20</td><td colspan="5">GFC_N</td><td colspan="3">GR_N</td></tr>
<tr><td>0x21</td><td colspan="8">GFS_N(7:0)</td></tr>
<tr><td>0x22</td><td colspan="5">MPS_N(4:0)</td><td colspan="3">GFS_N(10:8)</td></tr>
<tr><td>0x23</td><td colspan="3">MPC_N(2:0)</td><td colspan="5">MPS_N(9:5)</td></tr>
<tr><td>0x24</td><td>OSR_N(0)</td><td colspan="7">MPC_N(9:3)</td></tr>
<tr><td>0x25</td><td colspan="7">OFS_N(6:0)</td><td>OSR_N(1)</td></tr>
<tr><td>0x26</td><td colspan="2">OFC_N(1:0)</td><td colspan="2">ORC_N</td><td>OFS_N(10)*</td><td colspan="3">OFS_N(9:7)</td></tr>
<tr><td>0x27</td><td colspan="8">OFC_N(9:2)</td></tr>
<tr><td>0x28</td><td colspan="7">PH_N(6:0)</td><td>OFC_N(10)*</td></tr>
<tr><td>0x29</td><td></td><td></td><td></td><td></td><td></td><td>PH_N(9)*</td><td colspan="2">PH_N(8:7)</td></tr>
<tr><td>0x2A</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0x2B</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0x2C</td><td>ACOT_N(0)</td><td></td><td>ACOR_N</td><td colspan="5">ACOC_N(4:0)</td></tr>
<tr><td>0x2D</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>ACOT_N(1)</td></tr>
<tr><td>0x2E</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0x2F</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="9">*) MSB and signum respectively.</td></tr>
</table>

Table 6: Register layout

OVERVIEW

Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Digital Parameters								
0x30	OFFS_ST(7:0)							
0x31	OFFS_ST(15:8)							
0x32	OFFS_ST(23:16)							
0x33	OFFS_ST(31:24)							
0x34	0	OFFS_ST(38:32)						
0x35	OFFS_MT(7:0)							
0x36	OFFS_MT(15:8)							
0x37	OFFS_MT(23:16)							
0x38	SPO_S(7:0)							
0x39	SPO_N(2:0)			SPO_S(12:8)				
0x3A	SPO_N(10:3)							
0x3B	UBL_S(1:0)		UBL_M(3:0)				SPO_N(12:11)	
0x3C	UBL_N(2:0)			SBL_S(2:0)			UBL_S(3:2)	
0x3D	MODE_ST(3:0)				SBL_N(2:0)			UBL_N(3)
0x3E	DL_MT(2:0)			DL_ST(4:0)				
0x3F	GRAY_SCD	ELC	ESSI	RSSI	NBISS	M2S(1:0)		DL_MT(3)
0x40	0	CHK_MT	DIR	MODE_MT(1:0)		CFG_E2P(2:0)		
0x41	E2EPR	SWC_MT	GET_MT	NCRC_MT	GRAY_MT	LNT_MT	SBL_MT(1:0)	
0x42	CFGEW(7:0)							
0x43	FRQ_TH(1:0)		NC_BISS	0	S2ERR	S2WRN	PROT_E2P(1:0)	
0x44	0	0	0				AUTORES(1:0)	
0x45								
0x46								
0x47				TRACMODE(1:0)		CALMODE(2:0)		
0x48			DSR(1:0)		DTRI(1:0)		DSC(1:0)	
0x49								
0x4A								
0x4B								
0x4C	CID_SCD(3:0)						TOS(1:0)	
0x4D		0	0	0		0	0	1
0x4E	CRC_E2P(9:2)							
0x4F	CRC_E2P(1:0)							
0x50*	PRES_ST(7:0)							
0x51	PRES_ST(15:8)							
0x52	PRES_ST(23:16)							
0x53	PRES_ST(31:24)							
0x54	0	PRES_ST(38:32)						
0x55	PRES_MT(7:0)							
0x56	PRES_MT(15:8)							
0x57	PRES_MT(23:16)							
0x58 ... 0x74								

OVERVIEW								
Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS Register (with read access)								
0x75	TH_WRN	EPR_ERR	FRQ_WDR	FRQ_STUP	NON_CTR	MT_CTR	MT_ERR	MT_WRN
0x76	ACS_MAX	AM_MIN	AM_MAX	ACM_MIN	ACM_MAX	CT_ERR	RF_ERR	TH_ERR
0x77	CMD_EXE	AN_MIN	AN_MAX	ACN_MIN	ACN_MAX	AS_MIN	AS_MAX	ACS_MIN
COMMAND Register: MN_CMD (with write access)								
0x77	0	0	0	0	0	MN_CMD(2:0)		
Device Identification (preset values after start-up without EEPROM)								
0x78	0x4D ≡ M							
0x79	0x4E ≡ N							
0x7A	Internal identifier (0x04 ≡ Y2)							
0x7B	0	0	0	BANK_ACT*	GRAY_SCD	M2S(1:0)		DL_MT(3)
0x7C	equivalent to address 0x4C							
0x7D	equivalent to address 0x3E							
0x7E	0x69 ≡ i							
0x7F	0x43 ≡ C							
Hints	All registers can be written and read as long as no protection level has been set (see PROT_E2P). Addresses with gray face box are located in the external EEPROM *) Bank selection is active. BANK_ACT = 1, if CFG_E2P /= 000							

Table 7: Register layout

OPERATING MODES and CALIBRATION PROCEDURES

iC-MN supports a number of different calibration strategies, providing both digital and analog test signals to this end. The following tables give the various modes of operation.

For the adjustment of the signal conditioning unit analog test signals are output in analog **calibration modes ANA_x**, with digital signals activated by digital **calibration modes DIG_x**, enabling the signal conditioning to be set across measurements of various duty cycles. The order of the procedure for both modes of calibration is described in the following chapter.

Alternatively, with an active signal level controller iC-MN can be calibrated in **controller modes AAC_x**, where the residual signal ripple is minimized. For this purpose the signal gain, offset and phase correction parameters must be set in such a way that the controller signal CGUCKx available at pin T0 are devoid of AC contents.

In **calibration modes TWIB and TEIB** the temperature monitoring and bias reference source IBP can be adjusted. Here the temperature threshold is set to the required value for either warning or shutdown; the other value is determined by the fixed difference of the switching thresholds.

As the VTTx measurement voltages and CGUCKx signals are only available via a buffer stage the buffer offset voltage must be taken into account if the temperature thresholds are to be adjusted with any accuracy. To this end the buffer offset voltage can be measured in **calibration mode TBOS**. A voltage is then applied to pin T1, with the buffer offset voltage being the difference between this and pin T0.

	Parameter			Output Signals			
Op. Mode	TRACMODE	CALMODE	BYP*	Pins PSOUT, NSOUT, PCOUT, NCOUT	Pin T0	Pin T1	Pin DIR
Normal	0	0		Output of master track via line driver	0	0	-

Table 8: Normal operating mode

	Parameter			Output Signals			
Op. Mode	TRACMODE	CALMODE	BYP*	Pins PSOUT, NSOUT, PCOUT, NCOUT	Pin T0	Pin T1	Pin DIR
Signal calibration modes with VDCx intermediate voltages							
ANA_M	1	0	0	Calib. signals of master chan.	SVDCM	CVDCM	-
	1	0	1	PSINM, NSINM, PCINM, NCINM	SVDCM	CVDCM	-
ANA_S	2	0	0	Calib. signals of segment chan.	SVDCS	CVDCS	-
	2	0	1	PSINS, NSINS, PCINS, NCINS	SVDCS	CVDCS	-
ANA_N	3	0	0	Calib. signals of nonius chan.	SVDCN	CVDCN	-
	3	0	1	PSINN, NSINN, PCINN, NCINN	SVDCN	CVDCN	-
Signal calibration modes with AC noise evaluation (with active sine-square level controlling)							
AAC_M	1	4		Calib. signals of master chan.	CGUCKM		-
AAC_S	2	4		Calib. signals of segment chan.	CGUCKS	-	-
AAC_N	3	4		Calib. signals of nonius chan.	CGUCKN	-	-
Bias calibration, temperature-sensor calibration, and buffer offset measurement							
TWIB	0	5		Output of master track via line driver	VTS_w	VTth	IBP
TEIB	0	6		Output of master track via line driver	VTS_e	$VTth_{err}$	IBP
TBOS	0	7		Output of master track via line driver	BUFFOUT	BUFFIN	-
Notes	S/D conversion modes with a cyclic conversion, such as 0x08, 0x09, 0x0A, are not permitted during signal calibration. Cyclic BiSS data requests must also be avoided due to its trigger for sample-and-hold. Analog calibration signals are output via 5 kΩ source impedance. The maximum permissible signal frequency is 2 kHz for a load of 200 pF (see Elec. Char. 709, 710) * Bypass function: inputs (without voltage divider) to outputs, ca. 7 kΩ source impedance						

Table 9: Operating modes for analog signal calibration

Calibration Using Comparated Sine/Cosine Signals

	Parameter			Output Signals			
Op. Mode	TRACMODE	CALMODE	BYP*	Pins PSOUT, NSOUT, PCOUT, NCOUT	Pin T0	Pin T1	Pin DIR
Signal calibration modes with comparated sine/cosine signals							
DIGO_M	1	1		Calib. signals of master chan.	DIGOFFCOS	DIGOFFSIN	-
DIGA_M	1	2		Calib. signals of master chan.	0	DIGAMP	-
DIGP_M	1	3		Calib. signals of master chan.	0	DIGPHASE	-
DIGO_S	2	1		Calib. signals of segment chan.	DIGOFFCOS	DIGOFFSIN	-
DIGA_S	2	2		Calib. signals of segment chan.	0	DIGAMP	-
DIGP_S	2	3		Calib. signals of segment chan.	0	DIGPHASE	-
DIGO_N	3	1		Calib. signals of nonius chan.	DIGOFFCOS	DIGOFFSIN	-
DIGA_N	3	2		Calib. signals of nonius chan.	0	DIGAMP	-
DIGP_N	3	3		Calib. signals of nonius chan.	0	DIGPHASE	-

Table 10: Operating modes for digital signal calibration

Calibration Of Signal Offsets

Fig. 3: The duty ratio is set accurately to 50 % using parameter OFS_x. This measurement requires a high resolution, for instance of 0.06 %, for calibrating the offset to 0.2 % with reference to the signal amplitude. The resulting interpolation error of 3 LSB (referred to a resolution of 13 bits) corresponds to an angle error of 0.11 degree (360 degree means one signal period).

Fig. 4: The duty ratio is set accurately to 50 % using parameter OFC_x.

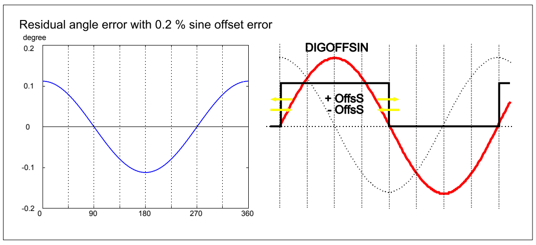


Figure 3: Mode DIGO_x: DIGOFFSIN at Pin T1.

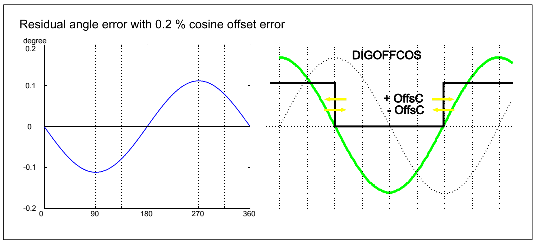


Figure 4: Mode DIGO_x: DIGOFFCOS at Pin T0.

Calibration Of Signal Amplitudes And Phase

Fig. 5: To calibrate the duty cycle to exactly 50 % the fine gain parameters GFC_x und GFS_x can balance the signal amplitudes. If a signal amplitude difference of 0.67 % remains after calibration, the interpolation error enlarges to approx. 4.5 LSB at 13 bit resolution.

Fig. 6: Duty cycle calibration to exactly 50 % is carried out using parameter PH_x. A remaining phase error of 0.7 degree reduces the interpolation accuracy to 10 bit (equal to 8 LSB error at 13 bit resolution, respectively).

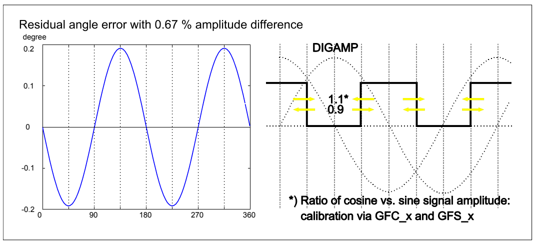


Figure 5: Mode DIGA_x: DIGAMP at Pin T1.

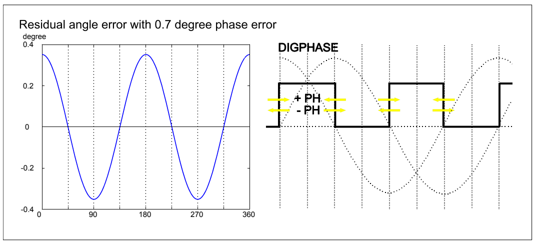


Figure 6: Mode DIGP_x: DIGPHASE at Pin T1.

SIGNAL CONDITIONING for MASTER-, SEGMENT- and NONIUS-Channel (x= M,S,N)

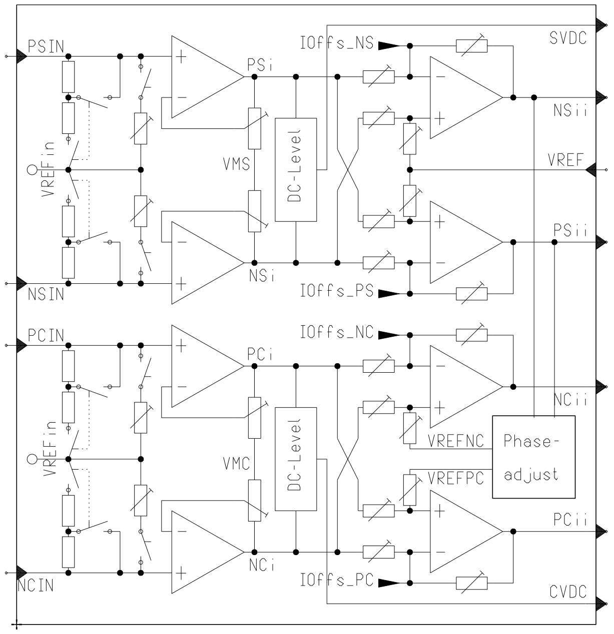


Figure 7: Schematic of Input Stage

The input stages for sine and cosine are instrumentation amplifiers and can process current and voltage signals; selection is made for all three tracks using UIN. Signal conditioning should be performed in the order given in the following.

UIN	Addr. 0x0A; bit 0
Code	Function
0	I Mode: current inputs
1	V Mode: voltage inputs

Table 11: Signal mode

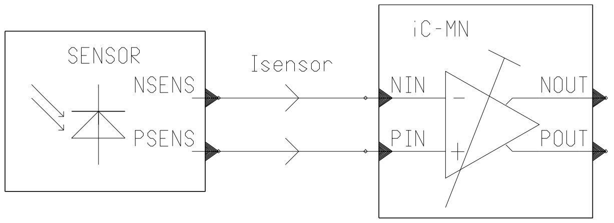


Figure 8: Direction of current flow

Current Signals
For current signals internal reference VREFin is adapted to the input current polarity using DCPOS. The input resistance is set using RIN (1:0). When selecting the input resistance the average potentials SVDC and CVDC should be between 125 mV and 250 mV to obtain a reasonable offset calibration range.

DCPOS	Addr. 0x0A; bit 6	
Code	Polarity I_{sensor}	VREFin()
0	Negative	2.5 V
1	Positive	1.5 V

Table 12: Input current polarity

RIN	Addr. 0x0A; bit 2:1
Code	Resistance
0	1.6 kΩ
1	2.3 kΩ
2	3.2 kΩ
3	4.6 kΩ

Table 13: Input resistance with I mode

Voltage Signals
If the voltage signals are too large the input signal can be quartered by an internal divider. The voltage divider is referenced to the VREFin reference source which is set by DCPOS. In order to use the input voltage range of the input amplifier to its full capacity DCPOS should be set to 1 in voltage divider mode.

TUIN	Addr. 0x0A; bit 3
Code	Function
0	Not active
1	Voltage divider active

Table 14: Input voltage divider

Additionally, using CVREF the user can select whether VREFin is the reference potential generated internally or a voltage provided externally.

CVREF	Addr. 0x0B; bit 4:3
Code	Function
00	Generated internally
01	Reserved
10	Internal VREFin() output to pin ACOS*
11	External ref. voltage supplied to pin ACOS
Note	*) No load permitted, buffer required.

Table 15: VREF Source Selection

All other settings are to be carried out for each individual track separately. A small x in the register name stands for (M)aster, (S)egment and (N)onius respectively.

Gain Adjustment

The gain is set in three stages. The gain range is first determined for sine and cosine using register GR_x (2:0). Register GFC_x (4:0) can then be used to finely adjust the gain of the cosine track. In the final stage of the process the amplitude of the sine track is adapted to suit the cosine track using register GFS_x (10:0). With differential input signals the overall sine gain of one track is thus calculated as GAINS_x = GR_x * GFS_x; the total cosine gain is then GAINC_x = GR_x * GFC_x.

GR_M	Addr. 0x00; bit 2:0
GR_S	Addr. 0x10; bit 2:0
GR_N	Addr. 0x20; bit 2:0
Code	Coarse gain
0	6.0
1	12.4
2	16.2
3	20.2
4	26.0
5	31.6
6	39.5
7	48.0

Table 16: Gain range sine/cosine

GFC_M	Addr. 0x00; bit 7:3
GFC_S	Addr. 0x10; bit 7:3
GFC_N	Addr. 0x20; bit 7:3
Code k	Fine gain $GFC = 6.25^{\frac{k}{31}}$
0x00	1
0x01	1.07
0x02	1.13
...	...
0x1F	6.25

Table 17: Gain factor cosine

GFS_M	Addr. 0x02; bit 2:0
	Addr. 0x01; bit 7:0
GFS_S	Addr. 0x12; bit 2:0
	Addr. 0x11; bit 7:0
GFS_N	Addr. 0x22; bit 2:0
	Addr. 0x21; bit 7:0
Code k	Fine gain $GFS = 6.25^{\frac{k}{1984}}$
0x000	1
0x001	1.0009
0x002	1.0018
...	...
0x7FF	6.6245

Table 18: Gain factor sine

Offset Calibration

When calibrating the offset the offset reference source must first be selected using REFVOS (1:0). This setting is valid for all three tracks. If VDC is selected as the offset reference SVDCx is the reference for the sine track and CVDCx for the cosine. The VDC reference enables the offset calibration to be automatically tracked dependent on the DC level of the input signal. If ACO is chosen as the offset reference the voltage at pin ACOx, divided into $^{1}/_{20}$, acts as a reference. This enables the offset to be calibrated dependent on the supply voltage of the sensor.

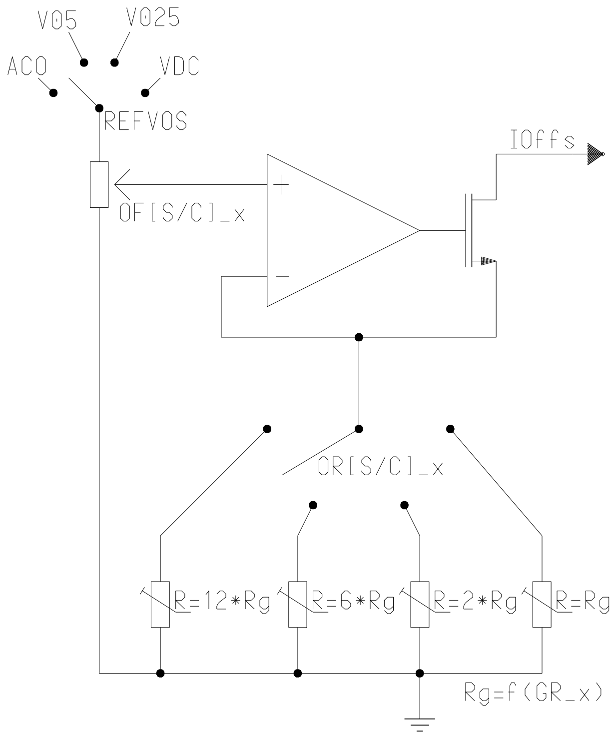


Figure 9: Principle offset calibration circuit with selectable reference sources.

REFVOS	Addr. 0x0A; bit 5:4	
Code	Type of source	
0	Feedback of pin ACO	REFVOS = V(ACOx)/20
1	Reference V05	REFVOS = 0.5 V
2	Reference V025	REFVOS = 0.25 V
3	Tracked source VDC	REFVOS = SVDCx, CVDCx

Table 19: Offset reference source

Source VDC is to be used as reference for current inputs. The average potentials of sine (SVDCx) and cosine (CVDCx) are determined by:

$$SVDCx = (1 - k_s) \cdot V(PSi) + k_s \cdot V(NSi)$$

and

$$CVDCx = (1 - k_c) \cdot V(PCi) + k_c \cdot V(NCi)$$

Using MPS_x (9:0) and MPC_x (9:0) k_s and k_c should be configured in such a way that the AC fraction is minimal with both voltages.

MPS_M	Addr. 0x03; bit 4:0
	Addr. 0x02; bit 7:3
MPS_S	Addr. 0x13; bit 4:0
	Addr. 0x12; bit 7:3
MPS_N	Addr. 0x23; bit 4:0
	Addr. 0x22; bit 7:3
Code	$SVDC = (1 - k_s) \cdot V(PSi) + k_s \cdot V(NSi)$
0x000	$k_s = 0.3333$
0x001	$k_s = 0.3336$
...	...
0x3FF	$k_s = 0.6666$

Table 20: Intermediate voltage sine

MPC_M	Addr. 0x04; bit 6:0
	Addr. 0x03; bit 7:5
MPC_S	Addr. 0x14; bit 6:0
	Addr. 0x13; bit 7:5
MPC_N	Addr. 0x24; bit 6:0
	Addr. 0x23; bit 7:5
Code	$CVDC = (1 - k_c) \cdot V(PCi) + k_c \cdot V(NCi)$
0x000	$k_c = 0.3333$
0x001	$k_c = 0.3336$
...	...
0x3FF	$k_c = 0.6666$

Table 21: Intermediate voltage cosine

The calibration range for the offset of sine and cosine is dependent on the source selected by REFVOS and is set using ORS_x (1:0) and ORC_x (1:0). The offset correction accuracy is influenced with the above.

ORS_M	Addr. 0x05; bit 0
	Addr. 0x04; bit 7
ORS_S	Addr. 0x15; bit 0
	Addr. 0x14; bit 7
ORS_N	Addr. 0x25; bit 0
	Addr. 0x24; bit 7
Code	Range
0	maxVOSS_x = 3 * REFVOS
1	maxVOSS_x = 6 * REFVOS
2	maxVOSS_x = 18 * REFVOS
3	maxVOSS_x = 36 * REFVOS

Table 22: Offset range sine

ORC_M	Addr. 0x06; bit 5:4
ORC_S	Addr. 0x16; bit 5:4
ORC_N	Addr. 0x26; bit 5:4
Code	Range
0	maxVOSC_x = 3 * REFVOS
1	maxVOSC_x = 6 * REFVOS
2	maxVOSC_x = 18 * REFVOS
3	maxVOSC_x = 36 * REFVOS

Table 23: Offset range cosine

The achievable angle accuracy following interpolation is affected by the internal signal strength and the offset calibration step width, depending on the set correction range and reference source. By way of example these dependencies are shown in the following table, for half and full scale signal levels (FS means 6 Vpp).

Range x Source	maxVOSC_x maxVOSS_x	Cal. Step Width (LSB)	Limitation Of Angle Accuracy @ 100 % (6 Vpp) @ 50 % (3 Vpp)
3 x 0.25 V	750 mV	732 µV	none (>13 bit) none (>13 bit)
6 x 0.25 V	1.5 V	1465 µV	none (>13 bit) none (>13 bit)
6 x 0.5 V	3 V	4396 µV	0.08°, ca. 12 bit 0.16°, ca. 11 bit
18 x 0.5 V	9 V	8789 µV	0.16°, ca. 11 bit 0.32°, ca. 10 bit

Table 24: Offset calibration and influence on angle accuracy

The sine and cosine offsets are calibrated by a linear voltage divider using OFS_x (10:0) and OFC_x (10:0).

OFS_M	Addr. 0x06; bit 3:0
	Addr. 0x05; bit 7:1
OFS_S	Addr. 0x16; bit 3:0
	Addr. 0x15; bit 7:1
OFS_N	Addr. 0x26; bit 3:0
	Addr. 0x25; bit 7:1
Code	OFS_x = OffsS_x*maxVOSS_x
0x000	OffsS_x = 0
0x001	OffsS_x = -0.0009
0x002	OffsS_x = -0.0019
...	...
0x3FF	OffsS_x = -1
0x400	OffsS_x = 0
0x401	OffsS_x = 0.0009
0x402	OffsS_x = 0.0019
...	...
0x7FF	OffsS_x = 1

Table 25: Offset voltage sine

OFC_M	Addr. 0x08;	bit 0
	Addr. 0x07;	bit 7:0
	Addr. 0x06;	bit 7:6
OFC_S	Addr. 0x18;	bit 0
	Addr. 0x17;	bit 7:0
	Addr. 0x16;	bit 7:6
OFC_N	Addr. 0x28;	bit 0
	Addr. 0x27;	bit 7:0
	Addr. 0x26;	bit 7:6

Code	OFC_x = OffsC_x*maxVOSC_x
0x000	OffsC_x = 0
0x001	OffsC_x = -0.0009
0x002	OffsC_x = -0.0019
...	...
0x3FF	OffsC_x = -1
0x400	OffsC_x = 0
0x401	OffsC_x = 0.0009
0x402	OffsC_x = 0.0019
...	...
0x7FF	OffsC_x = 1

Table 26: Offset voltage cosine

Phase Correction

The phase between sine and cosine is calibrated by PH_x (9:0). With a phase error of 2.5° or more the amplitude and offset must be readjusted for a track resolution accuracy of 13 bits.

PH_M	Addr. 0x09;	bit 2:0
	Addr. 0x08;	bit 7:1
PH_S	Addr. 0x19;	bit 2:0
	Addr. 0x18;	bit 7:1
PH_N	Addr. 0x29;	bit 2:0
	Addr. 0x28;	bit 7:1

Code	Function
0x000	+ 0 °
0x001	+ 0.0204 °
...	...
0x1FF	+ 10.396 °
0x200	- 0 °
0x201	- 0.0204 °
...	...
0x3FF	- 10.396 °

Table 27: Sine/cosine phase correction

ANALOG PARAMETERS

Signal Level Controller

By tracking the sensor's power supply via the controlled current sources (outputs ACOM, ACOS and ACON) iC-MN can keep the sine/cosine track signals for the ensuing sine-to-digital converter constant regardless of temperature and aging effects.

When adjusting the signal conditioning a constant current source is used in place of the controlled current source, the set current of which can be adjusted using ACOR_M(6:0) or ACOR_x(5:0) (x = S, N). This current must be so low as to leave enough reserve for temperature and aging effects and ensure that no unnecessary power dissipation is generated. However, the source current may not be too low so as to permit a better signal contrast and improved signal to noise ratio. Using this current the signal calibration can then be performed so that the sine/cosine signals at the sine-to-digital converter have a (differential) value of 6 Vpp in their calibrated state. Once calibration has proved successful the signal level controller can be activated.

There are three integrated signal level control units in iC-MN, all of which are powered by VACO. It is thus possible to regulate each track individually or, in optical systems with an LED, for example, all three tracks using the master signal level controller. If the control unit's working range is exceeded, an error is generated.

ACOT_M(8:7)	Addr. 0x0D; bit 0 Addr. 0x0C; bit 7
Code	Operating mode
00	Quadratic regulation active*
01	Sum regulation active
10	Constant current source mode
11	Not permitted
*) Quadratic regulation of V()scq = $\sqrt{(V(PSOUT - V(NSOUT))^2 + (V(PCOUT - V(NCOUT))^2}$	

Table 28: Controller op. mode, ACOM output

ACOR_M(6:5)	Addr. 0x0C; bit 6:5
Code	Current range I_{max}(ACOM)
00	5 mA
01	10 mA
10	25 mA
11	50 mA

Table 29: Current source range, ACOM output

ACOC_M(4:0)	Addr. 0x0C; bit 4:0
Code	Setpoint
0x00	3.125% * I_{max}(ACOM)
0x01	6.25% * I_{max}(ACOM)
...	...
0x1E	96.875% * I_{max}(ACOM)
0x1F	100% * I_{max}(ACOM)

Table 30: Current source setpoint, ACOM output

ACOT_S(7:6) **ACOT_N(7:6)**	Addr. 0x1D; bit 0 Addr. 0x1C; bit 7 Addr. 0x2D; bit 0 Addr. 0x2C; bit 7
Code	Operating mode
00	Quadratic regulation active
01	Sum regulation active
10	Constant current source mode
11	Not permitted

Table 31: Controller op. mode, ACOS/ACON outputs

ACOR_S(5) **ACOR_N(5)**	Addr. 0x1C; bit 5 Addr. 0x2C; bit 5
Code	Current range I_{max}(ACOS), I_{max}(ACON)
0	5 mA
1	10 mA

Table 32: Current source range, ACOS/ACON outputs

ACOC_S(4:0) **ACOC_N(4:0)**	Addr. 0x1C; bit 4:0 Addr. 0x2C; bit 4:0
Code	Setpoint
0x00	3.125% * I_{max}(ACOS, ACON)
0x01	6.25% * I_{max}(ACOS, ACON)
...	...
0x1E	96.875% * I_{max}(ACOS, ACON)
0x1F	100% * I_{max}(ACOS, ACON)

Table 33: Current source setpoint, ACOS/ACON output

Bias Current Source

The calibration of the bias current source in operation mode *TWIB* or *TEIB* is prerequisite for adherence to the given electrical characteristics and also instrumental in the determination of the chip timing (e.g. SCL clock frequency). For the calibration of source IBP to its target value of 200 µA the voltage across the 5 kΩ measurement resistor has to be adjusted to 1 V.

CFGIBP	Addr. 0x0D; bit 4:1
Code k	$IBP \sim \frac{31}{31-k}$
0x0	100.00 %
0x1	103.3 %
...	...
0xF	193.7 %

Table 34: Bias current source calibration

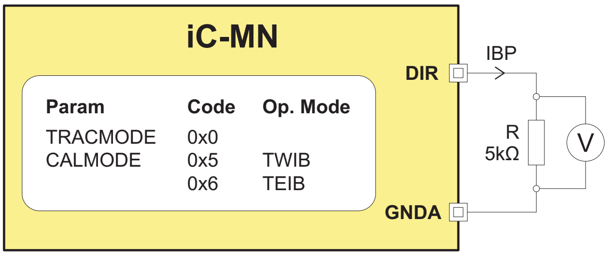


Figure 10: Measurement circuit

Temperature Sensor

As regards temperature two settings can be made; either a temperature threshold for an excessive temperature warning or an excessive temperature error can be set. The excessive temperature error and warning are coupled to one another (see Characteristics C07). Calibration of the excessive temperature warning in calibration mode *TWIB* is described by way of example.

To set the required warning temperature T_w the temperature sensor voltage $VTS_w(T_{curr})$ at which the warning is generated is first determined. T_{curr} is the actual temperature. To this end a voltage ramp from VDD towards GND is applied to pin T1 until pin NERR indicates the error message. The necessary activation threshold voltage $VTth(T_{curr})$ is then calculated. The required warning temperature T_w, temperature coefficients TCs and TCth (see Electrical Characteristics, Section C) and measurement value $VTS_w(T_{curr})$ are entered into this calculation:

$$VTth(T_{curr}) = \frac{VTS_w(T_{curr}) + TCs \cdot (Tw - T_{curr})}{1 + \frac{TCth}{1+TCth\cdot(T_{curr}-T_{norm})} \cdot (Tw - T_{curr})}$$

The reference temperature T_{norm} is 27 °C. Activation threshold voltage $VTth(T_{curr})$ is provided for a high impedance measurement (10 MΩ) at output pin T0 and must be set by programming CFGTA(4:0) to the calculated value.

CFGTA	Addr. 0x0E; bit 1:0 Addr. 0x0D; bit 7:5
Code k	$VTth \sim \frac{100+5k}{100}$
0x00	100 %
0x01	105 %
...	...
0x1F	255 %

Table 35: Calibration of temperature monitoring

Signal Noise Filters

iC-MN has a noise filter for both the analog output drivers and the sine-to-digital converter. These filters can be activated by ENF.

ENF(0)	Addr. 0x0E; bit 1
Code	Function
0	Disabled
1	Sin/Cos Output driver noise filter activated

Table 36: Noise filter for the output drivers

ENF(1)	Addr. 0x0E; bit 2
Code	Function
0	Disabled
1	S/D Conversion noise filter activated

Table 37: Noise filter for the sine-to-digital converter

SINE-TO-DIGITAL CONVERSION MODES

iC-MN has two principle modes of operation. In **nonius modes** 2 or 3 tracks are combined by a nonius calculation with synchronization; in **multiturn modes** the up to 3 tracks are combined to form an absolute word via gear box code synchronization.

The used and synchronization bit lengths (parameters UBL_x and SBL_x) are selectable for both operating modes; in multiturn modes it is also possible to output unsynchronized data from all tracks.

With both principle operating modes iC-MN offers various sine-to-digital conversion modes. With a data request via the I/O interface this determines:

- The sample time and thus the ”age” of the output data
- The necessary processing time prior to generation of the output data word.

Internal Bit Lengths

The used bit length is set for the master, segment and nonius tracks using registers UBL_M, UBL_S and UBL_N. From these used bits the internal singleturn data word is then generated, for which purpose synchronization bits are used. The bit lengths used for synchronization can be set separately via register SBL_S for the segment track and register SBL_N for the nonius track. Limitations governing the settable bit lengths are summarized in Table 41.

UBL_M	Addr. 0x3B; bit 5:2
Code	Bit length master
0x00	0
0x01..0x03	not permitted
0x04	4
...	...
0x0D	13

Table 38: Bit length master

UBL_S	Addr. 0x3C; bit 1:0
	Addr. 0x3B; bit 7:6
UBL_N	Addr. 0x3D; bit 0
	Addr. 0x3C; bit 7:5
Code	Used bit length
0x00	0
...	...
0x0D	13

Table 39: Used bit length for segment and nonius

SBL_S	Addr. 0x3C; bit 4:2
SBL_N	Addr. 0x3D; bit 3:1
Code	Synchronization bit length
0x00	0
...	...
0x04	4

Table 40: Synchronization segment and nonius

Track	Count of bits processed	Possible bit count $\sum$
Master	UBL_M	0, 4..13
Segment	UBL_S+SBL_S	0, 4..13
Nonius	UBL_N+SBL_N	0, 4..13

Table 41: Possible bit counts for UBL_M and UBL_x+SBL_x

S/D CONVERSION with NONIUS CALCULATION

For the nonius modes iC-MN has a flash counter which counts the zero crossings of the master track. When the system is started this flash counter is preloaded with the absolute period information which has been most recently calculated using the nonius and segment tracks (or only the nonius track).

The output data word always is the flash counter value synchronized with the master track. Furthermore, it is possible to output synchronized singleturn and multiturn position data which can be set using the parameter MODE_MT (see page 46).

MODE_ST	Addr. 0x3D; bit 7:4
Operation modes with nonius calculation (Nonius Modes)	
Code	Description
	Data outp. following S/D conversion of master track
0x00	Period verification disabled
0x01	Frequency-dependent period verification
0x02	Period verification enabled
	Data output following S/D conversion of all tracks
0x03	Frequency-dependent period verification
0x04	Period verification enabled
	Zero-delay data output: result of previously triggered S/D conversion
0x05	Period verification disabled
0x06	Frequency-dependent period verification
0x07	Period verification enabled
	Zero-delay data output: last result of background S/D conversion (asynchronous)
0x08	Period verification disabled
0x09	Frequency-dependent period verification
0x0A	Period verification enabled
	Zero-delay data output: last result of S/D conversion triggered by pin T3
0x0B	Period verification enabled
Notes	On changing parameter MODE_ST during operation command SOFT_RES should be issued. Modes 0x08, 0x09, 0x0A are not permitted during calibration via Op.Mode's ANA_x oder DIGx_x.

Table 42: Nonius modes

Output Data Verification

It is possible to verify the counted period when a nonius calculation has been completed. Possible settings include:

1. No verification of counted periods
2. Frequency-dependent verification of counted periods. Exceeding the maximum master track signal frequency set by FRQ_TH (see Table 46) disables the flash counter verification versus nonius calculation. If the limit is again undershot, future conversions are again verified.
3. Period verification versus nonius calculation is always enabled and executed with each conversion.

Op. Mode Descriptions Of Nonius Modes

MODE_ST Codes 0x00, 0x01, 0x02

With this mode the processing time is largely determined by the conversion time of the master track. The conversion procedure is as follows:

1. A data readout request triggers the conversion of all selected tracks
2. Following conversion of the master track: synchronization with the internal flash counter and output of the synchronized postion value
3. During data readout: conversion of the remaining tracks and nonius calculation
4. Generation of NON_CTR with the next data readout cycle

MODE_ST Codes 0x03, 0x04

The processing time is largely determined by the sum of the conversion time of the tracks for conversion. The conversion procedure is as follows:

1. A data readout triggers the complete conversion of the set tracks
2. Following conversion of the master track: synchronization with the internal flash counter
3. Following conversion of the remaining tracks: nonius calculation and generation of NON_CTR

4. Transmission of the synchronized position value. The transmitted NON_CTR counts as part of the current conversion.

MODE_ST Codes 0x05, 0x06, 0x7
The processing time is low as "old" data is transmitted, the time of sampling is, however, known (NB: The data from the first readout is invalid following a SOFT_RES). The conversion procedure is as follows:

1. With a data readout: immediate transmission of the data from the last readout cycle including the relevant NON_CTR
2. With a data readout: start of a new conversion and providing of data for the next data readout cycle. NON_CTR is output directly at the NERR pin.

MODE_ST Codes 0x08, 0x09, 0xA
The processing time is low and the time of sampling not precisely known. The conversion procedure is as follows:

1. Regardless of the data readout: permanent background conversion
2. With a data readout: transmission of current data. Each NON_CTR is output directly at the NERR pin. In data transmission a NON_CTR error is only signaled when the error occurs during the relevant nonius calculation.

MODE_ST Code 0x0B
This mode can be used in systems in which sampling must be synchronized to a frequency determined externally and independent of the data readout cycles. The conversion procedure is as follows:

1. A conversion with nonius synchronization is triggered via pin T3. NON_CTR is output directly at the NERR pin.
2. With a data readout the most recent conversion data triggered by pin T3 is transmitted including the relevant NON_CTR.

Principle PPR And Bit Length Dependencies
With a nonius system with three tracks UBL_M must be set so that it is at least as large as the maximum value of MAX(UBL_S+SBL_S, UBL_N+SBL_N). If only two tracks are used, UBL_S and SBL_S must be set to zero. UBL_M must then at least match the maximal value of MAX(UBL_N+SBL_N).

The necessary number of signal periods per revolution for the individual tracks is then determined by the selected used bit lengths:

Track	Required signal periods
Master	$2^{UBL\_S+UBL\_N}$
Segment	$2^{UBL\_S+UBL\_N} - 2^{UBL\_N}$
Nonius	$2^{UBL\_S+UBL\_N} - 1$

The following tables show the possible settings and required number of signal periods. The total physical angle resolution in nonius mode is obtained from the sum of UBL_M+UBL_S+UBL_N. At the same time the bit lengths set for synchronization determine a limit up to which a nonius calculation is possible. This limit is given in Table 45 as the maximum tolerable phase deviation which may occur between the segment and master track or nonius and master track (with reference to the electrical 360° period of the master signal).

Bits/Track		Signal periods/Turn			Physical resolution a)	
UBL_S	UBL_N	Master	Segm.	Nonius	min b)	max
2	2	16	12	15	2+2+4	2+2+13
3	2	32	28	31	2+3+5	2+3+13
3	3	64	56	63	3+3+5	3+3+13
4	3	128	120	127	3+4+6	3+4+13
4	4	256	240	255	4+4+6	4+4+13
5	4	512	496	511	4+5+7	4+5+13
5	5	1024	992	1023	5+5+7	5+5+13
6	5	2048	2016	2047	5+6+8	5+6+13
6	6	4096	4032	4095	6+6+8	6+6+13

a) For configuration of the output data length, see Table 51
b) For the minimum data length SBL_x = 0x02 is assumed

Table 43: Settings for 3-track nonius mode

Bits/Track	Signal periods/Turn		Physical resolution a)	
UBL_N	Master	Nonius	min b)	max
4	16	15	4+6	4+13
5	32	31	5+7	5+13
6	64	63	6+8	6+13

a) For configuration of the output data length, see Table 51
b) For the minimum data length SBL_x = 0x02 is assumed

Table 44: Settings for 2-track nonius mode

UBL_N/ UBL_S	SBL_N/ SBL_S	Permissible Max. Phase Deviation [given in degree per signal period of 360°]
2	2	+/- 22.5°
	3	+/- 33.75°
	4	+/- 39.38°
3	2	+/- 11.25°
	3	+/- 16.88°
	4	+/- 19.69°
4	2	+/- 5.63°
	3	+/- 8.44°
	4	+/- 9.84°
5	2	+/- 2.81°
	3	+/- 4.22°
	4	+/- 4.92°
6	2	+/- 1.41°
	3	+/- 2.11°
	4	+/- 2.46°

Table 45: Tolerable phase deviation for the master versus the nonius or segment track (with reference to 360°, electrical)

The synchronization principle is summarized in Figure 11, where φ represents the digitized angle of the relevant track.

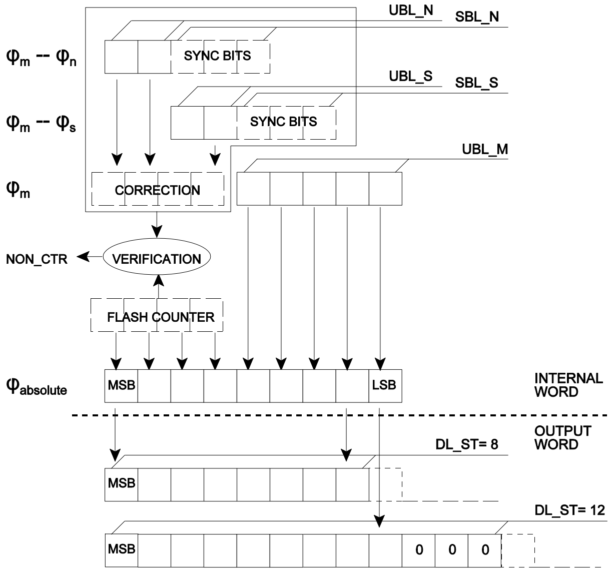


Figure 11: Principle of nonius mode synchronization

Digital Frequency Monitoring

iC-MN features an integrated frequency monitoring circuit for the master track. A signal frequency warning threshold can be configured by FRQ_TH.

FRQ_TH	Addr. 0x43; bit 7:6
Code	Warning Threshold
00	7.625 kHz
01	31.25 kHz
10	62.5 kHz
11	125 kHz

Table 46: Signal frequency monitoring

FRQ_TH is used by the frequency-dependent period verification feature available for nonius modes (see MODE_ST = 0x01, 0x03, 0x06 and 0x09).

The following applies to all modes with nonius synchronization: if the frequency of the master track is too high at power on, FRQ_STUP and FRQ_WDR remain set until the period verification was successful below the frequency warning threshold. In nonius modes without an enabled period verification it must be observed that FRQ_STUP remains permanently set and can only be reset by SOFT_RES when the warning threshold is undershot.

S/D CONVERSION with MULTITURN SYNCHRONIZATION

In multiturn modes the output data word always matches the current converted and synchronized track data. For 1 to 3 selected tracks parameters SBL_S and SBL_N adjust the gear box synchronization, whereas the selected used bit lengths (UBL_x) determine the reduction ratio required for the multiturn gear box:

Synchronization	Gear reduction
Master track ↔ Singleturn	2^{UBL_M}
Segment track ↔ Master track	2^{UBL_S}
Nonius track ↔ Segment track	2^{UBL_N}

One limitation in multiturn mode is that neither an external multiturn can be configured nor counted multiturn data output. Parameters MODE_MT and M2S must be set to 0. Figure 12 shows the synchronization principle, where φ represents the digitized angle of the relevant track.

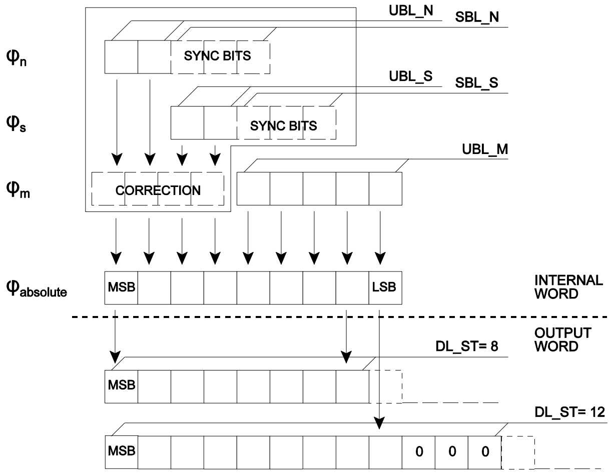


Figure 12: Principle of multiturn synchronisation

MODE_ST	Addr. 0x3D; bit 7:4
Operation modes with multiturn synchronization (MT Modes)	
Code	Description
0x0C	Data output following S/D conversion of all tracks with MT synchronization configured via SBL_x
0x0D	Data output: result of previously triggered S/D conversion with MT synchronization configured via SBL_x
0x0E	Data output: last result of background S/D conversion (asynchronous) with MT synchronization configured via SBL_x
0x0F	Data output: last result of S/D conversion triggered by pin T3 with MT synchronization configured via SBL_x
Notes	On changing parameter MODE_ST during operation command SOFT_RES should be issued.

Table 47: Multiturn modes

Op. Mode Descriptions Of Multiturn Modes

MODE_ST Code 0x0C
The processing time is largely determined by the sum of the conversion time of the configured tracks. Procedure of conversion:

1. A data readout request triggers the complete conversion of the set tracks
2. Gear box synchronization
3. Transmission of the output data

MODE_ST Code 0x0D
The processing time is low as ”old” data is transmitted, the time of sampling is, however, known. The conversion procedure is as follows:

1. With a data readout: immediate transmission of the data from the last readout cycle
2. With a data readout: start of a new conversion and providing of data for the next readout cycle.

NB: The data from the first readout is invalid following a SOFT_RES.

MODE_ST Code 0x0E
The processing time is low and the time of sampling not precisely known. The conversion procedure is as follows:

1. Regardless of the data readout: permanent background conversion
2. With a data readout: transmission of current data.

MODE_ST Code 0x0F
This mode can be used in systems which require that asynchronous sampling is independent of the data readout timing. The conversion procedure is as follows:

1. A conversion is triggered via pin T3, if applicable with gear box code synchronization.
2. With a data readout the most recent output data triggered by pin T3 is transmitted.

S/D CONVERSION with DIRECT OUTPUT

iC-MN functions as a simultaneous sampling, 3-channel sine-to-digital converter when the multiturn modes are selected with deactivated synchronization. When SBL_S = 0 and SBL_N = 0 no track synchronization takes place; the data from all three tracks is queued up for output without any further processing.

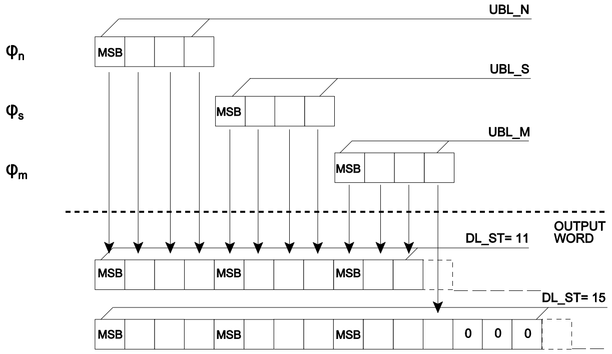


Figure 13: Principle of simultaneous sampling, 3-channel S/D conversion with direct data output

MODE_ST	Addr. 0x3D; bit 7:4
Direct output via MT modes with deactivated synchronization	
Code	Description
0x0C	Data output following S/D conversion of all tracks; synchronization disabled (SBL_x = 0)
0x0D	Data output: result of previously triggered S/D conversion; synchronization disabled (SBL_x = 0)
0x0E	Data output: last result of background S/D conversion (asynchronous); synchronization disabled (SBL_x = 0)
0x0F	Data output: last result of S/D conversion triggered by pin T3; synchronization disabled (SBL_x = 0)
Notes	On changing parameter MODE_ST during operation command SOFT_RES should be issued.

Table 48: MT modes used for direct output

Op. Mode Descriptions Of Direct Output Modes

MODE_ST Code 0x0C

The processing time is largely determined by the sum of the conversion time of the configured tracks. The conversion procedure is as follows:

1. A data readout request triggers the complete conversion of the set tracks
2. Transmission of the output data

MODE_ST Code 0x0D

The processing time is low as ”old” data is transmitted, the time of sampling is, however, known (NB: The data from the first readout is invalid following a SOFT_RES). The conversion procedure is as follows:

1. With a data readout: immediate transmission of the data from the last readout cycle
2. With a data readout: start of a new conversion and providing of data for the next readout cycle.

MODE_ST Code 0x0E

The processing time is low and the time of sampling not precisely known. The conversion procedure is as follows:

1. Regardless of the data readout: permanent background conversion
2. With a data readout: transmission of current data.

MODE_ST Code 0x0F

This mode can be used especially for resolver systems, in which 1 to 3 channels need to be sampled in synchronism with a specific carrier frequency. An external trigger signal supplied to pin T3 takes over the sampling control and thus decouples it from the data readout timing. The conversion procedure is as follows:

1. A conversion is triggered by pin T3
2. With a data readout the most recent output data triggered by pin T3 is transmitted.

TRACK OFFSET CALIBRATION

Depending on the track resolution the offset values of the nonius and segment tracks (POV = Phase-Offset-Value) must be justified to the left in the SPO_N and SPO_S registers. These offsets are added to the conversion result of each track prior to synchronization and are instrumental in calibrating the track.

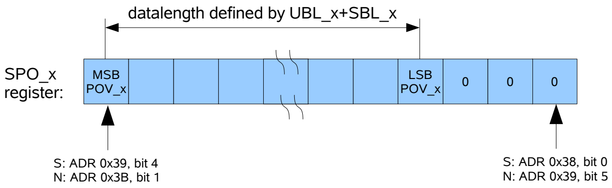


Figure 14: SPO_x (x=S,N)

SPO_N	Addr. 0x3B;	bit 1:0
	Addr. 0x3A;	bit 7:0
	Addr. 0x39;	bit 7:5
SPO_S	Addr. 0x39;	bit 4:0
	Addr. 0x38;	bit 7:0
0x0000 . . . 0x1FFF	Track Offset	

Table 49: Track offsets for nonius and segment

Note: For nonius synchronization (see MODE_ST) it is important that the used tracks within the $2^{UBL\_S+UBL\_N}$ master track periods have a shared zero crossing once. With SPO_S or SPO_N the segment and nonius tracks can be shifted to the master track accordingly.

I/O INTERFACE

Protocol

iC-MN can transmit position data according to the SSI protocol where both data length and error messaging are configurable. The selected mode of operation for sine-to-digital conversion can limit the permissible SSI clock frequency (see Operating Conditions on page 15). The highest possible SSI clock frequency of 4 MHz is permissible for converter modes with an immediate data output.

TOS	Addr. 0x4C; bit 1:0	
Code	Timeout t_{out}	Internal clock counts
00	typ. 16 µs	31-32
01	typ. 8 µs	15-16
10	typ. 2 µs	3-4
11	typ. 1 µs	1-2
Notes	One clock count is equal to $\frac{4}{fosc}$ (see Char. A01)	

Table 50: Timeout

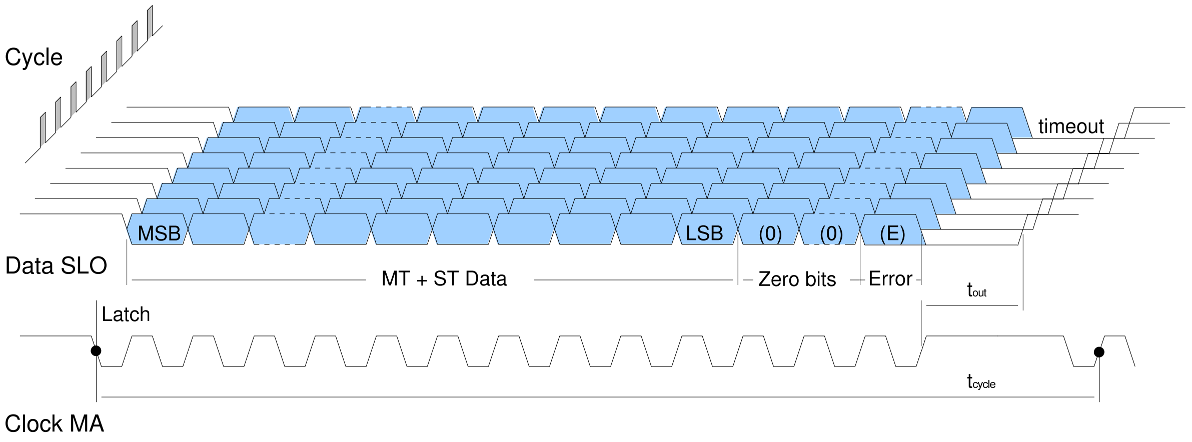


Figure 15: Example of SSI line signals

Output Data Length

For singleturn data lengths (DL_ST) which are less than 13 bits the SSI data word is zero filled. The optional error bit is always the final bit of the data word.

If enabled by M2S, multiturn data is always transmitted upfront the singleturn data. The format option Gray or binary code covers the MT and ST data word in its entirety; filled in zeros and the error bit remain untouched.

The output bit count is determined by parameters DL_ST, M2S and ESSI:

max(13, DL_ST+ESSI) + MT bits

Example: *DL_ST = 0 (≡8 Bit); ESSI = 1.*

Result: 8 bits of data + 4 zeros + 1 error bit are transmitted = 13 bits of data.

DL_ST	Addr. 0x3E; bit 4:0
Code	Bit count
0x00	8 bit plus zeroes (+1 error bit)*
...	...
0x05	13 bit (+1 error bit)*
...	...
0x11	25 bit (+1 error bit)*
	Bit counts listed below are valid only for multiturn synchronization mode (s.P. 30 ff.)
0x12	26 bit (+1 error bit)*
...	...
0x19	33 bit (+1 error bit)*
0x1A	39 bit (+1 error bit)*
Notes	*) When enabled by ESSI = 1

Table 51: ST Data length

M2S	Addr. 0x3F; bit 2:1
Code	Function
00	no output
01	MT data output of lowest 4 bits
10	MT data output of lowest 8 bits
11	Complete output, MT bit count following DL_MT

Table 52: MT Data output

Output Options

ESSI	Addr. 0x3F; bit 5
Code	Error bit output
0	Not included
1	Error bit enabled

Table 53: Error bit

GRAY_SCD	Addr. 0x3F; bit 7
Code	Data format
0	Binary coded
1	Gray coded

Table 54: Data format (covers MT and ST data)

RSSI	Addr. 0x3F; bit 4
Code	Ring operation
0	Normal output If the clock count exceeds the data length, zero bits are supplied.
1	Ring operation
Notes	When enabling RSSI with the BiSS C protocol, pin SLI reads in data to be output via SLO.

Table 55: Ring operation

The behavior of the output data depending on the sense of rotation can be altered using pin DIR or via register DIR. Both signals are EXOR-gated and switch output data from increasing to decreasing values or vice versa.

DIR	Addr. 0x3D; bit 6
Code	Code direction
0	Not inverted
1	Inverted

Table 56: Code direction up/down

I/O INTERFACE with EXTENDED FUNCTIONS

Protocol

For the fast and safe transmission of converter data iC-MN's serial I/O interface has a BiSS C protocol which enables bidirectional register communication without changing the permanent cyclic data output. In order to simplify master implementation at the control unit end this protocol does not utilize multicycle data.

Alternatively, an *advanced SSI protocol* can be selected which permits unidirectional register communication for the transferral of parameters from the master to the slave iC-MN.

NBISS	Addr. 0x3F; bit 3
Code	Protocol
0	BiSS C protocol (NC_BiSS = 0, RSSI = 1)
1	Advanced SSI protocol (NC_BiSS = 0)
1	SSI protocol (NC_BiSS = 1)

Table 57: Interface protocol

TOS	Addr. 0x4C; bit 1:0	
Code	Timeout t_{out}	Internal clock counts
00	typ. 16 µs	31-32
01	typ. 8 µs	15-16
10	typ. 2 µs	3-4
11	typ. 1 µs	1-2
Notes	One clock count is equal to $\frac{4}{fosc}$ (see Char. A01)	

Table 58: Timeout

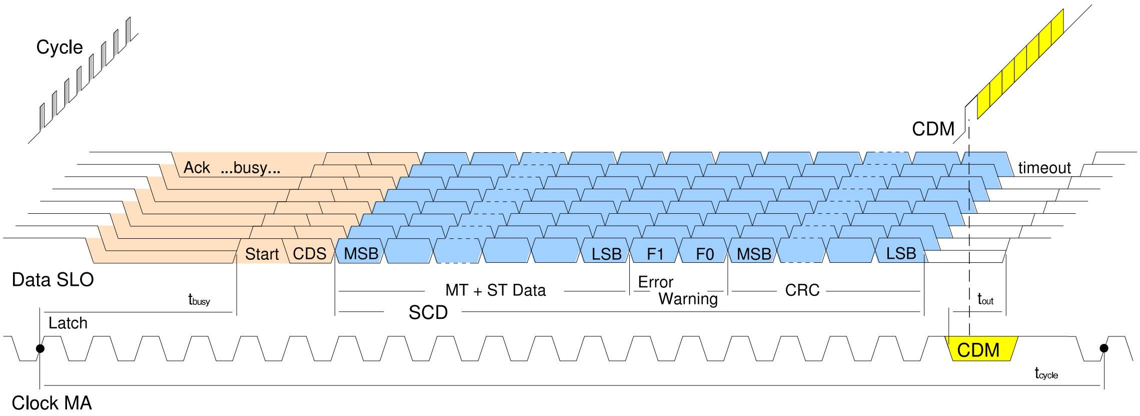


Figure 16: Example of line signals for BiSS C protocol

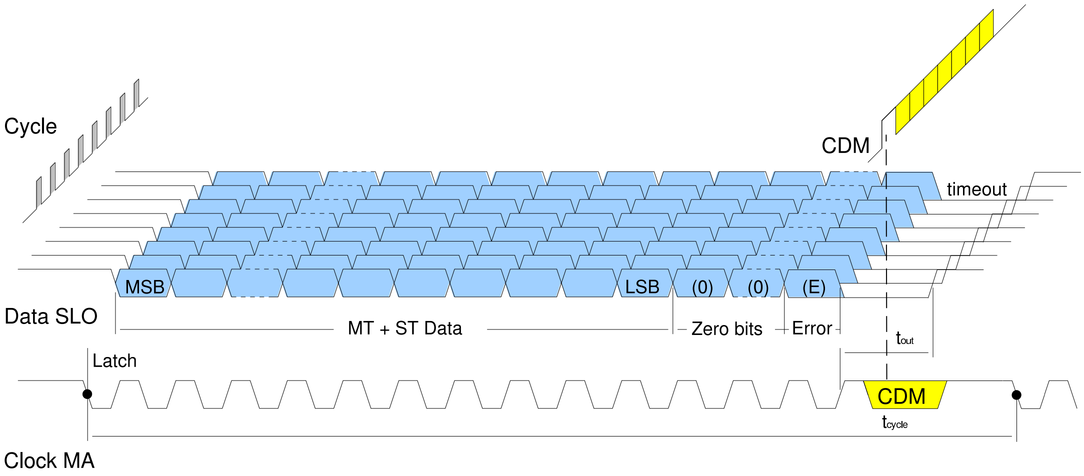


Figure 17: Example of line signals for *Advanced SSI protocol*

Output Data Length

The output bit count is derived from the parameters DL_ST, M2S and DL_MT. In accordance with the selected protocol two additional bits for the error and warning messages are always transmitted.

The output bit length for singleturn data can be set independent of the internal converter resolution. For bit lengths which exceed the internal word length the data following the LSB is zero filled. If enabled by M2S multiturn data is always transmitted before singleturn data.

DL_ST	Addr. 0x3E; bit 4:0
Code	Bit count
0x00 ... 0x05 ... 0x11	8 bit +2 bit for E/W ... 13 bit +2 bit for E/W ... 25 bit +2 bit for E/W
	Bit counts listed below are valid only for multiturn synchronization mode (see P. 30)
0x12 ... 0x19 0x1A	26 bit +2 bit for E/W ... 33 bit +2 bit for E/W 39 bit +2 bit for E/W

Table 59: ST Data length

M2S	Addr. 0x3F; bit 2:1
Code	Function
00	No output
01	MT data output of lowest 4 bits
10	MT data output of lowest 8 bits
11	Complete output, MT bit count following DL_MT

Table 60: MT Data output

Output Options

The Gray or binary code format option covers the singlecycle word in its entirety (MT and ST data); only filled in zeros and the error and warning bits remain unaltered.

GRAY_SCD	Addr. 0x3F; bit 7
Code	Data format
0	Binary coded
1	Gray coded

Table 61: Data format (covers MT and ST data)

The code direction of the output data word can be altered using pin DIR or register DIR. Both signals are EXOR-gated and together comprise the internal direction of rotation signal.

DIR	Addr. 0x3D; bit 6
Code	Direction of rotation
0	Not inverted
1	Inverted

Table 62: Inversion of code direction

For reasons of data security iC-MN provides fixed CRC polynomials (see Table 63). The CRC start value can be freely selected, thus enabling a PLC to clearly allocate data to the source (for safety applications). Register communication can be optionally blocked by parameter NC_BiSS.

Data Channel	CRC HEX Code	Polynomial	Calculation Start Value
SCD	0x43	$x^6+x^1+x^0$	see CID_SCD
CDM, CDS	0x13	$x^4+x^1+x^0$	0x0

Table 63: BiSS CRC polynomials

CID_SCD	Addr. 0x4C; bit 7:4
Code	CRC start value SCD
0x00 . . . 0x0F	CID_SCD

Table 64: CRC start value for SCD

NC_BISS	Addr. 0x43; bit 2
Code	Function
0	BiSS C register communication enabled
1	Communication disable (no execution of commands, no access to RAM or EEPROM
Notes	If the device setup and a set communication disable NC_BiSS are to be stored to the EEPROM, the preset function can be triggered at pin PRES.

Table 65: Communication disable

Safety Application Settings
It is possible to transmit a life counter value in the sensor data for safety applications. When the life counter is activated, a 6-bit counter value is transmitted in the sensor data which is incremented with each new sensor data readout. The life counter has a range of 1 to 64.

ELC	Addr. 0x3F; bit 6
Code	Function (only with BiSS C protocol)
0	Life counter not active
1	Life counter enabled

Table 66: Life counter

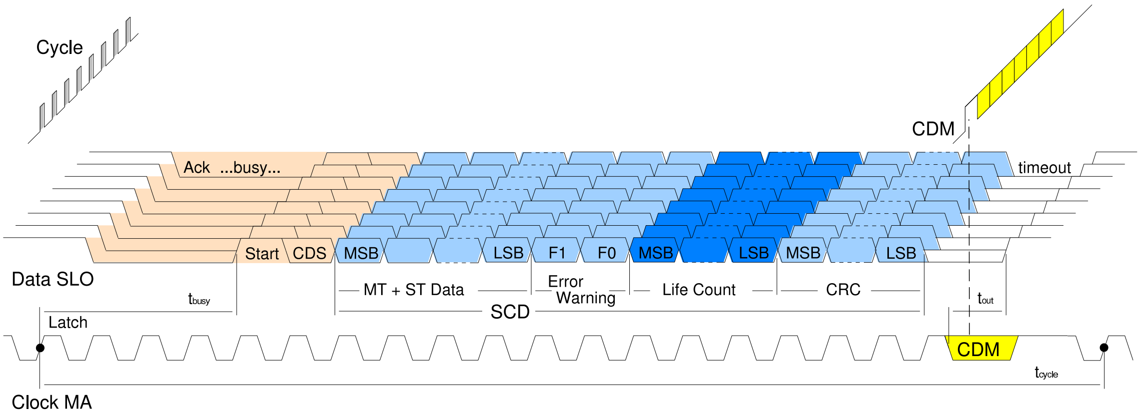


Figure 18: Example of line signals for BiSS C protocol with life counter

Busy Register
iC-MN has a 16-bit busy register. If, for example, two identically configured iC-MNs are connected up to the BiSS master as slaves in a chain, with the help of the busy register an internal clock jitter can be avoided which could lead to different data conversion times for the two slaves. Should the busy register not be sufficient, i.e. should iC-MN need longer to convert data than the subsequent slave, iC-MN generates the start bit and marks the data it has output as faulty. This ensures that the data of the ensuing slave is not lost.

CONFIGURATION OF DIGITAL DRIVER OUTPUTS

The digital outputs SLO and NSLO can be used as either a push-pull, lowside or highside driver. The mode of operation is determined by DTRI. The driving capability is set via the short-circuit current parameter.

In order to meet RS422 specifications a short-circuit current of 50 mA should be selected as well as to reduce the internal power dissipation. The driving capability can be reduced when external line drivers are used.

In order to reduce crosstalk and to improve EMC the slew rate can be selected to suit the line length. If the edge steepness is reduced to 300 ns the maximum permissible transmission frequency is limited to ca. 300 kHz if RS422 specifications are to be adhered to.

DTRI	Addr. 0x48; bit 3:2
Code	Operating mode
00	Push-pull operation
01	Highside driver mode (P channel open drain)
10	Lowside driver mode (N channel open drain)
11	Not permitted

Table 67: Driver output mode

DSC	Addr. 0x48; bit 1:0
Code	Short-circuit current
00	50 mA
01	20 mA
10	4 mA
11	1.2 mA

Table 68: Driver short-circuit current

DSR	Addr. 0x48; bit 5:4	
Code	Slew rate	Permissible transmission frequency
00	10 ns	10 MHz max.
01	30 ns	3 MHz max.
10	100 ns	1 MHz max.
11	300 ns	300 kHz max.

Table 69: Driver slew-rate

COMMAND and STATUS REGISTERS

Execution Of Internal Commands

The command register at address 0x77 can be accessed fully independent of the internal state of operation. Depending on the data value written to this register the execution of an implemented command is triggered.

MN_CMD	Addr. 0x77; bit 2:0	W
Code	Command	Description
0x0	SOFT_RES	Soft reset (new startup using internal config. data)
0x1	WRITE_CONF	Transfers internal config. data to the EEPROM
0x2	SOFT_PRES	Calls preset routine
0x3	CRC_CHECK	CRC verification of the internal config. data
0x4	TOG_BISS	Temporal toggle of interface protocol: BiSS C ↔ SSI
...0xF	No function	

Table 70: Implemented commands

The command **SOFT_RES** resets internal state machines, counters, and the status registers. The configuration RAM is not reset here. During the command execution a write access to the configuration RAM is still possible, whereas the external EEPROM is not accessible.

If the device is in nonius mode (see page 30), the first conversion is used to determine the period and the result stored as an initial value for the period fraction of the internal flash counter. If an external multiturn device is configured (MODE_MT ≠ 00), its data is read in and stored as the initial value for the multiturn data fraction of the internal flash counter.

With **WRITE_CONF** the internal configuration is stored to the EEPROM. The CRC (CRC_E2P) is automatically updated and written to address 0x4E or 0x4F. For a description of the preset routine initiated by **SOFT_PRES** see page 50.

CRC_CHECK starts a CRC verification of the internal configuration RAM. During the check the internal data bus may not be accessed. Should the check not confirm the configuration data as error free, status bit EPR_ERR is set.

Command **TOG_BISS** only causes the communication protocol to switch temporarily (BiSS → SSI, or SSI → BiSS). RAM parameter NBISS is not altered here. The command can be used for SSI encoders to later enable parameterization, for example.

Execution Of Protocol Commands

iC-MN supports selected BiSS C protocol commands:

CMD	Selected address (IDS > 0x00)	Broadcast address (IDS = 0x00)
10	Execute SOFT_PRES	-
11	Execute CRC_CHECK	-

Table 71: Implemented protocol commands

Automatic Reset Function

AUTORES can be used to set whether the command SOFT_RES is automatically generated or not if the error AM_MIN occurs.

AUTORES	Addr. 0x44; bit 1:0
Code	Function
00	No automatic reset
01	SOFT_RES after error AM_MIN, timeout 8 ms
10	SOFT_RES after error AM_MIN, timeout 16 ms
11	SOFT_RES after error AM_MIN, timeout 32 ms

Table 72: Automatic reset function

For as long as the amplitude of the master track is too low or the AM_MIN error is set, SOFT_RES is active. When AM_MIN is no longer set, the timeout configured using AUTORES expires. It is only after this that SOFT_RES is reset and the device subsequently returns to normal operation.

Should an AM_MIN error occur while a command or the preset function is being carried out, SOFT_RES is only implemented once the command has been terminated.

The behavior of the I/O interface with an active SOFT_RES depends on the protocol selected. For **BiSS C** a zero is returned as a data value and the error and warning bits are set; for **SSI** the last data value to be output is repeated (the error bit is set if configured via SSIE). In both cases the error state is indicated at pin NERR by a low signal.

Status Register

The status register is reached by a read access to addresses 0x75 to 0x77. In the event of an error the relevant bit is set and maintained until the status register is read out or the command SOFT_RES is performed (with the exception of status bits EPR_ERR and CMD_EXE). The status register can be accessed independent of the internal state of operation.

STATUS		Addr. 0x75; bit 7:0 R
Bit	Name	Description of status message
7	TH_WRN	Excessive temperature warning
6	EPR_ERR	Configuration error on startup: - No EEPROM (flag EPR_NO set) - Invalid check sum (flag EPR_NV set)
5	FQ_WDR	Excessive signal frequency on master track*: on current readout request
4	FQ_STUP	Excessive signal frequency on master track*: during startup
3	NON_CTR	Period counter consistency error: counted period ↔ calculated Nonius position
2	MT_CTR	Multiturn data consistency error: counted multiturn ↔ external MT data
1	MT_ERR	Multiturn communication error: - Error bit set - CRC error - No start bit - General communication error
0	MT_WRN	Multiturn data indicates warning message (BiSS warning bit set)
	Notes	*) Relevant for nonius synchronization modes (MODE_ST = 0x00 to 0x0B); the warning threshold can be set using parameter FRQ_TH; Error indication logic: 1 = true, 0 = false

Table 73: Status register 0x75

STATUS		Addr. 0x76; bit 7:0 R
Bit	Name	Description of status message
7	ACS_Max	Control error: range at max. limit
6	AM_Min	Signal error: poor level (master track)
5	AM_Max	Signal error: clipping (master track)
4	ACM_Min	Control error: range at min. limit
3	ACM_Max	Control error: range at max. limit
2	CT_ERR	Readout cycle repetition to short*
1	RF_ERR	Excessive SSI clock frequency: conversion data not valid when latching data for output.
0	TH_ERR	Excessive temperature error
	Notes	*) Relevant for nonius synchronization modes MODE_ST = 0x00 to 0x07 (calculation routines must end before a new request is received) Error indication logic: 1 = true, 0 = false

Table 74: Status register 0x76

EPR_ERR indicates that no EEPROM was found on system startup (EPR_NO) or that a CRC error was recognized for the internal setup (EPR_NV). If no EEPROM has been recognized, EPR_ERR remains set even after SOFT_RES.

CMD_CNV and CMD_EXE are signaled on the same status bit and not stored, as opposed to the other status bits. CMD_CNV is set on the initialization of a command which requires the internal converter. CMD_EXE is set on commands which employ the internal data bus.

STATUS		Addr. 0x77; bit 7:0 R
Bit	Name	Description of status message
7	CMD_EXE CMD_CNV	Command execution in progress, or iC-MN in startup phase
6	AN_Min	Signal error: poor level (nonius track)
5	AN_Max	Signal error: clipping (nonius track)
4	ACN_Min	Control error: range at min. limit
3	ACN_Max	Control error: range at max. limit
2	AS_Min	Signal error: poor level (segment track)
1	AS_Max	Signal error: clipping (segment track)
0	ACS_Min	Control error: range at min. limit
	Notes	Error indication logic: 1 = true, 0 = false

Table 75: Status register 0x77

Non-Volatile Diagnosis Memory

By enabling E2EPR all status messages can be stored to the external EEPROM the first time they occur (physical EEPROM addresses 0x75 to 0x77).

On a system startup iC-MN reads in the status messages already stored in the EEPROM. As soon as an error message occurs which has not been noted in the external memory the corresponding status register bit is transfered to the EEPROM. This way a "cumulative" error register is compiled in which all messages are stored which occur during operation. Only the current errors can be read out via the status register (BiSS addresses 0x75 to 0x77).

The cumulative errors which are stored at EEPROM addresses 0x75 to 0x77 can only be read out via BiSS with CFG_E2P > 000 and PROT_E2P = 00 to bank 1, address 0x35-0x37 (see page 52 ff. for memory map).

Note: Once configuration has been completed and before the system is delivered the data at the EEPROM addresses 0x75 to 0x77 should be initialized with zeroes.

E2EPR	Addr. 0x41; bit 7
Code	Description
0	Disabled
1	EEPROM savings of cumulative status messages enabled

Table 76: Diagnosis memory enable

ERROR AND WARNING BIT

For the error and warning bit output the logic is always low active; a logic zero displays an active error or warning message. With the exception of an external system error message (read in via I/O pin NERR and assigned to EXT_ERR) all error codes mentioned in the following are stored in the status register should the corresponding error event occur.

The allocation of error messages to the error and warning bit is either fixed or can be varied with the CFGEW parameter. The following tables explain the fixed and optional visibility.

Fixed Allocation Of Error Messages		
Message	Visibility via error bit	Conditions
EPR_NV* EPR_NO CMD_CNV** CT_ERR	●	None
RF_ERR	●	Visible when NBISS = 1
MT_ERR MT_CTR	●	Visible when MODE_MT = 01, 10
NON_CTR FQ_STUP	●	Visible when MODE_ST set for nonius synch.
Notes	*) Reset by command SOFT_RES **) CMD_CNV is also visible for warning bit.	

Table 77: Fixed allocation of messages for error bit indication

Variable Allocation Of Error Messages		
Message	Visibility via error bit	Visibility via warning bit
MT_WRN	n/a	○
TH_WRN	n/a	○
FQ_WDR	n/a	○
ACx_MAX	n/a	○
ACx_MIN	n/a	○
Ax_MAX	○	○
Ax_MIN	○	○
TH_ERR	○	n/a
EXT_ERR	○	n/a
Notes	○ = configurable via CFGEW x = M, S, N	

Table 78: Variable allocation of error messages for error/warning bit indication

EXT_ERR can only be configured to the error bit and is not latched by the status register. It permits iC-MN to signal an error state of further ICs to the PLC, when the messaging IC pulls down the NERR pin. With devices featuring open-drain alarm outputs a wired-or bus logic can be installed.

EXT_ERR	
Code	Description
0	No external error
1	External component indicating an error to pin NERR

Table 79: External error message

CFGEW	Adr 0x42, bit(7:0)
Bit	**Visibility for error bit**
7	Ax_MAX, Ax_MIN
6	EXT_ERR
5	TH_ERR
	Enables additional functions, please refer to the description given below.
Bit	**Visibility for warning bit**
4	FQ_WDR
3	Ax_MAX and Ax_MIN
2	ACx_MAX and ACx_MIN
1	TH_WRN
0	MT_WRN
Notes	x = M, S, N Encoding of bit 7...0: 0 = message enabled, 1 = message disabled

Table 80: Error and warning bit configuration

The visibility of the temperature error can be configured on the error bit by CFGEW(5) = 0. The occurrence of a temperature error then causes:

1. The setpoint of the signal level controller to be reduced to the lowest setting
2. The analog output voltages to switch to VDD/2 at outputs PSOUT, NSOUT, PCOUT and NCOUT
3. The RS422 output driving capability to be limited to 20 mA.

The following must also be taken into account:

- Error messages which are signaled via the error bit of the serial I/O interface are also indicated by a low signal at the NERR pin
- Nonius synchronization errors (NON_CTR) are indicated directly at the NERR pin

- Temperature and signal level errors are indicated directly at the NERR pin. These errors are only signaled via the error bit if they are active at the point when data is accepted into the output shift register.

All errors which occur during operation are stored in the status register regardless of the configuration of the error/warning bit (see page 43).

Visibility Of Latched Status Messages

Parameter S2WRN enables status messages configured to the warning bit using CFGEW and stored in the status register to be output to the warning bit. In this instance the warning bit is set until the relevant status register is read out. Parallel to S2WRN the behavior of the error bit and the NERR pin can be influenced by S2ERR.

S2WRN	Addr. 0x43; bit 2
Code	Visibility for warning bit
0	Current messages configured to the warning bit
1	As above, or-gated with latched status messages which are configured to the warning bit

Table 81: Visibility for warning bit

S2ERR	Addr. 0x43; bit 3
Code	Visibility for error bit and NERR
0	Current messages configured to the error bit
1	As above, or-gated with latched status messages which are configured to the error bit

Table 82: Visibility for error bit (and NERR pin)

MT INTERFACE

In nonius modes iC-MN can connect to an external multiturn sensor via the serial MT interface. Following synchronization of the MT data with the ST data the multiturn period counter is set to its initial position. Each further revolution is then logged by the internal period counter.

Even when the MT interface is not employed, the internal 24-bit multiturn period counter can be configured to complement singleturn position data output by a counted multiturn position (see M2S).

Additionally, the MT interface can be configured as a parallel two-pin interface to read in a single bit multiturn position accompanied by a synchronization bit. In this way coverage of the absolute singleturn position can be doubled if additional sensors provide 180 and 90 degree sector information.

MODE_MT	Addr. 0x40; bit 4:3
Code	Function
00*	Multiturn position counted internally
10*	Serial MT interface active (SSI)
11*	Parallel MT interface active (2-bit mode): Pin MTMA is input for 180° and pin MTSLI input for 90° sector information
Notes	*) NCRC_MT = 0 required If MODE_MT is altered during operation, command SOFT_RES must be issued (see page 42).

Table 83: MT Interface operation mode

Configuration Of Data Lengths

The bit length of the internal MT counter and of the multiturn data word is set using parameter DL_MT. For synchronization purposes the synchronization bit length must be set by SBL_MT. Synchronization occurs between the external multiturn data read in and the period information counted internally. At synchronization bit lengths > 1 bit synchronization can occur automatically within the relevant phase tolerances.

With a single synchronization bit (SBL_MT = 00) no automatic synchronization can take place. Here, iC-MN cannot recognize whether the external multiturn sensor provides leading or trailing position data (what may vary depending on gear box assembly). This must be set manually by parameter LNT_MT.

Figure 19 shows the principle of MT synchronization for ideal signals (without indication of synchronization tolerance limits). It shows 2 bit and 1 bit synchronization for leading and trailing signals.

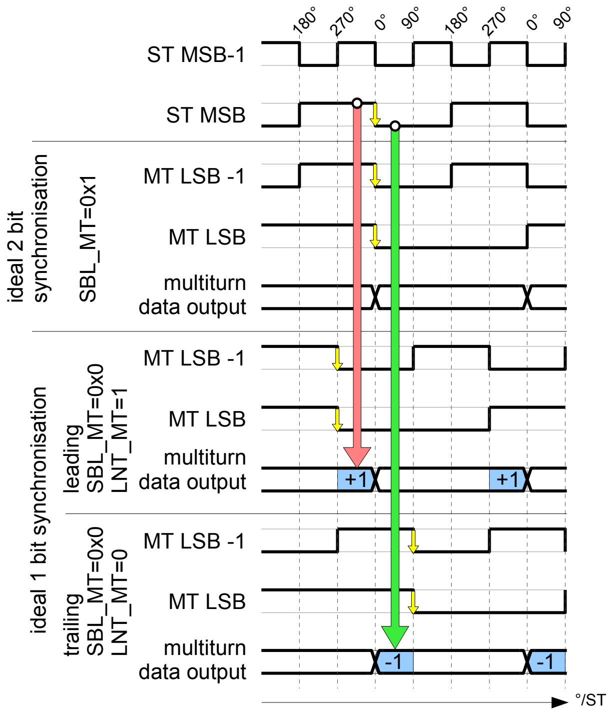


Figure 19: Principle of MT synchronization for 1 bit and 2 bit synchronization signals

With a synchronization bit length of two or more bits iC-MN ignores parameter LNT_MT selecting for leading or trailing MT data. Synchronization bit lengths of 3 bit or 4 bit enlarge further the synchronization tolerance between multiturn and singleturn (see Table 85).

DL_MT	Addr. 0x3E; bit 7:5
Code	Multiturn bit count*
0x00	8
...	...
0x0C	20
0x0D	24
0x0E	1
0x0F	4
Notes	*) Does not include synchronization bits of the external MT sensor.

Table 84: MT data length (and counter depth)

SBL_MT	Addr. 0x41; bit 1:0	
Code	MT synchronization bit length	Synchronization range (ST resolution)
00	1 bit	±90°
01	2 bit	±90°
10	3 bit	±135°
11	4 bit	±157.5°

Table 85: MT synchronization bit length

LNT_MT	Addr. 0x41; bit 2
Code	Function (single sync. bit, SBL_MT = 0x00)
0	Trailing
1	Leading

Table 86: Leading/trailing gear box assembly

Via CHK_MT the device can be configured so that the counted multiturn period is verified every 8 ms. An error in the multiturn check (the comparison of the counted multiturn period and the external multiturn position data) is signaled via the error bit (MT_CTR is set in the status register, see page 43).

CHK_MT	Addr. 0x40; bit 6
Code	Function
0	Verification disabled
1	Cyclic verification each 8 ms

Table 87: Period counter verification

GRAY_MT	Addr. 0x41; bit 3
Code	Data format
0	Binary coded
1	Gray coded

Table 88: MT Interface data format

Error Handling

If a communication error appears when reading in external multiturn data during the **startup phase** (such as pin MTSLI reading a permanent logic 0 or the external MT sensor not responding), the first conversion and request for the external multiturn data are repeated up to three times (see Figure 20). If the error persists after a fourth attempted readin, the device goes into normal operating mode. Conversion requests for the single-turn position data are possible, but MT_ERR remains permanently set.

The error handling in **normal operating mode** when the multiturn data verification is activated is shown in Figure 21. If there is an error in communication no further readouts are attempted and MT_ERR remains permanently set.

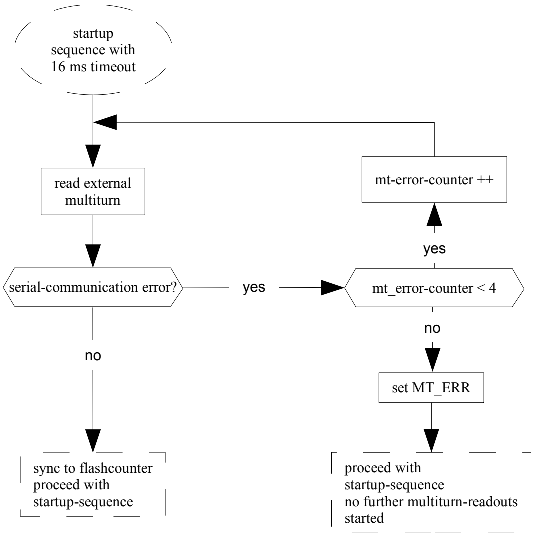


Figure 20: Error handling during start up phase

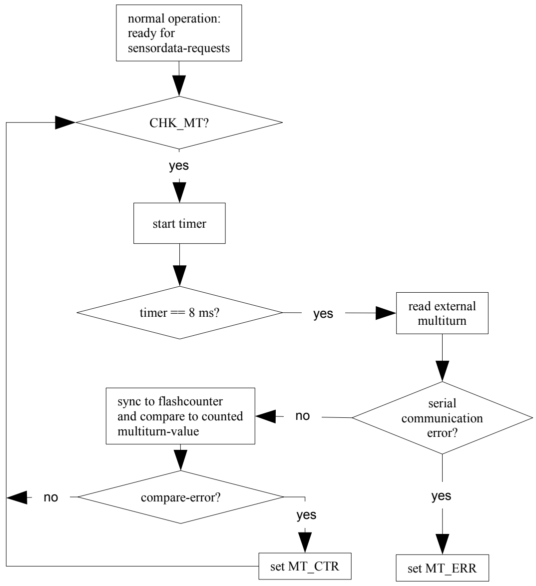


Figure 21: Error handling during normal operation with cyclic period counter verification

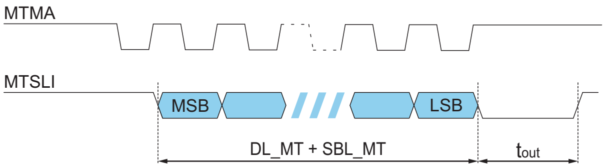


Figure 22: Line signals of the serial MT interface MODE_MT = 0x10 (SSI)

MT Interface with 2-bit mode

In this mode pin MTMA functions as an additional input, besides pin MTSLI. The inputs now expect digital signals phase shifted by 90°, whereas MTMA reads the single bit period information, and MTSLI the shifted synchronization bit. The following figure explains the principle and the table below gives the necessary settings.

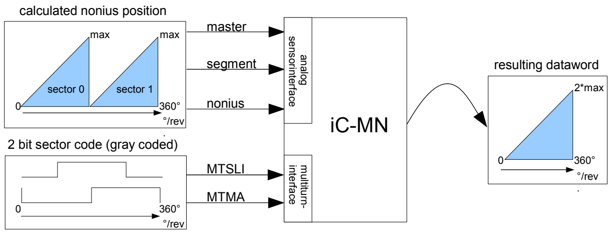


Figure 23: Principle of 2-bit mode

Parameter	Description
MODE_MT = 11	MT interface op. mode: 2-bit mode
DL_MT = 0x0E	MT data length: 1 bit
SBL_MT = 00	Synchronization bit length: 1 bit
LNT_MT = 0 or 1	Depending on MTMA signal: leading or trailing
GRAY_MT = 1	MT data format: Gray coded
M2S = 11	Enable for MT plus ST data output

Table 89: Required settings for 2-bit mode

The required position of the multiturn and synchronization bit depends on parameter LNT_MT. Figure 24 shows the required signal positions with leading respectively trailing operation. The green arrows are indicating the permissible relative position tolerances.

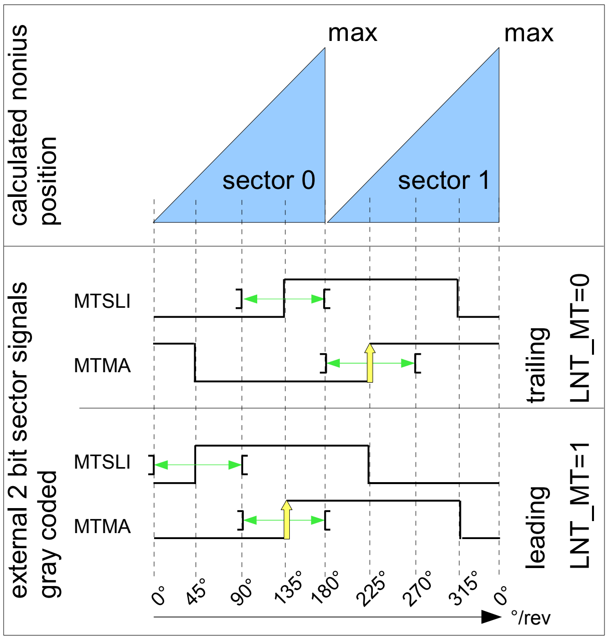


Figure 24: Position of switch points in reference to the parameter LNT_MT

A typical application example where the 2-bit mode can be used for, is a magnetic angle encoder scanning the pole wheel by MR sensors. A nonius coded wheel of 16, 15 and 12 pole pairs yields 32, 30 and 24 sine periods per turn on iC-MN's analog inputs. The nonius calculation would not produce absolute angle position data over a single revolution since the maximum singleturn value is achieved twice. The distinction as to which half of the revolution the axis is in can only be made using section sensors, two Hall sensors for example, whose digital outputs are connected up directly to MTMA and MTSLI. Furthermore, the 2-bit mode can be used also with systems based on a 2 track nonius calculation.

MT INTERFACE with EXTENDED FUNCTIONS

The serial multiturn interface can be operated in the BiSS C protocol which enables multiturn sensor error messages to be evaluated (via the error and warning bits, each of which are low active) and communication to be monitored (evaluation of the CRC bits, see Figure 25).

The error behavior of the multiturn interface has already been described in Figures 20 and 21; only a set error bit (low) or a CRC error are now also classified as a communication error.

MODE_MT	Addr. 0x40; bit 4:3
Code	Function
00	Internal multiturn period counting
01	BiSS C protocol
Notes	If MODE_MT is altered during operation, command SOFT_RES must be issued (see page 42).

Table 90: MT Interface operation mode

SWC_MT	Addr. 0x41; bit 6
Code	CRC polynomial (HEX)
0	0x43
1	0x25

Table 91: MT Interface CRC polynomial

NCRC_MT	Addr. 0x41; bit 4
Code	Function
0*	CRC verification active
1	Disabled
Note	*) Only permitted with MODE_MT = 01.

Table 92: MT Interface CRC verification

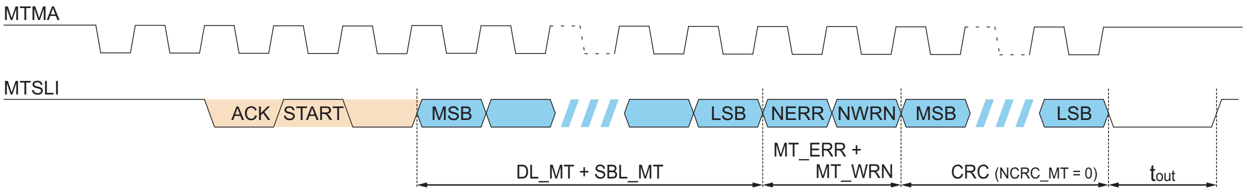


Figure 25: Example of the MT interface line signals with BiSS C protocol

Direct Communication To Multiturn Sensor
Making use of the BiSS Interface bus capabilities, iC-MN can connect the external multiturn sensor to the BiSS master controller when GET_MT is enabled. To this end pin MA receiving the BiSS master's clock signal is fed through to pin MTMA and the MTSLI pin is activated in place of the SLI pin. Upon enabling this mode the singlecycle timeout must have elapsed and an additional init command carried out by the BiSS master, before it can run the first register communication.

Example: external multiturn sensor built with iC-MN is connected to the MT interface of a first iC-MN, preparing the singleturn data. With GET_MT enabled, the external multiturn can then be addressed via BiSS ID 0 and the singleturn via BiSS ID 1. This temporal chain operation eases device parameterization during encoder manufacturing.

GET_MT	Addr. 0x41; bit 5
Code	Function
0	Disabled
1	MT sensor communication enabled

Table 93: Direct BiSS communication enable for MT sensor via I/O Interface

PRESET FUNCTION

The preset function sets the output position data to a predefined position value and is initiated by a high flank at pin PRES or by calling the SOFT_PRES command (writing 0x02 to the command register, see Table 70). If an external EEPROM is available the preset values are read in from the preset registers. A preset value of zero is otherwise assumed. The current position is determined. Correction factors for the output (OFFS_ST, OFFS_MT) are calculated and stored in the internal RAM. With an EEPROM available the entire contents of the RAM are written to said EEPROM, thus storing the OFFS_ST and OFFS_MT data.

Note: Command SOFT_PRES blocks iC-MN's internal RAM for accesses over a certain time.

For the output the OFFS_ST and OFFS_MT values are subtracted from the internal synchronized result with each conversion (Note: In MODE_ST = 0x05-0x07 and 0x0D the sensor data is designated faulty after the first readout. The readout data is equivalent to the correction factor.)

OFFS_ST	Addr. 0x34; bit 6:0 Addr. 0x33; bit 7:0 Addr. 0x32; bit 7:0 Addr. 0x31; bit 7:0 Addr. 0x30; bit 7:0
0x00000 . . . 0x7FFFF	Singleturn output offset

Table 94: Position offset for ST data output

PRES_ST	Addr. 0x54; bit 6:0 Addr. 0x53; bit 7:0 Addr. 0x52; bit 7:0 Addr. 0x51; bit 7:0 Addr. 0x50; bit 7:0
0x00000 . . . 0x7FFFF	Preset register singleturn (EEPROM only, see text)

Table 95: Preset value for ST data output

The position of the preset value for the singleturn data word (ST_DW) in preset register PRES_ST varies depending on the converter mode (MODE_ST see Table 42). For nonius synchronization operating mode see Figure 26; see Figure 27 for multiturn synchronization operating mode.

In the PRES_MT register the multiturn preset values are always justified to the right with the LSB (starting at address 0x55, bit 0).

OFFS_MT	Addr. 0x37; bit 7:0 Addr. 0x36; bit 7:0 Addr. 0x35; bit 7:0
0x000 . . . 0xFFF	Multiturn output offset

Table 96: Position offset for MT data output

PRES_MT	Addr. 0x57; bit 7:0 Addr. 0x56; bit 7:0 Addr. 0x55; bit 7:0
0x000 . . . 0xFFF	Preset register multiturn (EEPROM only)

Table 97: Preset value for MT data output

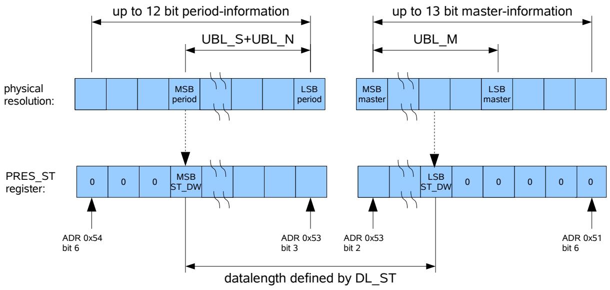


Figure 26: PRES_ST with nonius synchronization mode

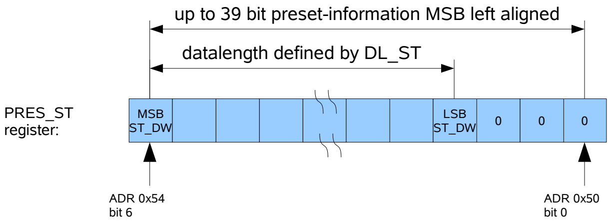


Figure 27: PRES_ST with multiturn synchronization mode

STARTUP BEHAVIOR

Figure 28 shows the startup behavior of iC-MN. After turning on the power supply (power-on reset) iC-MN reads the configuration data from the EEPROM. If the data can be read without error, a timeout of 8 ms is allowed to elapse.

If the multiturn interface has been configured for an external sensor, the device waits for a longer timeout of 16 ms to elapse. The multiturn data is then read in and the first conversion performed in order to determine the absolute position (see page 47). iC-MN then goes into normal operation.

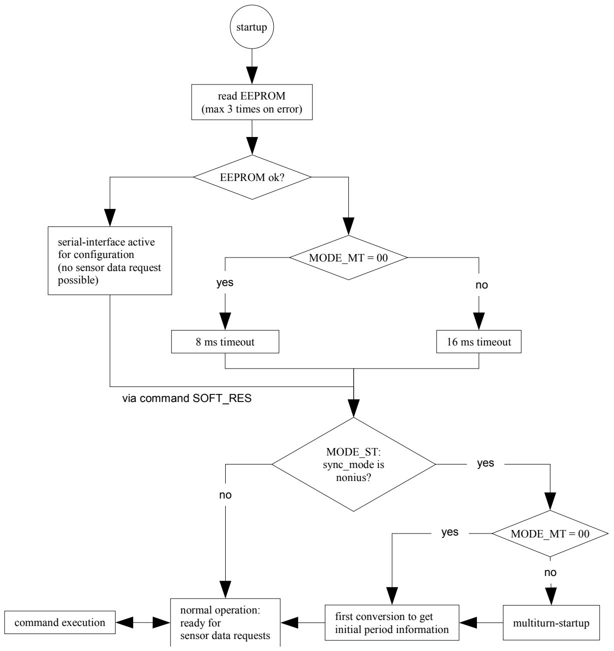


Figure 28: Startup behavior

If an error occurs while the EEPROM data is being read (a CRC error or communication error with the EEPROM), the current readin process is canceled and restarted. Following a third failed attempt the readin procedure is ended and the internal iC-MN configuration registers (addresses 0x00 to 0x4D) initialized with a zero.

In doing so, NBISS = 0 selects for the BiSS C protocol for the I/O interface enabling BiSS C register communication.

If an attempt to read sensor data is made iC-MN would reply an 8-bit zero value with set error and warning bits (sequence: start bit 1x high, position 8x zero, error/warning 2x zero, CRC 6x high followed by zero bits when the clock signal is continued).

Following successful configuration using the I/O interface command SOFT_RES must be issued in order to switch iC-MN to normal operation (see page 42).

EEPROM INTERFACE

The serial EEPROM interface consists of the two pins SCL and SDA and enables read and write access to a serial EEPROM (such as a 24C02 with 128 bytes, 5 V type with a 3.3 V function). The data in the EEPROM is secured by a CRC to the addresses 0x4E and 0x4F.

Application Hints

To protect the EEPROM against a reversed power supply voltage it can be connected to the integrated supply switch (pins VDDA and GNDA). The EEPROM specifications and absolute maximum ratings should comply to the pin voltages of VDDA, SCL and SDA during startup and operation. A protective circuit may be advisable depending on the EEPROM model.

For EEPROM selection the following minimal requirements must be fulfilled: (e. g. Atmel AT24C01B, 128x8)

- Operation from 3.3 V to 5 V, I^2C-Interface
- Minimal 1024 bit, 128x8

CRC_E2P(1:0) **CRC_E2P(9:2)**	Addr. 0x4F; bit 7:6 Addr. 0x4E; bit 7:0
Code	Description
0x000 ... 0x3FF	CRC formed by CRC polynomial 0x409

Table 98: EEPROM Data Check Sum

Memory Map And Register Access

Depending on the EEPROM size different bank assignments can be configured using CFG_E2P. There are three areas, placed one after the other, which are designated for this purpose in the memory:

1. CONF: iC-MN configuration data
2. EDS : **E**lectronic **D**ata **S**heet
3. USER: OEM data, free user area

CFG_E2P		Adr 0x40; Bit 2:0			
		Banks per area (64 bytes each)			
Code	Bytes	CONF	EDS	USER	EEPROM, Typ
For SSI applications:					
000*	128	2	-	-	1 kbit, C01 up
001	256	3	1	-	2 kbit, C02 up
For BiSS applications with EDS:					
010	512	3	4	1	4 kbit, C04 up
011	1024	3	4	9	8 kbit, C08 up
100	1024	3	12	1	8 kbit, C08 up
101	2048	3	4	25	16 kbit, C016 up
110	2048	3	12	17	16 kbit, C016 up
111	2048	3	24	5	16 kbit, C016 up
Notes	*) direct addressing mode				

Table 99: Configuration of external memory

Direct Addressing

The registers can be accessed via the I/O interface and direct addressing (for CFG_E2P = 000). In accordance with the BiSS protocol the number of bytes addressed is restricted to 128. Accessing addresses 0x00 to 0x4F reads or writes to iC-MN's internal RAM register. The data from this special address area can only be transmitted to the EEPROM by the command WRITE_CONF.

The registers for addresses 0x50 to 0x70, 0x78 to 0x7B and 0x7D to 0x7F are in the EEPROM and can be accessed byte-wise by a BiSS register access for read or write.

The addresses missing in the above are located in iC-MN: the status register from 0x75 to 0x77 (read only), the MN_CMD register at 0x77 (write only), and the I/O interface parameters CID_SCD and TOS at address 0x7C. The latter has no access limitations and can always be read and written to (content is mirrored to 0x4C).

Bank-Wise Addressing

iC-MN also supports bank-wise addressing (for CFG_E2P $\neq$ 000) according to the *BiSS Interface C Protocol Description*. In this mode of configuration iC-MN divides the internal address sections into banks of 64 bytes each. The address sections visible via the I/O interface recognizes a "dynamic" section (addresses 0x00 to 0x3F) and a "static" section which is permanently visible (addresses 0x40 to 0x7F). The static address section is always independent of the bank currently selected. Figure 29 illustrates how the banks selected by BANKSEL are addressed.

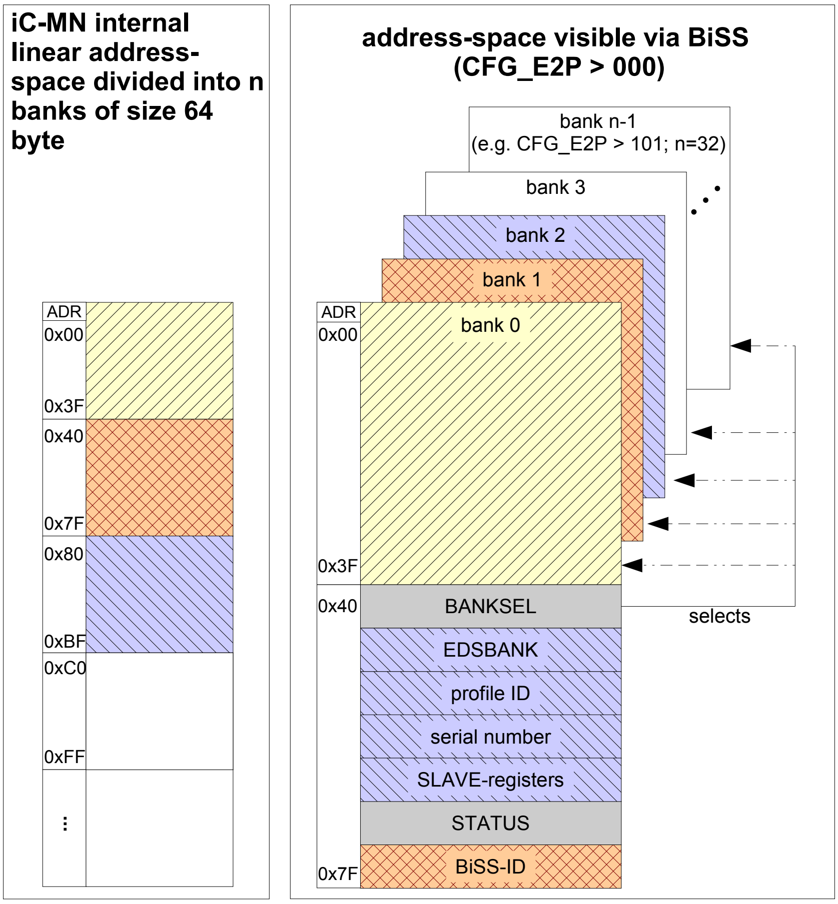


Figure 29: Principle of bank-wise memory addressing

Register access can be restricted via PROT_E2P (see Table 100). PROT_E2P = 10 selects safety level 2, a shipping mode with limited access. Shipping 2 can be set back to level 1 (shipping 1), for which purpose the content of address 0x43 must be written anew.

PROT_E2P(1:0)	Addr. 0x43; bit 1:0	
Code	Mode	Access Limitation (see Figure 30 and 31)
00	Configuration Mode, free access	RP0
01	Configuration Mode, limited access	RP1
10	Shipping Mode 1, reset to RP1 is possible	RP2
11	Shipping Mode 2, reset is not possible	RP2

Table 100: Register Access Control

Sections CONF, EDS and USER are protected at different levels in shipping mode for read and write access.

PROT_E2P(1:0)	Addr. 0x43; bit 1:0		
	Range		
RPL*	CONF	EDS	USER
RP0	r/w	r/w	r/w
RP1	STATUS n/a r/w for others	r/w	r/w
RP2	n/a	r only	r/w
Note	* Register Protection Level		

Table 101: Register Read/Write Protection Levels (n/a: iC-MN refuses access to those register addresses.)

Figure 30 shows the static memory area and Figure 31 the area which can be altered by BANKSEL. The BiSS register access limitations which are generated by parameter PROT_E2P are marked ”R/W” for read/write access and ”R” for read only. The original site of data returned by access to the BiSS register is designated by ”RAM” for iC-MN’s internal RAM, by ”E2P” for the EEPROM and by ”INT” for those of iC-MN’s internal registers which cannot be preloaded on startup.

static part: BiSS addresses 0x3F-0x7F

addressing scheme				register-protection-level		data
bank	**address**	**content**	**mapped to address**	**RP1**	**RP2**	**location**
0-31	0x40	BANKSEL	internal	R/W	R/W	INT
	0x41	EDSBANK	0x081		R	E2P
	0x42	profile ID	0x082			
	0x43		0x083			
	0x44	serial number	0x084			
	⋮		⋮			
	0x47		0x087			
	0x48	SLAVE-registers	0x088			
	⋮		⋮			
	0x6F		0x0AF			
	0x70	reserved	0x0B0			
	⋮		⋮			
	0x74		0x0B4			
	0x75	STATUS	internal		R/W	INT
	0x76	STATUS				
	0x77	STATUS/MN_CMD				
	0x78	BISS-ID	0x078		R	E2P
	⋮		⋮			
	0x7C		0x04C		R/W	RAM
	⋮		⋮		R	E2P
	0x7F		0x07F			

Figure 30: User view: BiSS memory access 0x40 to 0x7F, content independent of BANKSEL; CFG_E2P ≠ 000

bank switched part: BiSS addresses 0x00-0x3F

addressing scheme				register-protection-level		data
bank	**address**	**content**	**mapped to address**	**RP1**	**RP2**	**location**
0	0x00	parameter values with CRC	0x000	R/W	n/a	RAM
	⋮		⋮			
	0x3F		0x03F			
1	0x00		0x040			
	⋮		⋮			
	0x0C		0x04C		R/W	
	⋮		⋮		n/a	
	0x0F		0x04F			
	0x10	preset-values	0x050		R/W	E2P
	⋮		⋮			
	0x17		0x057			
	⋮	free	⋮		n/a	
	0x35	STATUS accumulated (see E2EPR for details)	0x075	n/a		
	0x36		0x076			
	0x37		0x077			
	0x38	BiSS-ID	0x078	R/W	R	
	⋮		⋮			
	0x3C		0x04C		R/W	RAM
	⋮		⋮		R	E2P
	0x3F		0x07F			
2	0x00	reserved	0x080			
	0x01	EDSBANK, profile ID, serial number, SLAVE-registers	0x081			
	⋮		⋮			
	0x2F		0x0AF			
	0x30	reserved	0x0B0			
	⋮		⋮			
	0x3F		0x0BF			
3	0x00		0x0C0		R or R/W	
	⋮		⋮			
	0x3F		0x0FF			
⋮	⋮	⋮	⋮			
31	0x00		0x7C0			
	⋮		⋮			
	0x3F		0x7FF			

Figure 31: User view: BiSS memory access 0x00 to 0x3F, content switchable with BANKSEL; CFG_E2P ≠ 000

APPLICATION NOTES: Configuration As BiSS C-Slave Including EDS (Electronic Data Sheet)

Preconditions:

1. CFG_E2P <> b000. The bank switch function must be activated.

2. EDSBANK = 0x03. No other values possible. Addressing via BiSS: Bank: 2, Adr: 0x01 or direct to EEPROM: Adr: 0x081

3. Setting of profile ID according to the following tables; Addressing via BiSS: Bank: 2, Adr: 0x02-0x03 or direct to EEPROM: Adr: 0x082-0x083

BiSS Profile	0-12	
MODE_ST	0x00-0x0B (Nonius)	0x0C-0x0F (Multiturn)
NBISS	0	
ELC	0	
GRAY_SCD	0	
DL_ST	0x04 (12)	
DL_MT	-	
M2S	0x00	
R_MT	0x00 (0)	
R_ST	UBL_M+UBL_S+UBL_N	
SBL_x	≠0x00	-
Notes	UBL_M+UBL_S+UBL_N ≤ 12	

Table 102: Setup for BiSS profile 0-12

BiSS Profile	0-24	
MODE_ST	0x00-0x0B (Nonius)	0x0C-0x0F (Multiturn)
NBISS	0	
ELC	0	
GRAY_SCD	0	
DL_ST	0x10 (24)	
DL_MT	-	
M2S	0x00	
R_MT	0x00 (0)	
R_ST	UBL_M+UBL_S+UBL_N	
SBL_x	≠0x00	
Notes	UBL_M+UBL_S+UBL_N ≤ 24	

Table 103: Setup for BiSS profile 0-24

BiSS Profile	0-24++	
MODE_ST	0x00-0x0B (Nonius)	0x0C-0x0F (Multiturn)
NBISS	0	
ELC	0	
GRAY_SCD	0	
DL_ST	0x11(25)	> 0x10 (24) < 0x18 (32)
DL_MT	-	
M2S	0x00	
R_MT	0x00 (0)	
R_ST	0x19 (25)	UBL_M+UBL_S+UBL_N
SBL_x	≠0x00	
Notes	UBL_M=13, UBL_S=6, UBL_N=6	UBL_M+UBL_S+UBL_N = DL_ST; UBL_M+UBL_S+UBL_N > 24

Table 104: Setup for BiSS profile 0-24++

BiSS Profile	12-12
MODE_ST	0x00-0x0B (Nonius)
NBISS	0
ELC	0
GRAY_SCD	0
DL_ST	0x04 (12)
DL_MT	0x04 (12)
M2S	0x03
R_MT	0x0C (12)
R_ST	UBL_M+UBL_S+UBL_N
SBL_x	≠0x00
Notes	UBL_M+UBL_S+UBL_N ≤ 12

Table 105: Setup for BiSS profile 12-12

BiSS Profile	12-24
MODE_ST	0x00-0x0B (Nonius)
NBISS	0
ELC	0
GRAY_SCD	0
DL_ST	0x10 (24)
DL_MT	0x04 (12)
M2S	0x03
R_MT	0x0C (12)
R_ST	UBL_M+UBL_S+UBL_N
SBL_x	≠0x00
Notes	UBL_M+UBL_S+UBL_N ≤ 24

Table 106: Setup for BiSS profile 12-24

BiSS Profile	12-24++
MODE_ST	0x00-0x0B (Nonius)
NBISS	0
ELC	0
GRAY_SCD	0
DL_ST	0x11(25)
DL_MT	0x04 (12)
M2S	0x03
R_MT	0x0C (12)
R_ST	0x19 (25)
SBL_x	≠0x00
Notes	UBL_M=13, UBL_S=6, UBL_N=6

Table 107: Setup for BiSS profile 12-24++

BiSS Profile	24-12
MODE_ST	0x00-0x0B (Nonius)
NBISS	0
ELC	0
GRAY_SCD	0
DL_ST	0x04 (12)
DL_MT	0x0D (24)
M2S	0x03
R_MT	0x18 (24)
R_ST	UBL_M+UBL_S+UBL_N
SBL_x	≠0x00
Notes	UBL_M+UBL_S+UBL_N ≤ 12

Table 108: Setup for BiSS profile 24-12

BiSS Profile	24-24
MODE_ST	0x00-0x0B (Nonius)
NBISS	0
ELC	0
GRAY_SCD	0
DL_ST	0x10 (24)
DL_MT	0x0D (24)
M2S	0x03
R_MT	0x18 (24)
R_ST	UBL_M+UBL_S+UBL_N
SBL_x	$\neq$ 0x00
Notes	UBL_M+UBL_S+UBL_N $\leq$ 24

Table 109: Setup for BiSS profile 24-24

BiSS Profile	24-24++
MODE_ST	0x00-0x0B (Nonius)
NBISS	0
ELC	0
GRAY_SCD	0
DL_ST	0x11(25)
DL_MT	0x0D (24)
M2S	0x03
R_MT	0x18 (24)
R_ST	0x19 (25)
SBL_x	$\neq$ 0x00
Notes	UBL_M=13, UBL_S=6, UBL_N=6

Table 110: Setup for BiSS profile 24-24++

Remarks to iC-MN with EDS:

1. CFG_E2P $\neq$ b000 (i.e. bank switch function has been activated.)
2. EDSBANK must be set 0x03 (no other values are possible)
   Addressing via BiSS: Bank: 2, Adr: 0x01
   or direct to EEPROM: Adr: 0x081
3. Set profile ID.
   Addressierung via BiSS: Bank: 2, Adr: 0x02-0x03
   or direct to EEPROM: Adr: 0x082-0x083

APPLICATION NOTES: PLC Operation

PLC Operation

There are PLCs with a remote sense supply which require longer for the voltage regulation to settle. At the same time the PLC inputs can have high-impedance resistances versus an internal, negative supply voltage which define the input potential for open inputs.

In this instance iC-MN's reverse polarity protection feature can be activated as the outputs are tristate during the start phase and the resistances in the PLC determine the pin potential. During the start phase neither the supply VDD nor the output pins, which are also monitored, must fall to below ground potential (pin GND); otherwise the device is not configured and the outputs remain permanently set to tristate.

In order to ensure that iC-MN starts with the PLCs mentioned above pull-up resistors can be used in the encoder. Values of 100 kΩ are usually sufficient; it is, however, recommended that PLC specifications be specifically referred to here.

DESIGN REVIEW: Notes On Chip Functions

iC-MN Y2		
No.	Function, Parameter/Code	Description and Application Hints
		No exclusions known at time of printing.

Table 111: Notes on chip functions regarding iC-MN chip releas Y2

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We understand suitable application of our published designs to be state-of-the-art technology which can no longer be classed as inventive under the stipulations of patent law. Our explicit application notes are to be treated only as mere examples of the many possible and extremely advantageous uses our products can be put to.

ORDERING INFORMATION

Type	Package	Order Designation
iC-MN	48-pin QFN 7x7 mm	iC-MN QFN48
Evaluation Board	Size 140mm x 100mm	iC-MN EVAL MN1D

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH	**Tel.: +49 (61 35) 92 92-0**
Am Kuemmerling 18	**Fax: +49 (61 35) 92 92-192**
D-55294 Bodenheim	**Web: http://www.ichaus.com**
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