iC-MD 48-BIT QUADRATURE COUNTER WITH RS422 RECEIVER AND SPI/BISS INTERFACE

preliminary

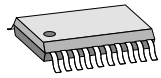
FEATURES

- Configurable quadrature 3-channel binary counter of 16, 24, 32 and 48 bit (TTL, RS422 or LVDS input)
- Fast RS422 12 V receiver for differential A/B/Z encoder signal
- Count frequency to 40 MHz
- Monitoring of A/B phase logic with error message
- Evaluation of distance-coded reference marks
- Pin-triggered touch-probe function with selectable hi/lo edge sensitivity
- Error and warning signal generation
- Operation from 3.3 V to 5 V
- Configuration via bus capable SPI and BiSS C Interface
- Two actuator output signals
- Default operation mode permits plug & play without programming
- 3 Channel 16 bit counting (TTL: A/B)
- 2 Channel 16, 24 or 16+32 bit counting (TTL: AP/AN/BP, BN/CP/CN)
- 1 Channel 16, 24, 32 or 48 bit counting (TTL: AP/AN/BP or RS422, LVDS: AP,AN/BP,BN/CP,CN differential)

APPLICATIONS

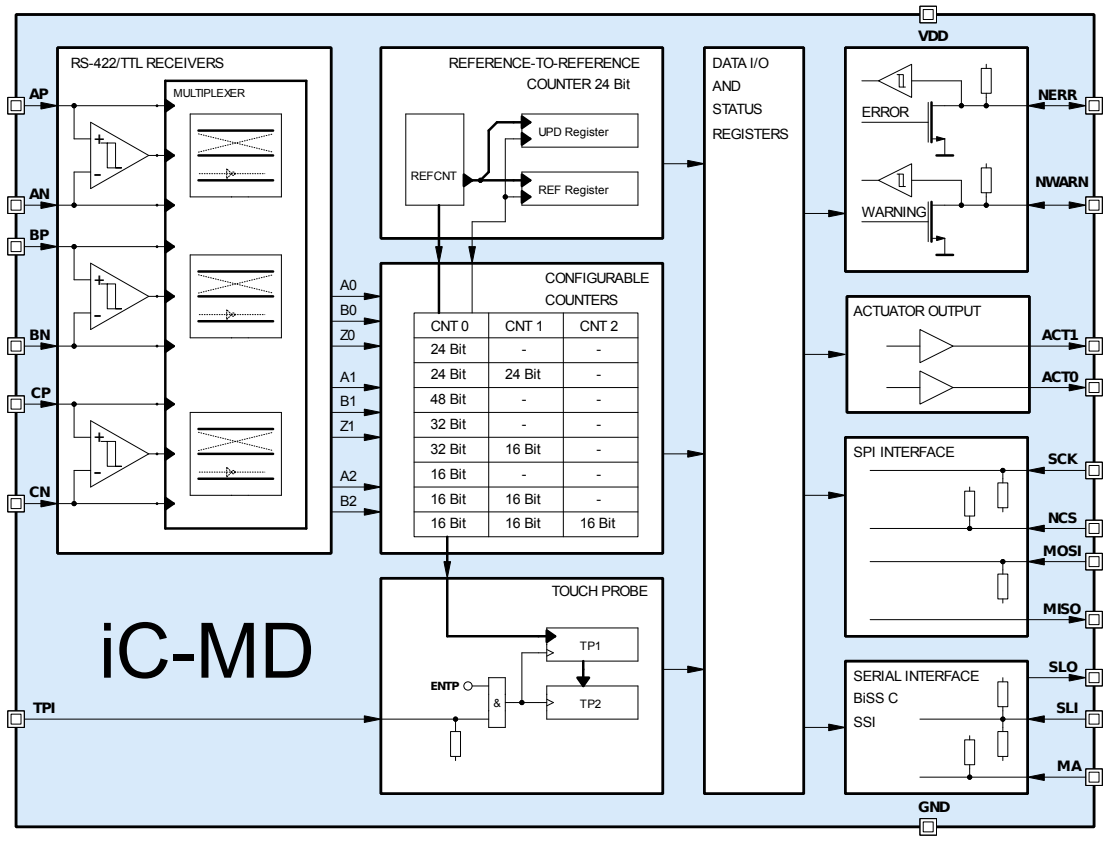
- PLC interface to linear scales, rotary encoders, digital gauges
- Motion control

PACKAGES



TSSOP 20

BLOCK DIAGRAM



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DESCRIPTION

iC-MD evaluates incremental encoder signals with A, B and index tracks from up to three encoders.

After power-on the iC-MD has all the RAM bits at 0 as default configuration, that means one 24 bit counter is configured with RS422 differential inputs. The encoder signals A+/A- are connected to AP,AN, B+/B- to BP,BN and Z+/Z- to CP,CN. The device can be programmed via the SPI interface or BiSS Interface.

The 48 bit counter can be configured as up to three counters with variable counter depths of 16, 24, 32 or 48 bits, but the sum of bits of all the configured counters can not be higher than 48 bits. Some of the possible configurations are 1x48 bit, 2x24 bit, 3x16 bit, 1x32 + 1x16 bit. Each edge of the synchronized encoder signal counts (fourfold edge evaluation).

An additional 24bit counter REF counter is used to store the distance (number of pulses) between the first two index pulses after power-on and the distance between every last two index pulses in UPD register.

An event at the input pin TPI (configurable as rising, falling or both edges) loads the register TP1 with the actual value of the counter 0, and shift the old value of TP1 in register TP2. This registers can also be loads through the instruction bit TP, via SPI or BiSS (Register communication).

Two bidirectional ports are used as error and warning output (low active) and can be pulled down from outside to signals an external error or external warning. This external error and warning are internally latched in the status registers.

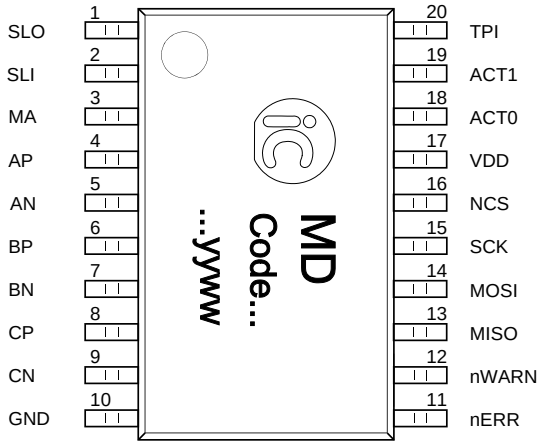
A set of status registers monitor the status of the counter, TP1, TP2, REF, UPD, power on and external error and warning pins.

The BiSS Interface uses the BiSS C protocol and reads out the counter and registers TP1, TP2 and UPD as Sensor data. REF register is read via BiSS C register communication.

The device described here is a multifunctional iC that contains integrated BiSS C interface components. The BiSS C process is protected by patent DE 10310622 B4 owned by iC-Haus GmbH and its application requires the conclusion of a license (free of charge).
Download the license at
www.biss-interface.com/bua

PACKAGING INFORMATION

PIN CONFIGURATION
TSSOP20 4.4 mm, lead pitch 0.65 mm



PIN FUNCTIONS

No.	Name	Function
1	SLO	BiSS/SSI Interface, data output
2	SLI	BiSS/SSI Interface, data input
3	MA	BiSS/SSI Interface, clock input
4	AP	Signal Input (CNT0)
5	AN	Signal Input (CNT0)
6	BP	Signal Input (CNT0/CNT1)
7	BN	Signal Input (CNT0/CNT1)
8	CP	Signal Input (CNT0/CNT1/CNT2)
9	CN	Signal Input (CNT0/CNT1/CNT2)
10	GND	Ground
11	NERR	Error Message Output (low active) / System Error Message Input
12	NWARN	Warning Message Output (low active) / System Warning Message Input
13	MISO	SPI Interface, data output
14	MOSI	SPI Interface, data input
15	SCK	SPI Interface, clock input
16	NCS	SPI Interface, chip select (low active)
17	VDD	3.0 . . . 5.5 V Supply Voltage
18	ACT0	Actuator Output 0
19	ACT1	Actuator Output 1
20	TPI	Touch Probe Input

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD		-0.3	7	V
G002	V()	Voltage at MA, SLI, NERR, NWARN, NCS, SCK, MOSI, TPI		-0.3	7	V
G003	I()	Current in MA, SLI, NERR, NWARN, NCS, SCK, MOSI, TPI		-4	4	mA
G004	V()	Voltage at AP, AN, BP, BN, CP, CN		-7	7	V
G005	I()	Current in AP, AN, BP, BN, CP, CN		-20	20	mA
G006	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G007	Tj	Junction Temperature		-40	150	°C
G008	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	ºC

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3 . . . 5.5 V, Tj = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VDD	Voltage Supply VDD		3		5.5	V
002	I(VDD)	Supply Current in VDD	TTL input configuration, 48 bits counter 10 MHz signal in AP (0° phase) and AN (90° phase), BP, BN, CP and CN to GND			15	mA
003	Vc()hi	Clamp Voltage hi	Vc()hi = V() - VDD, I() = 1 mA, all pins	0.4		1.5	V
004	Vc()lo	Clamp Voltage lo	Vc()hi = V() - VDD, I() = 1 mA, all pins	-1.5		-0.25	V
Digital Inputs: MA, SLI, SCK, MOSI, NCS, TPI							
101	Vt()hi	Input Threshold Voltage hi				2	V
102	Vt()lo	Input Threshold Voltage lo	VDD = 4.5 . . . 5.5 V VDD = 3 . . . 5.5 V	0.8 0.75			V V
103	Vt()hys	Input Hysteresis		150	250		mV
104	Ipd()	Input Pull-down Current at SCK, MOSI, TPI	V() = 1 V . . . VDD	2	30	75	µA
105	Ipu()	Input Pull-Up Current at NCS, MA	V() = 0 V . . . VDD - 1 V	-75	-30	-2	µA
106	fclk(MA)	Permissible Clock Frequency at MA	ENSSI = 1 (SSI protocol) ENSSI = 0 (BiSS protocol)			4 10	MHz MHz
107	Voc()	Pin Open Voltage at SLI		42	46.5	51	%VDD
108	Ri()	Internal Resistance at SLI	Referenced to VDD Referenced to GND	70 40		170 110	kΩ kΩ
109	to(SLI)	Digital Filter at SLI	SLI = open	5		25	µs
110	fclk(SCK)	Permissible Clock Frequency at SCK				10	MHz
Bidirectional Pins: NWARN, NERR							
201	Ipu()	Pull-Up Current	V() = 0 V . . . VDD - 1 V	-850	-100	-10	µA
202	Vt()hi	Input Threshold Voltage hi				2	V
203	Vt()lo	Input Threshold Voltage lo	VDD = 4.5 . . . 5.5 V VDD = 3 . . . 5.5 V	0.8 0.75			V V
204	Vt()hys	Input Hysteresis		150	250		mV
205	Vs()lo	Saturation Voltage lo	I() = 4 mA			450	mV
206	Isc()lo	Short-Circuit Current lo	V() = 0 V . . . VDD	4		100	mA
ABZ Counter							
301	R()	Counter Resolution				48	bit
302	fcnt()	Permissible Count Frequency				40	MHz
303	PHab2	Permissible A/B Phase Distance	edge A vs. edge B and vice versa TTL=1 TTL=0, LVDS=X	 5 13			 ns ns
Power-Down Reset and Oscillator							
601	VDDon	Power-On Supply Voltage				2.9	V
602	VDDoff	Power-Down Voltage		2.1			V
603	VDDhys	Power-On Hysteresis	VDDon - VDDoff	35	100		mV
604	f(CLK)	Internal Oscillator Frequency	VDD = 3.5 . . . 5.5 V VDD = 3 . . . 3.5 V	1.4 1.6		5.6 6.7	MHz MHz
Digital Outputs: SLO, MISO, ACT0, ACT1							
701	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(), I() = -4 mA			450	mV
702	Vs()lo	Saturation Voltage lo	I() = 4 mA			450	mV
703	Isc()hi	Short-Circuit Current hi	V() = 0 . . . VDD	-115			mA
704	Isc()lo	Short-Circuit Current lo	V() = 0 . . . VDD			100	mA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3 . . . 5.5 V, Tj = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
RS-422 Configuration: Differential Inputs AP, AN, BP, BN, CP, CN							
A01	Vcm()	Common Mode Voltage Range	TTL = 0, LVDS = 0 VDD = 4.5 . . . 5.5 V VDD = 3 . . . 5.5 V	 0 0		 3 1.5	 V V
A02	Vd()	Differential Input Threshold Voltage	TTL = 0, LVDS = 0, V() = V(AP) - V(AN) V() = V(BP) - V(BN) V() = V(CP) - V(CN)	-300		300	mV
A03	Vhys()	Differential Input Hysteresis	TTL = 0, LVDS = 0, Vhys() = Vth()hi-Vth()lo (guaranteed by design)	2.5		10	mV
TTL Configuration: Input AP, AN, BP, BN, CP, CN							
B01	Vt()hi	Input Threshold Voltage hi at AP, AN, BP, BN, CP, CN	TTL = 1, LVDS = 0			2	V
B02	Vt()lo	Input Threshold Voltage lo at AP, AN, BP, BN, CP, CN	TTL = 1, LVDS = 0	0.8			V
B03	Vt()hys	Input Hysteresis at AP, AN, BP, BN, CP, CN	TTL = 1, LVDS = 0	150	300		mV
B04	Rpd()	Pull-Down Resistor	TTL = 1, LVDS = 0	35	50	65	kΩ
LVDS Configuration: Differential Inputs AP, AN, BP, BN, CP, CN							
C01	Vin()	Input Voltage Range	TTL = 0, LVDS = 1 VDD = 4.5 . . . 5.5 V VDD = 3 . . . 5.5 V	 0.8 0.8		 3 1.5	 V V
C02	Vd()	Differential Input Threshold Voltage	TTL = 0, LVDS = 1 V() = V(AP)-V(AN) V() = V(BP)-V(BN) V() = V(CP)-V(CN)	-200		200	mV
C03	Vhys()	Differential Input Hysteresis	TTL = 0, LVDS = 1 Vhys() = Vth()hi-Vth()lo (guaranteed by design)	1.2		12	mV

OPERATING REQUIREMENTS: SPI Interface

Operating Conditions: VDD = 3 . . . 5.5 V, Tj = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SPI Interface						
I001	tsCCL	Setup Time: NCS hi → lo before SCK lo → hi		15		ns
I002	tsDCL	Setup Time: MOSI stable before SCK lo → hi		20		ns
I003	thDCL	Hold Time: MOSI stable after SCK lo → hi		0		ns
I004	tCLh	Signal Duration SCK hi		25		ns
I005	tCLl	Signal Duration SCK lo		25		ns
I006	thCLC	Hold Time: NCS lo after SCK lo → hi		25		ns
I007	tCSh	Signal Duration NCS hi		0		ns
I008	tpCLD	Propagation Delay: MISO stable after SCK hi → lo			40	ns
I009	tpCSD	Propagation Delay: MISO high impedance after NCS lo → hi			25	ns
I010	f(SCK)	Clock Frequency			10	MHz

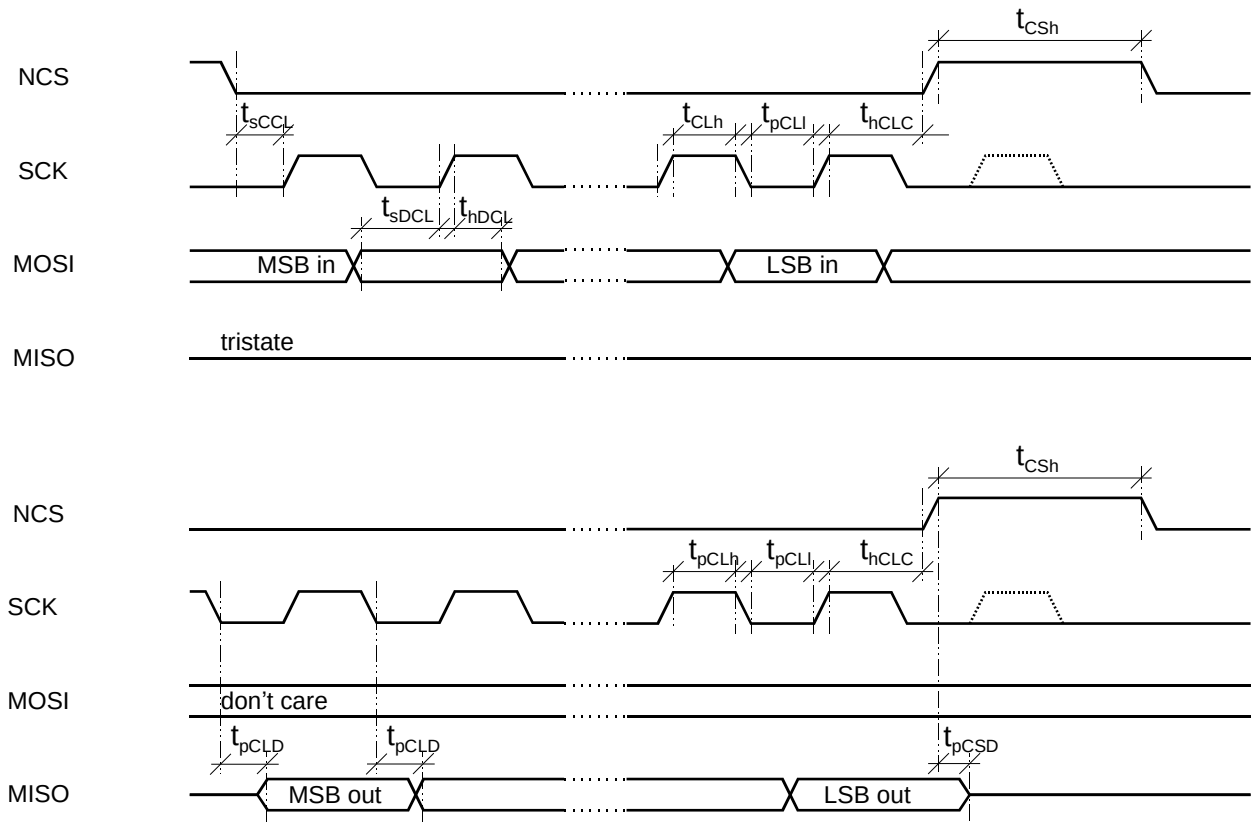


Figure 1: SPI write cycle (top) and read cycle (bottom)

OPERATING REQUIREMENTS: BiSS and SSI Interface

Operating Conditions: VDD = 3 . . . 5.5 V, Tj = -40 . . . 125 °C, unless otherwise noted; input levels lo = 0 ... 0.45 V, hi = 2.4 V ... VDD

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI Output (ENSSI = 1)						
I101	T_{MAS}	Permissible Clock Period	ENSSI = 1 SLI = open	250	2x t_{tos}	ns
I102	t_{MASh}	Clock Signal Hi Level Duration		25	t_{tos}	ns
I103	t_{MASl}	Clock Signal Lo Level Duration		25	t_{tos}	ns
BiSS C Single Cycle Data						
I104	T_{MAS}	Permissible Clock Period	ENSSI = 0	100		ns
I105	t_{MASh}	Clock Signal Hi Level Duration		25	t_{tos}	ns
I106	t_{MASl}	Clock Signal Lo Level Duration		25		ns

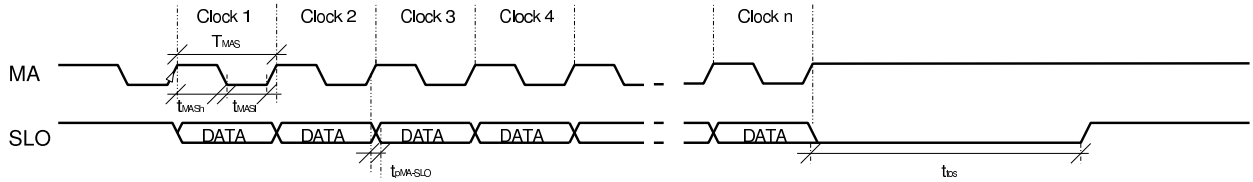


Figure 2: Timing diagram of SSI output.

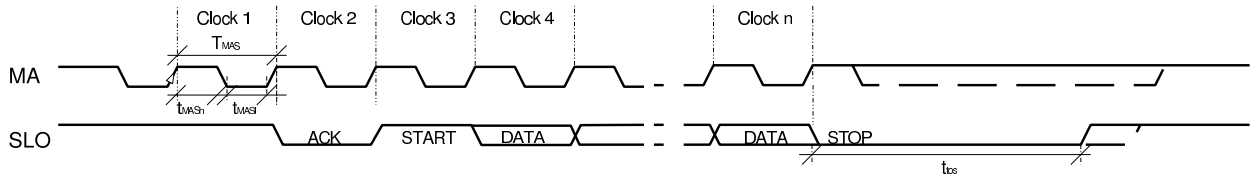


Figure 3: Timing diagram of BiSS C DATA (here: CDS, counter data, status, CRC)

CONFIGURATION PARAMETERS

Read/Write Registers

Configuration

INVZ0	Invert Z On CNT0 (P. 13)
INVZ1	Invert Z On CNT1 (P. 13)
EXCH0	Exchange AB On CNT0 (P. 13)
EXCH1	Exchange AB On CNT1 (P. 13)
EXCH2	Exchange AB On CNT2 (P. 13)
CNTCFG(2:0)	Counter Length Configuration (P. 12)
TTL	TTL Inputs (P. 13)
CBZ0	CNT0 Cleared By Z0 Signal (P. 12)
CBZ1	CNT1 Cleared By Z1 Signal (P. 12)
CFGZ(1:0)	Index Signal Configuration (P. 12)
TPCFG(1:0)	TPI Pin Configuration (P. 16)
PRIOR	SPI Interface Priority (P. 26)
MASK(9:0)	Error/Warning Event Mask (P. 21)
NMASK(1:0)	Error/Warning Event Not Mask (P. 21)
LVDS	LVDS/RS-422 Inputs (P. 13)
CH0SEL	BiSS Channel Selection CH0 (P. 25)
CH1SEL	BiSS Channel Selection CH1 (P. 25)
CH2SEL	BiSS Channel Selection CH2 (P. 25)
NENCH0	Disable BiSS Channel 0 (P. 25)
ENCH1	Enable BiSS Channel 1 (P. 25)
ENCH2	Enable BiSS Channel 2 (P. 25)

Table 6: Register Description

Write Only Registers

Instructions

ACT0	Control Actuator Pin ACT0 (P. 17)
ACT1	Control Actuator Pin ACT1 (P. 17)
TP	Touch Probe Instruction (P. 17)
ZCEN	Enable Zero Codification (P. 17)
ABRES0	Reset Counter CNT0 (P. 17)
ABRES1	Reset Counter CNT1 (P. 17)
ABRES2	Reset Counter CNT2 (P. 17)

Table 7: Instruction Byte

Read Only Registers

Measurement Data and Status

AB	AB Counter Values (P. 16)
NWARN	No Warning (P. 16)
NERR	No Error (P. 16)
TP1	Touch Probe Register 1 (P. 16)
TP2	Touch Probe Register 2 (P. 16)
NTPVAL	Touch Probe Register Not Valid (P. 16)
NABERR	No AB Counter Error (P. 16)
REF	Reference Counter Value (P. 14)
UPD	Update Register (P. 15)
NUPDVAL	Update Register Not Valid (P. 15)

Table 8: Counter Registers

Errors

ABERRx	AB Decodification Error Counter CNTx (P. 18)
EXTERR	External Error (P. 19)

Table 9: Error Registers

Warnings

OVFx	Counter Overflow Warning Counter CNTx (P. 18)
ZEROx	Zero Value In Counter CNTx (P. 18)
PDWN	Undervoltage Reset (P. 18)
RVAL	REF Register Value Valid (P. 18)
UPDVAL	UPD Update Register Valid (P. 18)
OVFREF	Reference Counter Overflow (P. 19)
TPVAL	Touch Probe Values Valid (P. 19)
EXTWARN	External Warning (P. 19)
COMCOL	Communication Collision (P. 19)
TPS	Touch Probe Pin Status (P. 19)
ENSSI	SSI Enabled (P. 19)

Table 10: Warning Registers

BiSS Identifier

BiSS Device ID	(P. 26)
BiSS Device Revision	(P. 26)
BiSS Device Manufacturer ID	(P. 26)

Table 11: Warning Registers

REGISTER MAP

PROGRAMMING								
Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration								
0x00	INVZ1	INVZ0	EXCH2	EXCH1	EXCH0	CNTCFG(2:0)		
0x01	TTL	CBZ1	CBZ0	CFGZ(1:0)		TPCFG(1:0)		PRIOR
0x02	MASK(7:0)							
0x03	LVDS	Reserved			NMASK(1:0)		MASK(9:8)	
0x04	CH2SEL	ENCH2	CH1SEL	ENCH1	CH0SEL	NENCH0	Reserved	
0x05	Reserved							
0x06	Reserved			Reserved	Reserved			
0x07	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Measurement Data (SPI read only)								
0x08	AB/SPICH(47:0) + NERR + NWARN							
0x09	Reserved							
0x0A	UPD(23:0) + NABERR + NUPDVAL							
0x0B	Reserved							
0x0C	TP1(23:0) + NABERR + NTPVAL							
0x0D	Reserved							
0x0E	TP2(23:0) + NABERR + NTPVAL							
Measurement Data (SPI and BiSS read only)								
0x10	REF(23:16)							
0x11	REF(15:8)							
0x12	REF(7:0)							
SPI write only data. (read via AB)								
0x20	SPICH(47:40)							
0x21	SPICH(39:32)							
0x22	SPICH(31:24)							
0x23	SPICH(23:16)							
0x24	SPICH(15:8)							
0x25	SPICH(7:0)							
Instruction Byte (write only)								
0x30	Reserved	ACT1	ACT0	TP	ZCEN	ABRES2	ABRES1	ABRES0
BiSS Profile ID (SPI and BiSS read only)								
0x42	BiSS Profile ID: 0x33							
0x43	BiSS Profile ID: 0x18							
Status								
0x48	ABERR0	OVF0	ZERO0	PDWN	RVAL	UPDVAL	OVFREF	TPVAL
0x49	ABERR1	OVF1	ZERO1	PDWN	EXTERR	EXTWARN	COMCOL	TPS
0x4A	ABERR2	OVF2	ZERO2	PDWN	EXTERR	EXTWARN	COMCOL	ENSSI

PROGRAMMING								
Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BiSS Device and Manufacturer ID (SPI and BiSS read only)								
0x78	BiSS Device ID - 0x4D ('M')							
0x79	BiSS Device ID - 0x44 ('D')							
0x7A	BiSS Device Revision - 0x58 ('X')							
0x7B	BiSS Device Revision - 0x00 ('0')							
0x7C	BiSS Device Revision - 0x00 (")							
0x7D	BiSS Device Revision - 0x00 (")							
0x7E	BiSS Device Manufacturer ID (default 0x69)							
0x7F	BiSS Device Manufacturer ID (default 0x43)							

Table 12: Register layout

COUNTER CONFIGURATION

iC-MD has a 48 bit counter configurable from single to up to three counters with bit lengths from 16 to 48 bit. Table 13 show all the possible counters configuration considering table 18 and table 20.

The ”count of counter” configuration is given by the registers CNTCFG as shown in table 13.

If it is configured with more than one counter, the input stage must be set to TTL (table 17).

CNTCFG	Addr. 0x00; bit (2:0)	Default = 0b000
Code	Counter Configuration	
000	CNT0 = 24 bit: 1 counter: TTL, RS422 or LVDS	
001	CNT0 = 24 bit + CNT1 = 24 bit:2 counter: TTL only	
010	CNT0 = 48 bit: 1 counter: TTL, RS422 or LVDS	
011	CNT0 = 16 bit: 1 counter: TTL, RS422 or LVDS	
100	CNT0 = 32 bit: 1 counter: TTL, RS422 or LVDS	
101	CNT0 = 32 bit + CNT1 = 16 bit: 2 counter: TTL only	
110	CNT0 = 16 bit + CNT1 = 16 bit: 2 counter: TTL only	
111	CNT0 = 16 bit + CNT1 = 16 bit + CNT2 = 16 bit: 3 counter: TTL only	

Table 13: Count of Counter and Counter Length Configuration

Note that the three counter configuration does not implement any Zero signal input, only A and B input signals.

The 48 bit register of the AB counter is also used as "SPI data channel" for data exchanging between SPI and BiSS interface, for that purpose the bit CH0SEL (table 65) must be set to 1. When CH0SEL = 1, the counting function for all the counters is deactivated.

Index Signal Z

In default operation configuration, the index signal Z is active when A = B = 1, as shown in table 14 with EXCH = 0 and INVZ = 0. All other configurations are also possible.

CFGZ	Addr. 0x01; bit (4:3)	Default = 0b00
Code	Function:	
00	Z active: when A = 1 B = 1	
01	Z active: when A = 1 B = 0	
10	Z active: when A = 0 B = 1	
11	Z active: when A = 0 B = 0	

Table 14: Index Signal Configuration

It can also be deactivated the clearing of counter by the index signal with the configuration bit CBZ (table 15 and table 16).

The CBZ configuration is only applicable after the second index pulse after power-on or the activation of ZCEN (table 40), because after it, the iC-MD will reset the counter value by the firsts two index pulse, independently of the CBZ configuration, in order to have the AB Counter value referenced to the second index pulse. By default, CBZ is set to 0, also the counters are not reset to 0 by the index signal. But the firsts two Index pulse always reset the counters.

CBZ0	Addr. 0x01; bit (5)	Default = 0b0
Code	Function	
0	CNT0 not cleared by Z0 signal	
1	CNT0 cleared by Z0 signal	

Table 15: CNT0 Cleared By Z0 Signal

CBZ1	Addr. 0x01; bit (6)	Default = 0b0
Code	Function	
0	CNT1 not cleared by Z1 signal	
1	CNT1 cleared by Z1 signal	

Table 16: CNT0 Cleared By Z1 Signal

INPUT CONFIGURATION

The input stage for the incremental signals ABZ is configurable as single-ended TTL and differential (RS-422 or LVDS). Differential inputs are possible only for a single counter configuration and the input configuration shown in table 18.

TTL	Addr. 0x01; bit (7)	Default = 0b0
Code	Function	
0	Differential inputs	
1	TTL inputs	

Table 17: TTL Inputs

Counter	A0		B0		Z0	
1xDifferential	AP	AN	BP	BN	CP	CN

Table 18: RS422 or LVDS Input Counters Configuration

If two or more counter are configured, the TTL input configuration shown in table 20 must be used and table 13 shows all the possible counter configuration.

It is possible to configure the differential input stage of iC-MD in two different modes; differential RS-422 and differential LVDS. See table 19.

LVDS	Addr. 0x03; bit (7)	Default = 0b0
Code	Function	
0	Differential RS-422 inputs	
1	Differential LVDS inputs	
Notes	condition: TTL=0	

Table 19: LVDS/RS-422 Inputs

Counters	A0	B0	Z0	A1	B1	Z1	A2	B2
1xTTL	AP	AN	BP	-	-	-	-	-
2xTTL	AP	AN	BP	BN	CP	CN	-	-
3xTTL	AP	AN	-	BP	BN	-	CP	CN

Table 20: TTL Input Counters Configuration

Note that the three counters configuration don't implement any Zero signal. It has only A and B input signals.

Register bits TTL and LVDS set the configuration of the quadrature input signals.

The configuration bit EXCH exchanges the input A and the input B of the counters. The default counting direction is positive in clockwise (CW) direction (A edge take place before B edge). But it is also possible to change the counting direction with the register EXCH. See table 21, table 22 and table 23.

EXCH0	Addr. 0x00; bit (3)	Default = 0b0
Code	Function	
0	Exchange AB CNT0 (CW positive)	
1	Exchange AB CNT0 (CCW positive)	

Table 21: Exchange AB Inputs Channel on Counter CNT0

EXCH1	Addr. 0x00; bit (4)	Default = 0b0
Code	Function	
0	Exchange AB CNT1 (CW positive)	
1	Exchange AB CNT1 (CCW positive)	

Table 22: Exchange AB Inputs on Counter CNT1

EXCH2	Addr. 0x00; bit (5)	Default = 0b0
Code	Function	
0	Exchange AB CNT2 (CW positive)	
1	Exchange AB CNT2 (CCW positive)	

Table 23: Exchange AB Inputs on Counter CNT2

The index (Z) signal can be inverted as shown in table 24 and table 25 with the register bits INVZ(1:0).

INVZ0	Addr. 0x00; bit (6)	Default = 0b0
Code	Function	
0	Non inverted Z on CNT0	
1	Inverted Z on CNT0(Z=0 active)	

Table 24: Invert Z Signal Counter CNT0

INVZ1	Addr. 0x00; bit (7)	Default = 0b0
Code	Function	
0	Non inverted Z on CNT1	
1	Inverted Z on CNT1(Z=0 active)	

Table 25: Invert Z Signal Counter CNT1

24 BIT REFERENCE COUNTER

An additional 24 bit counter is integrated in order to load the REF and UPD registers. The value of this internal counter can not be read, it can only be read the values of REF and UPD registers. The reference counter is activated by default after power-on and reset with every index signal (it is not affected by the configuration bit CFGZ, table 14).

Since the internal counter for REF and UPD is 24 bit long, the maximum number of edges that can be evaluated (loaded in UPD and REF) between two index signal goes from -2^{23} (negative counting direction) to $2^{23}-1$ (positive counting direction).

REF REGISTER

After the start up (Power on), the iC-MD counts the number of edges between the first two different index signals (Z) in the register REF. This function is always activated by the following situations:

- after power-on.
- by activating the zero codification function via instruction byte (table 40).

The process runs as following: the "reference counter" is set to zero with the first index signal, and the second index signal (must be different of the first one) loads the register REF with the value of "reference counter". It is the distance between the first and the second index signals. The AB counter is then set to 0 with the second index signal. The counter value is then referenced to the position of the second Z signal, and the number of edges between the first two index signals stored in REF.

REF(23:0)	Addr. 0x10 to 0x12;	R
0xXXXXXX	REF register value	

Table 26: Reference Counter Value

After the second index signal, the status bit RVAL (table 48) is set and remains at this value until the next power on, the activation of the zero codification function or until the resetting of the counter 0.

The following diagrams show the reference position acquisition process also called as zero codification function.

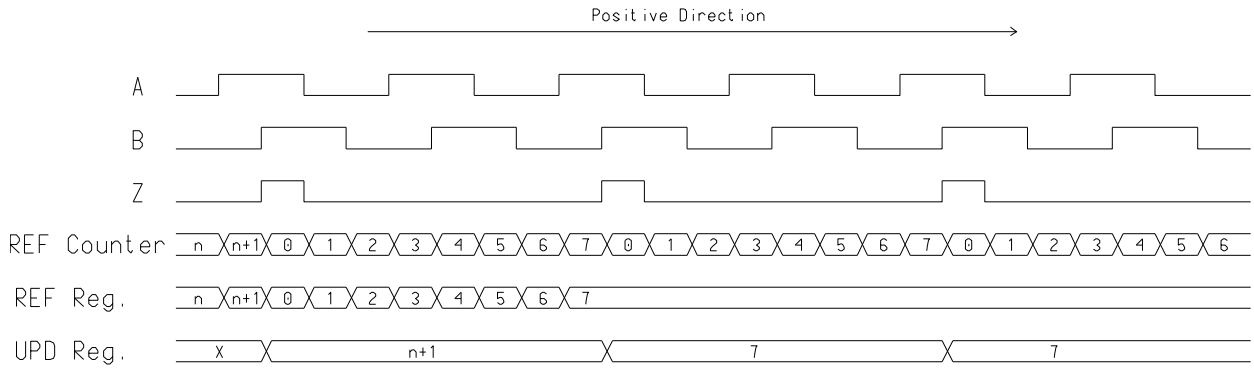


Figure 4: Zero-Codification: REF and UPD registers after activation of Zero Codification function

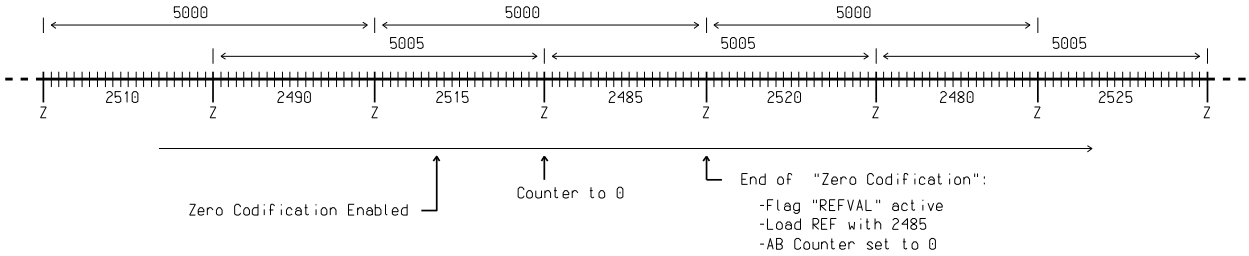


Figure 5: Zero-Codification: reference position acquisition

UPD REGISTER

The register UPD is load at every index pulse with the value of the "reference counter", it is the number of AB edges between the last two index pulses (value of the reference counter). It is used to check that any AB pulse was lost.

The status bit UPDVAL (table 49) signals that a new UPD value is available (UPD register was loaded and still not read).

UPD(23:0)	Addr. 0x0A;	R
0xXXXXXX	UPD register value	

Table 27: Update Register Value

NUPDVAL	Addr. 0x0A;	R
0	UPD value valid	
1	UPD value not valid	

Table 28: Update Register Not Valid

The following diagram shows the value of REF and UPD after activating the zero codification function when counting in negative direction.

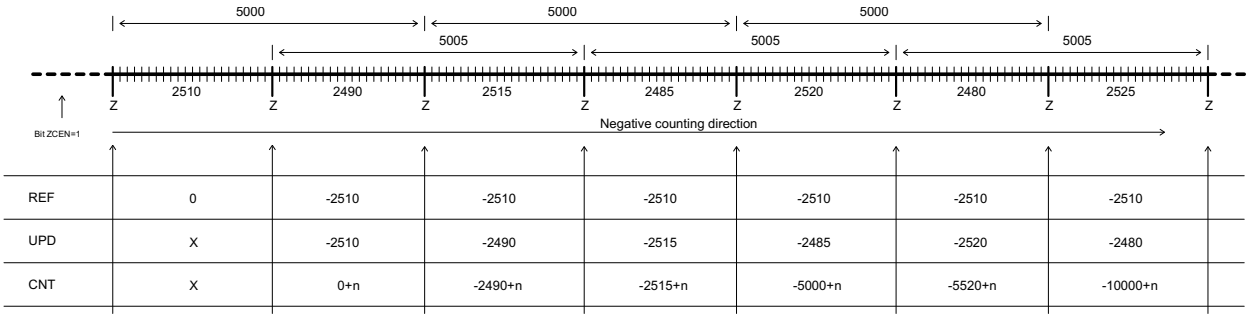


Figure 6: REF and UPD registers in negative direction

TP1, TP2 and AB REGISTERS

TP1, TP2 Registers

The touch probe registers consist of two 24 bit registers which are load with a TPI pin event (see table 29) or writing the instruction bit TP (table 41) via SPI/BiSS. At every TPI pin or TP instruction event, the register TP2 is load with the value of TP1 and TP1 is load with the actual value of counter 0. For using TP registers, AB counter must be configured to 24 bit, but if 2x24 bit counters are configured, only the counter 0 will be latched into TP1/TP2 registers. The TPI pin events can be configured as falling, rising or both edges, as shown in table 29.

TPCFG	Addr. 0x01; bit (2:1)	Default = 0b00
Code	Function	
00	both edges active	
01	rising edge active	
10	falling edge active	
11	pin TPI disabled	

Table 29: TPI Pin Configuration

TP1(23:0)	Addr. 0x0C;	R
0xXXXXXX	TP1 value	

Table 30: Touch Probe 1

TP2(23:0)	Addr. 0x0E;	R
0xXXXXXX	TP2 value	

Table 31: Touch Probe 2

NTPVAL	Addr. 0x0C or 0x0E;	R
0	TP valid	
1	TP not valid	

Table 32: Touch Probe Register Not Valid

The following diagram (figure 7) shows the function of the pin TPI when configured for both rising and falling edge.

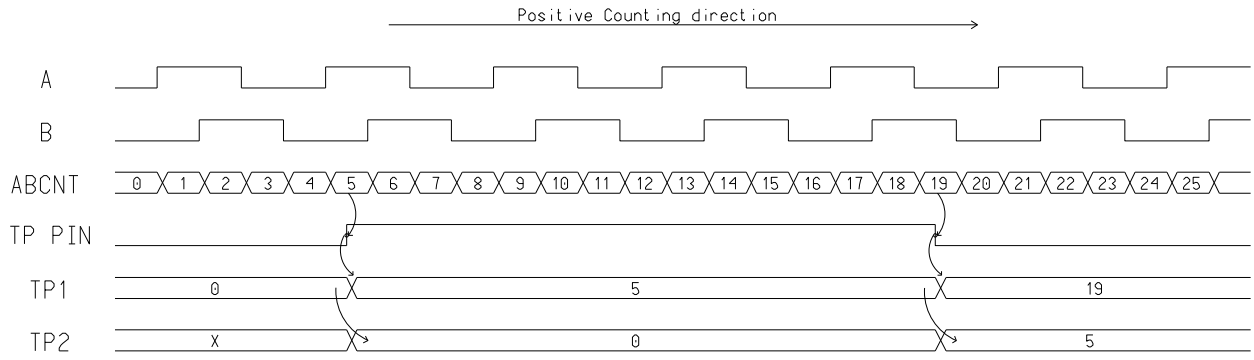


Figure 7: Function of TPI pin when TPCFG=11

AB Register

A 48 bit register (AB) is used to store and shift out the ABCNT Registers (Counters), and also the "SPI Channel Data" (SPICH). The register AB is read via BiSS (sensor data, channel 0) or via SPI (Adr 0x08), and the bit length is set by the configuration bits CNTCFG (table 13)

AB(47:0)	Addr. 0x08;	R
0xXX..XX	AB counter value	

Table 33: AB Counter Values

NWARN	Addr. 0x08;	R
0	Warning active	
1	No warning active	

Table 34: No Warning

NERR	Addr. 0x08;	R
0	Error active	
1	No Error active	

Table 35: No Error

NABERR	Addr. 0x0A or 0x0C or 0x0E;	R
0	AB counter value error	
1	AB counter correct value	

Table 36: No AB Counter Error

The bit CH0SEL (table 65) selects the data to be load in the AB register when reading the channel 0 via BiSS or the address 0x08 via SPI.

COMMUNICATION CONTROL

iC-MD can communicate simultaneously via SPI and BiSS in order to exchange data between SPI and BiSS. For this purpose, SPI writes the data to be read by BiSS in the AB register, and BiSS reads the SPICH (BiSS channel 0 configured as SPICH, see table 65).

If both interfaces attempt to read or write at the same time a different RAM address than the SPICH (Adr. 0x20 to 0x25), then the bit error COMCOL (table 54) is set and the communication of the interface without priority (see table 71) is not valid.

Instruction Byte

Register address 0x30 contains the write only instruction byte. When one of these bits is set to 1, then the corresponding operation is executed and then set back to 0, excepts the bits ACT0 and ACT1 which remain to the written value.

ABRES0	Addr. 0x30; bit 0	Default = 0b0
Code	Function	
1	Reset of counter 0	

Table 37: Reset Counter 0

ABRES1	Addr. 0x30; bit 1	Default = 0b0
Code	Function	
1	Reset of counter 1	

Table 38: Reset Counter 1

ABRES2	Addr. 0x30; bit 2	Default = 0b0
Code	Function	
1	Reset of counter 2	

Table 39: Reset Counter 2

ZCEN	Addr. 0x30; bit 3	Default = 0b0
Code	Function	
1	Enable zero codification	

Table 40: Enable Zero Codification

TP	Addr. 0x30; bit 4	Default = 0b0
Code	Function	
1	Load TP2 with TP1 value and TP1 with ABCNT value	
Notes	Counter must be configured to 24 bit length	

Table 41: Touch Probe Instruction

The instruction bits ACT0 and ACT1 set the actuator pins ACT0 and ACT1 to high or low voltage.

ACT0	Addr. 0x30; bit 5	Default = 0b0
Code	Function	
0	Set actuator pin 0 to GND	
1	Set actuator pin 0 to VDD	

Table 42: Control Actuator Pin 0

ACT1	Addr. 0x30; bit 6	Default = 0b0
Code	Function	
0	Set actuator pin 1 set to GND	
1	Set actuator pin 1 set to VDD	

Table 43: Control Actuator Pin 1

STATUS REGISTER and ERROR/WARNING INDICATION

The three bytes status registers (Adr. 0x48 to 0x4A) indicate the state of the iC-MD. All the status bits are latched (except TPS) when an error/warning occurs and are reset when reading the error/warning via SPI or BiSS excepts RVAL. The status bits TPVAL and UPDVAL are also reset by reading the register TP1 and UPD respectively.

The status bit TPS (table 55) is not latched, it signals the actual state of the input pin TPI.

Two of this status bits are error bits; ABERR (AB decodification error, table 44) and EXTERR (external error, table 52), all others status bits signal warnings.

Status bits ABERRx indicate a decodification error of the AB inputs, it occurs if the counting frequency is too high or if two incremental edges are too close (PHab2, Spec. Item No.303).

ABERRx	Addr. 0x48, 0x49, 0x4A; bit 7	R
Code	Description	
0	No decodification error in counter x	
1	Decodification error in counter x	
Notes	x = 0, 1, 2 Reset by reading Adr. 0x48 (ABERR0), 0x49 (ABERR1) and 0x4A (ABERR2) The corresponding counter must be reset (ABRES) after an error	

Table 44: AB Decodification Error of Counter CNTx

The maximum counting range of the counters depends on the counter configuration (see table 13). A counter with the bit length "n" has the maximum counting range will be from -2^{n-1} up to $2^{n-1}-1$. The corresponding bit OVFx is set to 1 if the counter exceeds these values.

OVFx	Addr. 0x48, 0x49, 0x4A; bit 6	R
Code	Description	
0	no overflow in counter x	
1	overflow in counter x	
Notes	x = 0, 1, 2 reset by reading Adr. 0x48 (OVF0), 0x49 (OVF1) and 0x4A (OVF2)	

Table 45: Counter Overflow Warning of Counter CNTx

ZEROx bits indicate that the counter value has reached the zero value.

ZEROx	Addr. 0x48, 0x49, 0x4A; bit 5	R
Code	Description	
0	no zero of counter x	
1	zero of counter x	
Notes	x = 0, 1, 2 reset by reading Adr. 0x48 (ZERO0), 0x49 (ZERO1) and 0x4A (ZERO2)	

Table 46: Zero Value in Counter CNTx

If VDD reaches the power off supply level (VDDoff, Spec. Item No. 602), the iC-MD is reset and the RAM initialized to the default value. Status bit PDWN indicates that this initialization has taken place.

PDWN	Addr. 0x48, 0x49, 0x4A; bit 4	R
Code	Description	
0	No undervoltage	
1	Undervoltage(RAM was reset)	
Notes	Reset by reading Adr. 0x48, 0x49 or 0x4A	

Table 47: Undervoltage Reset

RVAL status bit indicates that the reference value was load in the REF register, after the "Zero Codification" process. After power-on, this bit remains at 0 until the second different Index pulse.

RVAL	Addr. 0x48; bit 3	R
Code	Description	
0	REF Reg. not valid	
1	REF Reg. valid	
Notes	Reset by the instruction ZCEN(see table 40)	

Table 48: REF Register Values Valid

Every time that the UPD register is loaded, the status bit UPDVAL (UPD valid) is set to 1 until the status bit UPD or the register UPD is read via SPI or BiSS.

UPDVAL	Addr. 0x48; bit 2	R
Code	Description	
0	UPD Reg. not valid	
1	UPD Reg. valid	
Notes	Reset by reading Adr. 0x48 or the register UPD via SPI (Adr. 0x0A) or BiSS (Channel 1)	

Table 49: UPD Register Values Valid

If the number of AB edges between two index signals is greater than $2^{23}-1=8388607$ or lower than

-2^{23}=-8388608 the status bit OVFREF is set to 1 and indicates that the value of the UPD and REF registers are not valid.

OVFREF	Addr. 0x48; bit 1	R
Code	Description	
0	No Overflow in reference counter	
1	Overflow in reference counter	
Notes	Reset by reading Adr. 0x48	

Table 50: Reference Counter Overflow

After loading TP1/TP2 register, either via pin TPI or instruction TP (see table 41), the bit TPVAL is set to 1 and remains at 1 until the reading of TPVAL, TP1 or TP2 via SPI or BiSS.

TPVAL	Addr. 0x48; bit 0	R
Code	Description	
0	TPx registers not loaded TP1 and TP2 registers have not been updated	
1	New values loaded in TP1 and TP2	
Notes	Reset by reading Adr. 0x48, register TP1 or register TP2 via SPI (Adr. 0x0C and 0x0E) or BiSS (channel 1 and channel 2, see table 65)	

Table 51: Touch Probe Values Valid

The status bit (EXTERR: external error) indicates if the pin NERR was either pulled-down from outside or set to 0 from inside (an internal masked error has occurred).

EXTERR	Addr. 0x49, 0x4A; bit 3	R
Code	Description	
0	no external error	
1	external error	
Notes	Reset by reading Adr. 0x49 or 0x4A	

Table 52: External Error

The status bit (EXTWARN: external warning) bit indicates if the pin NWARN was either pulled-down from outside or set to 0 from inside (an internal masked warning has occurred).

EXTWARN	Addr. 0x49, 0x4A; bit 2	R
Code	Description	
0	no external warning	
1	external warning	
Notes	reset by reading Adr. 0x49 or 0x4A	

Table 53: External Warning

If BiSS/SSI and SPI try to access at the same time to the internal data bus (BiSS register communication and SPI communication) the bit COMCOL will be set indicating that a collision has taken place. If SPICH is activated (table 65), the writing process of AB via SPI and reading of channel 0 via BiSS at the same time will generate no COMCOL warning.

If a communication collision take place, only the interface with priority (See table 71) executes the write/read process correctly, but the other interface doe not write any data, the other interface does read a false value.

COMCOL	Addr. 0x49, 0x4A; bit 1	R
Code	Description	
0	no communication collision	
1	communications collided	
Notes	reset by reading Adr. 0x49 or 0x4A	

Table 54: Communication Collision

Bit TPS signals the actual state of the input pin TPI. If the pin TPI is high, the bit TPS remains at 1, and if TPI is set to low, TPS status bit is 0.

TPS	Addr. 0x49; bit 0	R
Code	Description	
0	TPI pin at low	
1	TPI pin at high	

Table 55: Touch-Probe Pin Status

Status bit ENSSI signals if the SSI interface instead of BiSS is configured. This is configured by the SLI pin, if the pin is open, the SSI interface is selected. ENSSI has an internal digital filter of 25 µs maximum.

ENSSI	Addr. 0x4A; bit 0	R
Code	Description	
0	SSI not enabled	
1	SSI enabled (pin SLI open)	

Table 56: SSI Enabled

Error and warning mask

The masks (MASK) and not masks (NMASK) bits, stipulate whether error and warning events are signaled as an alarm via the open drain I/O pins NERR and NWARN.

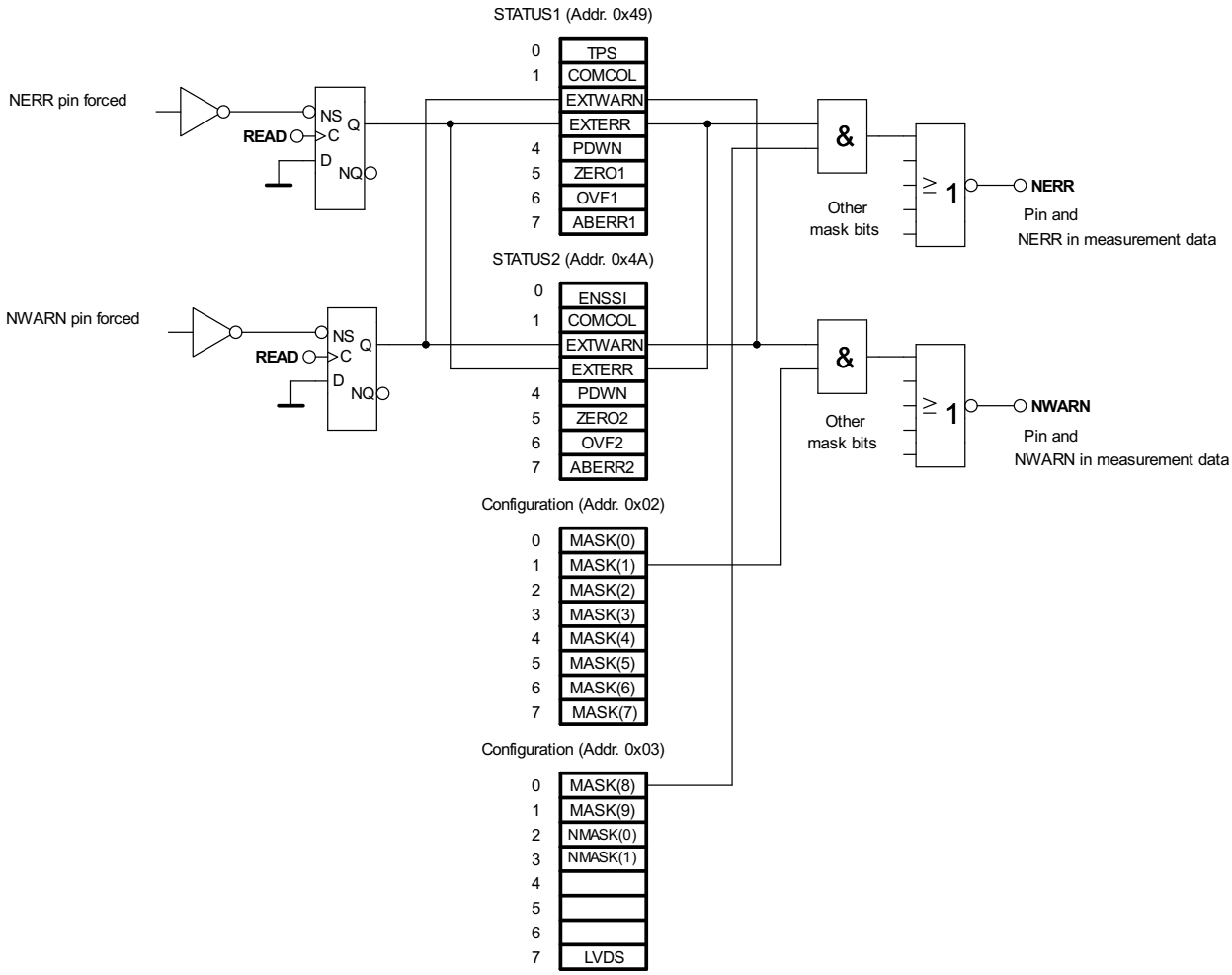


Figure 8: MASK gating

The latched events are reset with reading the STATUS addresses 0x48, 0x49 or 0x4A unless the event signals do not persist. The read access is indicated by the latch reset signal ”READ”.

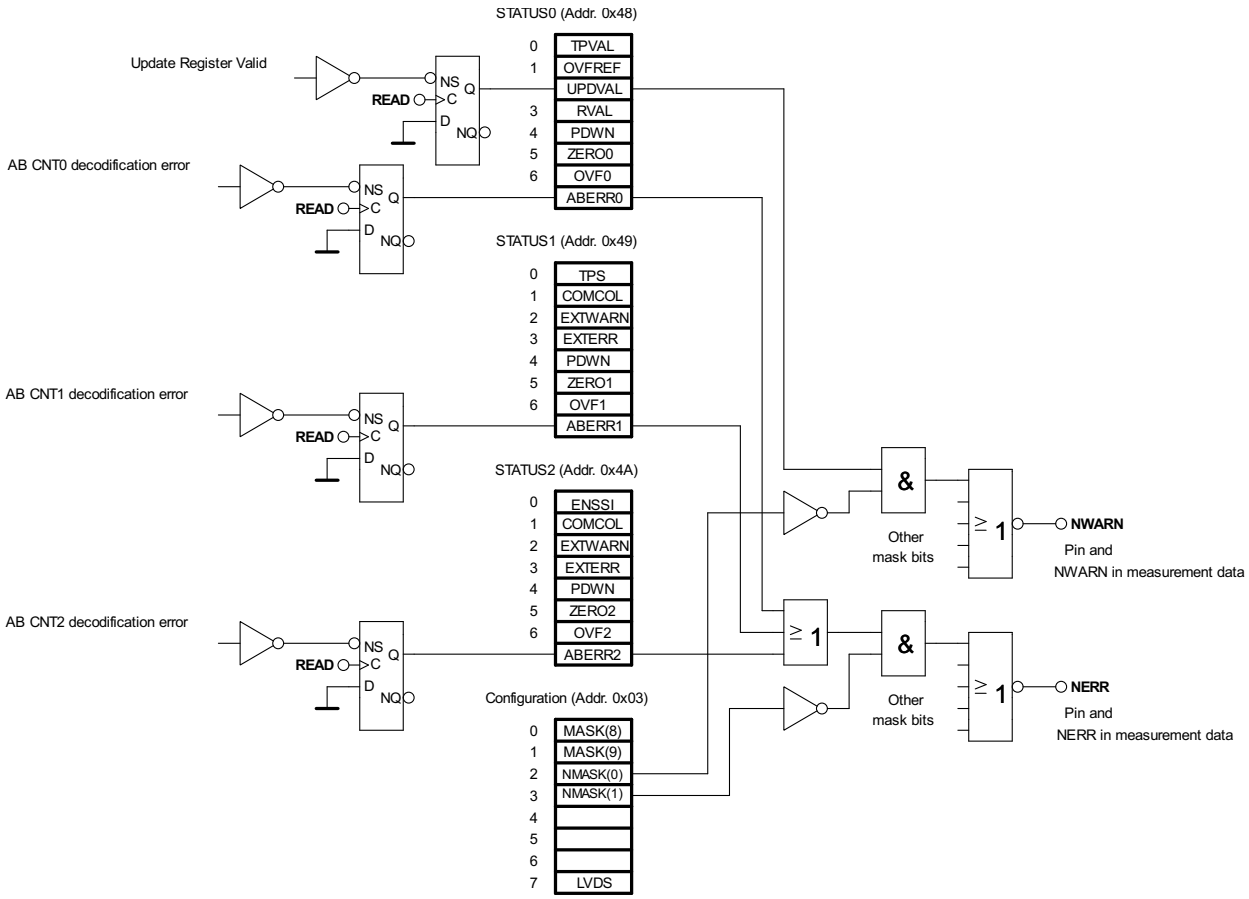


Figure 9: NMASK gating

The latched events are reset with reading the STATUS addresses 0x48, 0x49 or 0x4A unless the event signals do not persist. The read access is indicated by the latch reset signal ”READ”.

MASK	Adr 0x02, bit 7:0; Adr 0x03, bit 1:0 Default = 0x000
Bit	Error/Warning Event
9	enable SSI (warning)
8	external error (error)
7	zero value of active counter 0, 1 or 2 (warning)
6	touch-probe valid (warning)
5*	power down (RAM was initialized) (warning)
4	overflow of reference counter (warning)
3	overflow of counter 0, 1 or 2 (warning)
2	REF reg. valid (warning)
1	external warning (warning)
0	register communication collision (warning)
Notes	encoding of bit 9 . . . 0: 0 = message disabled, 1 = message enabled

Table 57: Error/Warning Event Masks

NMASK	Adr 0x03, bit 3:2 Default = 0b00
Bit	error/warning event
1	AB decodification error. e.g. too high frequency(error)
0	UPD reg. valid (warning)
Notes	encoding of bit 1...0: 0 = message enabled, 1 = message disabled

Table 58: Error/Warning Event Not Masks

SPI INTERFACE

The Serial Peripheral Interface (SPI) of iC-MD consists of a SPI slave interface with polarity 0 and phase 0.

Each transmission starts with a falling edge of NCS and ends with the rising edge. During transmission, commands and data are controlled by SCK and NCS according to the following rules:

- Commands and data are shifted; MSB first, LSB last
- Each output data/status bits are shifted out on the falling edge of SCK (MISO line) and each bit is sampled on the rising edge of SCK (Polarity 0, Phase 0).
- After the device is selected with the falling edge of NCS, an 8-bit command is received. The command defines the operations to be performed (Write/Read) and the address.
- The rising edge of NCS ends all data transfer and resets internal counter and command register
- Data transfer out from MISO starts with the falling edge of SCK immediately after the last bit of the SPI command is sampled in on the rising edge of SCK
- Data transfer to MOSI continues immediately after receiving the command in all cases where data is to be written to iC-MD internal registers
- The SPI interface can not be used for daisy chain setups.

SPI Communication

The first byte to be transmitted to the iC-MD via SPI is the instruction (or command) which determine the communication direction (read or write), and has the following structure:

SPI Commands							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	ADDRESS(6:0)						

Table 59: SPI command structure

The following diagrams show the SPI write and read processes.

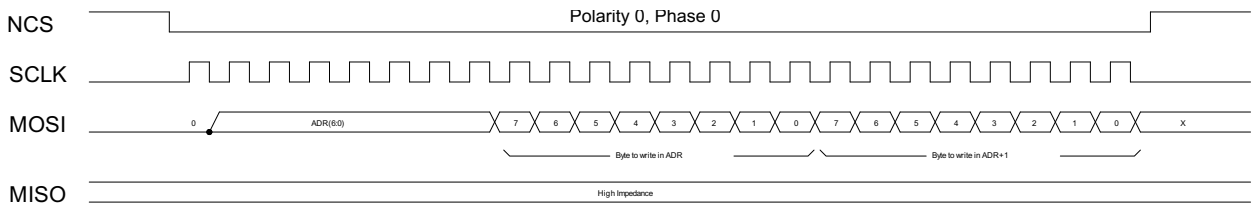


Figure 10: SPI Write Data

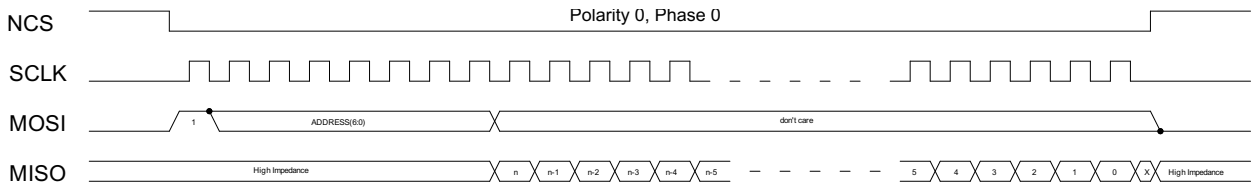


Figure 11: SPI Read Data

The data length to be **written** is always 8 bit, but it is possible to transmit several bytes of data consecutively if the NCS signal is not reset and SCLK continues being clocked. The address transmitted is then the start address which is internally increased by 1 following each transmitted byte.

The data length to be **read** after the read instruction is variable:

Address 0x0A, 0x0C, 0x0E: 24 bit + 2 bit data length
For TP1, TP2 and UPD registers the single SPI read requires a transfer of 26 bit in one sequence.

Example: UPD = 24 bit + NERR + NWARN SPI data access

SPI READ DATA UPD(23:0) + NERR + NWARN								
Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Measurement Data (SPI read only)								
0x0A	UDP(23:16)							
	UDP(15:8)							
	UDP(7:0)							
	NERR	NWARN	0b00.0000					

Table 60: Register layout

Address 0x08: variable data length
For counter data, it depends on the counter configuration CNTCFG (Adr. 0x00 bit (2:0)) how many bits this single transfer needs to clock out. See the table 61. The total length is CNT length + 2 bit (NERR, NWARN). Additional bits may be clocked out as a full byte.

CNTCFG	**Counter Configuration**			**Total CNT length**
0b000	CNT0 = 24 bit			24 bit
0b001	CNT1 = 24 bit	CNT0 = 24 bit		48 bit
0b010	CNT0 = 48 bit			48 bit
0b011	CNT0 = 16 bit			16 bit
0b100	CNT0 = 32 bit			32 bit
0b101	CNT1 = 32 bit		CNT0 = 16 bit	48 bit
0b110	CNT1 = 16 bit	CNT0 = 16 bit		32 bit
0b111	CNT2 = 16 bit	CNT1 = 16 bit	CNT0 = 16 bit	48 bit

Table 61: SPI Counter Data Position

Example: CNT0 = 48 bit + NERR + NWARN SPI data access

SPI READ DATA AB/SPICH(47:0) + NERR + NWARN								
Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Measurement Data (SPI read only)								
0x08	AB/SPICH(47:40) = CNT0(47:40)							
	AB/SPICH(39:32) = CNT0(39:32)							
	AB/SPICH(31:24) = CNT0(31:24)							
	AB/SPICH(23:16) = CNT0(23:16)							
	AB/SPICH(15:8) = CNT0(15:8)							
	AB/SPICH(7:0) = CNT0(7:0)							
	NERR	NWARN	0b00.0000					

Table 62: Register layout

Example: CNT1 = 24 bit + CNT0 = 16 bit + NERR + NWARN SPI data access

SPI READ DATA AB/SPICH(39:0) + NERR + NWARN								
Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Measurement Data (SPI read only)								
0x08	AB/SPICH(39:32) = CNT1(23:16)							
	AB/SPICH(31:24) = CNT1(15:8)							
	AB/SPICH(23:16) = CNT1(7:0)							
	AB/SPICH(15:8) = CNT0(15:8)							
	AB/SPICH(7:0) = CNT0(7:0)							
	NERR	NWARN	0b00.0000					

Table 63: Register layout

Default 8 bit data length on remaining addresses
For configuration data (Adr.- 0x00 to 0x07), REF and SPICH (Adr.- 0x10 to 0x25), ROM (Adr.- 0x42, 0x43) and Status Bit (Adr.- 0x48 to 0x4A). But it is possible to read several bytes of data consecutively if the NCS signal is not reset and SCLK continues being clocked. The address transmitted is then the start address which is internally increased by 1 following each transmitted byte.

BiSS and SSI INTERFACE

The BiSS interface is a bidirectional serial interface, which is used to read out the sensor data values and to write and read the internal configuration registers. For a detailed description of the protocol, see the BiSS C specification.

It consist of 3 configurable channels:

Channel	Data	Error	Warning	Data length	CRC polynomial	CRC mode
CH0	AB counter	NERR	NWARN	16 + 2 bit	1000011	inverted
				24 + 2 bit (default)		
				32 + 2 bit		
				48 + 2 bit		
	SPI Channel	NERR	NSPICHVAL	16 + 2 bit	1000011	inverted
				24 + 2 bit		
				32 + 2 bit		
				48 + 2 bit		
CH1	UPD	NABERR	NUPDVAL	24 + 2 bit	100101	inverted
	TP1	NABERR	NTPVAL	24 + 2 bit	100101	inverted
CH2	TP1	NABERR	NTPVAL	24 + 2 bit	100101	inverted
	TP2	NABERR	NTPVAL	24 + 2 bit	100101	inverted
Notes	channel 0 data length configurable via: CNTCFG (Adr.0x00, bit 3:0)					

Table 64: BiSS Channels

The error (NERR) and warning (NWARN) bit of the channel 0 signal the same data to be output at the pins NERR and NWARN, it's by default:

NERR: ABERR (AB signal error)

NWARN: UPDVAL (UPD Reg. up to date)

This bits can also be configured like the NERR and NWARN outputs, with the registers MASK (table 57) and NMASK(table 58)

Two different data can be selected for each channel, register CHxSEL (table 65) selects the data to be transmitted by the channels.

CHxSEL	Addr. 0x04; bit (7,5,3)	Default = 0b000
Code	Function	
XX0	channel 0: AB counter data	
XX1	channel 0: SPI data channel	
X0X	channel 1: UPD data	
X1X	channel 1: TP1 data	
0XX	channel 2: TP1 data	
1XX	channel 2: TP2 data	

Table 65: BiSS Channel Selection

All three channels are enabled supply data by default configuration, but all of them can be disable with the registers NENCH0 (table 66) and ENCHx (table 67)

NENCH0	Addr. 0x04; bit (2)	Default = 0b0
Code	Function	
0	BiSS channel 0 enabled	
1	BiSS channel 0 disabled	

Table 66: Disable BiSS Channel 0

ENCHx	Addr. 0x04; bit (6,4)	Default = 0b00
Code	Function	
X0	BiSS channel 1 disabled	
0X	BiSS channel 2 disabled	

Table 67: Enable BiSS Channel 1 and 2

N.B. With using BiSS protocol the device provides a BiSS Profile ID 0x33 0x18 (0x33 in address 0x42 and 0x18 in address 0x43) that is a void "BiSS Profile ID".

BiSS Device ID	Addr. 0x78 0x79; bit (7,0)	R
0x78	0x4D = ASCII "M"	
0x79	0x44 = ASCII "D"	

Table 68: BiSS Device ID

BiSS Device ID	Addr. 0x7A. . . 0x7D; bit (7,0)	R
0x7A 0x7B . . . 0x7D	0x5A = ASCII "Z" iC-MD Redesign Z 0x00 = ASCII n.a. (first redesign)	
0x7A 0x7B 0x7C . . . 0x7D	0x5A = ASCII "Z" iC-MD Redesign Z1 0x31 = ASCII "1" 0x00 = ASCII n.a.	
0x7A 0x7B . . . 0x7D	0x59 = ASCII "Y" iC-MD Redesign Y 0x00 = ASCII n.a.	
0x7A 0x7B . . . 0x7D	0x58 = ASCII "X" iC-MD Redesign X 0x00 = ASCII n.a. (latest redesign)	

Table 69: BiSS Device ID, BiSS Device Revision

BiSS Device Manufacturer ID	Addr. 0x7E 0x7F; bit (7,0)	R
0x7E	0x69 = ASCII "i"	
0x7F	0x43 = ASCII "C"	

Table 70: BiSS Device Manufacturer ID

SSI Protocol
An SSI protocol is selected if the input pin SLI is open. This enable signal has an internal digital filter of 25 µs maximum.

A clock pulse train from a controller is used to gate out sensor data. Between each clock pulse train there is a SSI timeout during which fresh data is moved into the register. Data is shifted out when the iC-MD receives a pulse train from the controller. When the least significant bit (LSB) goes high after the SSI timeout, new data is available to read.

The AB counter data transmitted is in the form of a binary code (24 bit + NERR + NWARN). If the input MA continues being clocked without SSI timeout, it will be output a total of 94 bit with the following scheme:

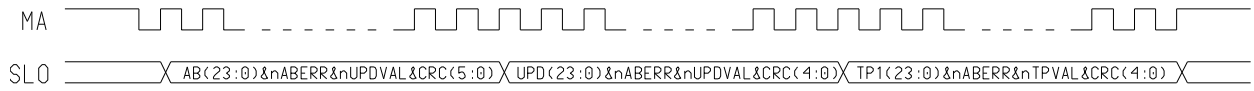


Figure 12: Output data with SSI protocol

INTERFACE PRIORITY

The Configuration bit PRIOR (Adr. 0x03, bit 1), set which interface has priority when taking place a Read-/Write interface collision. It means that if BiSS and SPI try to access to the configuration register at the same time, then only the one with the priority will write/read successfully the register. The error in the interface without priority will be signalized by the collision Status bit: SPICOL or BISSCOL, Adr.0x4A, bit(1:0).

PRIOR	Addr. 0x03; bit 0	Default = 0b0
Code	Function	
0	BiSS priority	
1	SPI priority	

Table 71: SPI Interface Priority

SPI Channel: SPI to BiSS communication
The counter register is also used for the transmission of data from SPI to BiSS. The data exchanging take place as following:

1. SPI writes the data to be transmitted in address 0x20 to 0x25, this data is written in the counter registers. The data length to be transmitted is selected by CNTCFG (Table 13) and can be configured as 16, 24, 32 or 48-bit
2. After the writing process, the bit SPICHVAL is set to 1 and read via BiSS as Warning bit of channel 0.
3. BiSS reads out the channel 0, the data written via SPI and two status bits, NERR and NWARN which indicates if the read data is valid.

ACTUATOR OUTPUTS, ERROR and WARNING I/O PINS

The pins NERR and NWARN are low active bidirectional ports (open collector outputs and digital inputs).

The inputs are used to latch an external error/warning (tables 52 and 53) and makes possible that this error/warning will be read by the controller via SPI or BiSS as status bits.

The instruction bits ACT0 and ACT1 (tables 42 and 43) set the value of the output pins ACT0 and ACT1.

APPLICATIONS NOTES

RS422 12 V capable inputs setup

The following figure 13 shows the resistors configuration used for a 12 V capable RS422 inputs. (see Fig. 13).

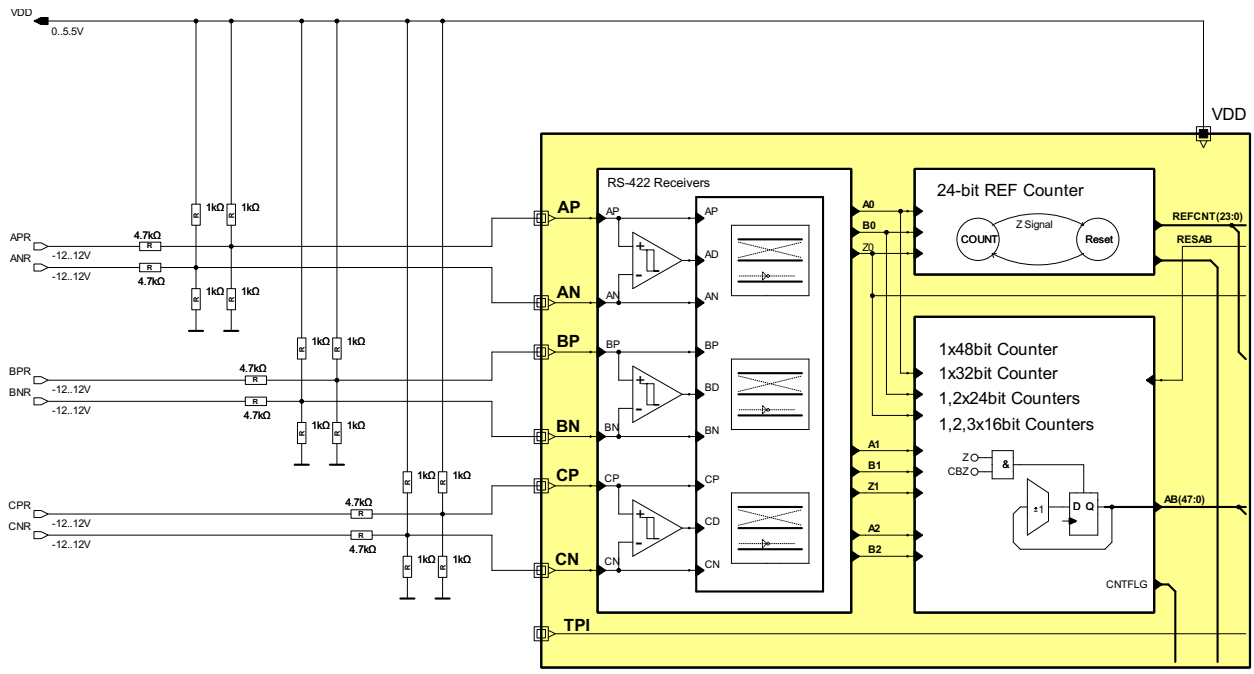


Figure 13: RS422 12 V capable configuration

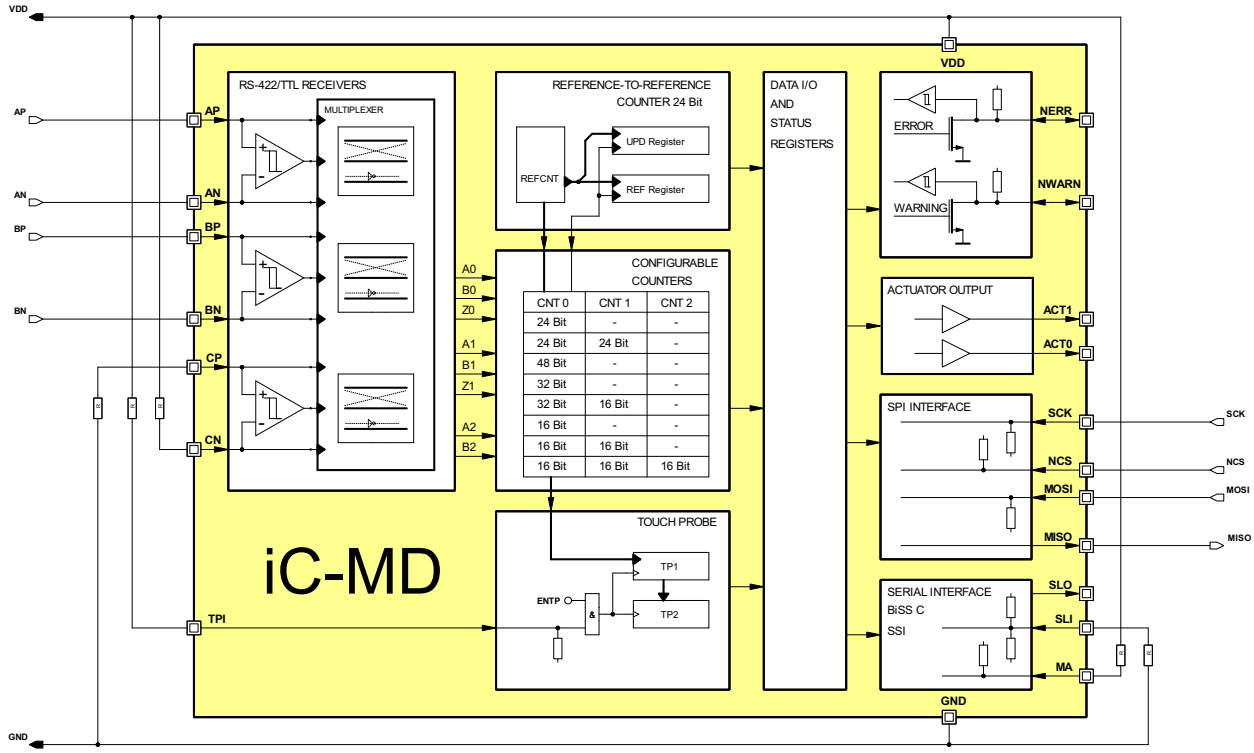


Figure 14: SPI only operation with unused constant pulled index input

Optional ”SPI only” operation setup
Figure 14 shows an SPI only configuration. All trigger events or status requests need to be accessed over the SPI interface.

- Default State of the BiSS Interface
  - Pull up resistor on input pin MA
  - Pull down resistor on input pin SLI
- On unused pin TPI:
  - Pull up resistor on input pin TPI

Optional unused index setup
Figure 14 shows a deactivated index input pins biasing for CP CN on differential input signals. The logic state of the index input is then 0.

- On unused counter pins CP CN with RS-422 receiver setup:
  - Pull down resistor on the positive input pin CP
  - Pull up resistor on the positive input pin CN
  - Consider INVZ0 = 0 signal configuration
  - Consider CFGZ = 0 signal configuration
- On unused counter pins with TTL/CMOS receiver setup:
  - Pull down resistor on input pin BP and CN
  - Consider INVZx = 0 signal configuration
  - Consider CFGZ = 0 signal configuration

DESIGN REVIEW: Notes On Chip Functions

iC-MD X		
No.	Function, Parameter/Code	Description and Application Hints
1		No further notes at time of printing.

Table 72: Notes on chip functions regarding iC-MD chip release X.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2010-11-02		Initial release	all

Rel.	Rel. Date*	Chapter	Modification	Page
A2	2012-02-22		Tables added, more detailed explanations	n.a.

Rel.	Rel. Date*	Chapter	Modification	Page
A3	2013-03-04		New title: 48-BIT QUADRATURE COUNTER	1
		DESCRIPTION	BUA info added	2
		REVISION HISTORY	REVISION HISTORY added	26

Rel.	Rel. Date*	Chapter	Modification	Page
A4	2015-02-18	STATUS REGISTER and ERROR/WARNING INDICATION	MASK and NMASK figures added	20, 21

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2017-3-30	ELECTRICAL CHARACTERISTICS	item 004, 201, 604 and C01 updated	5, 6
		ELECTRICAL CHARACTERISTICS	ENSSI replaces ENBISS, item i107 -113 removed, figure 4 removed, operating conditions updated,	8
		REGISTER MAP	Added ”SPI and BiSS read only”	10
		COUNTER CONFIGURATION	Table 13 address bits (2:0) updated	12
		BiSS and SSI INTERFACE	BiSS identifier details added	26
		BiSS and SSI INTERFACE	Table 70 updated 0x7E 0x7F for BiSS Device Manufacturer	26
		INTERFACE PRIORITY	Table 71 address bit (0) updated	26
		REVISION HISTORY	REVISION HISTORY updated	29

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* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-MD	TSSOP20		iC-MD TSSOP20
Evaluation Board iC-MD	100 mm x 80 mm PCB		iC-MD EVAL MD1D

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