

iC-JX

16-FOLD 24 V HIGH-SIDE DRIVER WITH μ C INTERFACE



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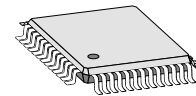
FEATURES

- 16 bidirectional input/output stages at 24 V
- Input/output mode programmable in 4-channel blocks
- Short-circuit-proof high-side drivers with diagnosis function
- 500 mA pulse and 150 mA permanent load driving capability
- Active flyback circuit
- Load diagnosis for driver current, output voltage and impedance (cable fractures, resistance and short circuits)
- 10-bit A/D converter for the generation of diagnosis measurement values
- Safety devices (voltage monitor, temperature sensor with warning and shutdown features, power output enable pin)
- Programmable interrupt generation with an events storage facility
- Variable digital filters for the debouncing of I/O signals
- Fast 8-bit parallel or serial SPI™-compatible μ C interface permits use in buses
- Logic supply from 3 V upwards

APPLICATIONS

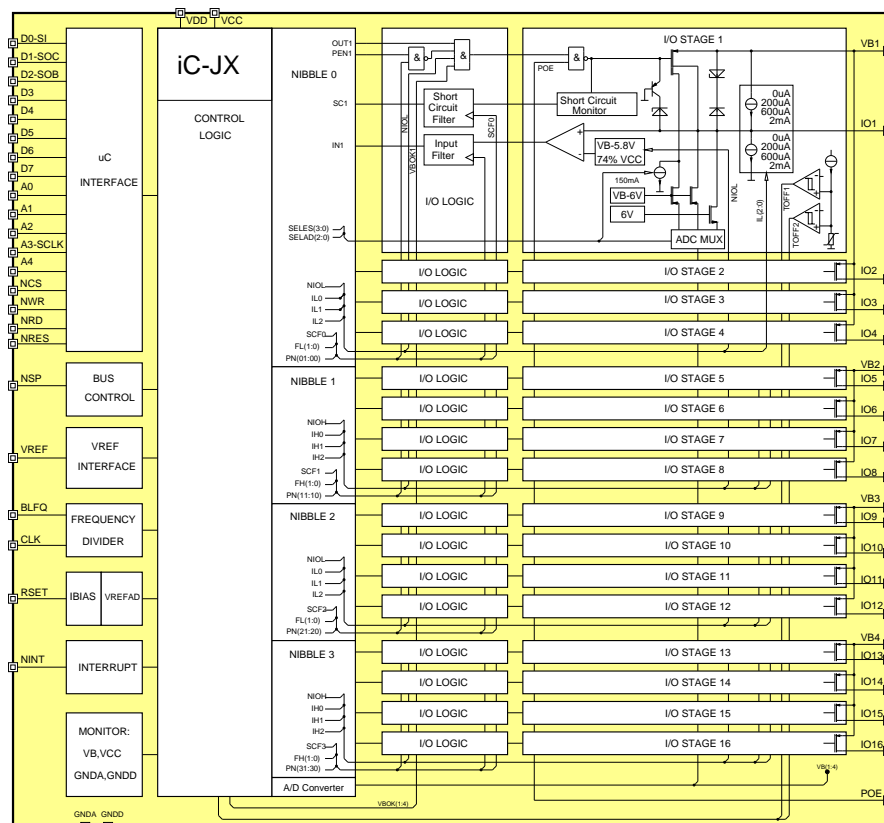
- Industrial 24 V applications
- Lamp switches with diagnostic features
- Inductive load driver circuits for relays and valves etc.

PACKAGES



MQFP52

BLOCK DIAGRAM



DESCRIPTION

iC-JX is a bidirectional I/O device with 4x4 high-side driver stages. The input or output function can be separately selected for blocks or nibbles of four I/O stages.

Each block can also be individually programmed with various filtering options for the debouncing of I/O pin signals or overcurrent messages, with current sources for the defining of levels at the inputs (low-side sources) or for load diagnosis at the outputs (high-side sources) and also with a flash pulse function.

To enable communication with the controller the device includes a parallel interface (with eight data, five address and three control pins) and also an SPI-compatible serial interface (with one pin for the clock, chip selection, data input and data output respectively). The type of interface is selected via pin NSP.

I/O stages with an input function can record logic levels at 24 V where a programmable pull-down current source (of up to 2 mA) either defines the level for open inputs or supplies a bias current for external switch contacts. Connecting safety circuits with integrated serial/parallel resistors to the device also enables leakage currents and short circuits to be pinpointed. The contact status can be read out using the microcontroller interface.

I/O stages with an output function drive various loads (such as lamps, cables or relays, for example) to a common ground with 150 mA of permanent current or 500 mA in pulse operation. Spikes and flyback currents are discharged by the integrated flyback circuits.

For synchronous flash display, as used for indicator lamps in plugboards, for example, a flash pulse enable can be individually set for each output to offload the controller. A common inhibiting input (POE) permits the global shutdown of all outputs and can be operated by an autonomous watchdog circuit.

All output stages are short-circuit-proof and protected against thermal destruction in the event of extreme power dissipation. Each stage has its own temperature sensor which is evaluated in two stages

and generates interrupt messages for the controller. The latter is warned before the device is forcibly shut-down. A short circuit also triggers an interrupt message; the current status here can be read out by the controller.

For the purpose of load diagnosis a programmable pull-up current source (of up to 2 mA) can be used to determine an initial load breakage or open loop (caused by a fractured cable, for example) before an output is switched on. The I/O pin status can always be read back via comparators. A load current measurement circuit then permits the load to be assessed; failed valves and faulty or wrongly implemented indicator lamps can be verified in this way. In addition, the analog measurement of voltage at the I/O pins allows safety switches to be analyzed with reference to ground, here without the driver function.

All analog measurements for the load current (per stage), for the I/O pin voltage (per stage, either referenced to Ground or VB), for the driver supply (all VB pins), for the internal voltage reference (VBG) and for the chip temperature are made available to the microcontroller as digital measurements by an integrated A/D converter which has 10 bits of resolution.

An interrupt pipeline which limits the loss of interrupts allows reliable processing of interrupts by the microcontroller. Registers provide information as to current events; messages can be individually enabled for all available interrupt sources.

iC-JX monitors all supply voltages and also the GNDD-GNDA connection to ground.

Monitored separately, undervoltage in the range of 2.5V at analog supply VCC or even short disruption of digital supply VDD causes all registers to be reset and the output stages to be shutdown.

Undervoltage at 24 V driver supply VB triggers a shutdown of the output stages without deleting the contents of the registers.

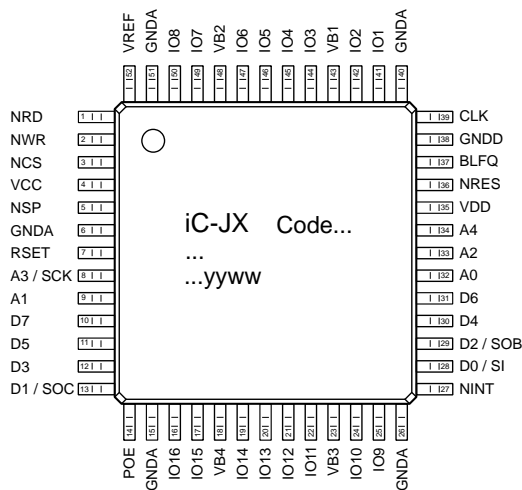
Diodes protect all inputs and outputs against destruction by ESD. iC-JX is also immune to burst transients according to IEC 1000-4-4 (4 kV; previously IEC 801-4).

PACKAGES MQFP52 to JEDEC Standard

PIN CONFIGURATION

MQFP52, pitch 0.65 mm

Orientation of the package label (Ⓢ JX code...) is subject to change.



PIN FUNCTIONS

No. Name Function

1	NRD	Not Read Enable
2	NWR	Not Write Enable
3	NCS	Not Chip Select
4	VCC	Supply Voltage (analog, 3...5.5 V)
5	NSP	Not Serial / Parallel (Mode)
6	GNDA	Ground (analog)
7	RSET	Resistor Setting (10 k Ω optional)
8	A3	Adress Bus
9	A1	Adress Bus
10	D7	Data Bus
11	D5	Data Bus
12	D3	Data Bus
13	D1	Data Bus
14	POE	Power Output Enable
15	GNDA	Ground (analog)
16	IO16	I/O Stage
17	IO15	I/O Stage
18	VB4	Supply Voltage for I/O Stages 13...16
19	IO14	I/O Stage
20	IO13	I/O Stage
21	IO12	I/O Stage

PIN FUNCTIONS

No. Name Function

22	IO11	I/O Stage
23	VB3	Supply Voltage for I/O Stages 9...12
24	IO10	I/O Stage
25	IO9	I/O Stage
26	GNDA	Ground (analog)
27	NINT	Not Interrupt
28	D0	Data Bus
29	D2	Data Bus
30	D4	Data Bus
31	D6	Data Bus
32	A0	Address Bus
33	A2	Address Bus
34	A4	Address Bus
35	VDD	Supply Voltage (logic, 3...5.5 V)
36	NRES	Not Reset
37	BLFQ	Blink Frequency
38	GNDD	Ground (logic)
39	CLK	Clock (optional)
40	GNDA	Ground (analog)
41	IO1	I/O Stage
42	IO2	I/O Stage
43	VB1	Supply Voltage for I/O Stages 1...4
44	IO3	I/O Stage
45	IO4	I/O Stage
46	IO5	I/O Stage
47	IO6	I/O Stage
48	VB2	Supply Voltage for I/O Stages 5...8
49	IO7	I/O Stage
50	IO8	I/O Stage
51	GNDA	Ground (analog)
52	VREF	External Voltage Reference (optional)

*Additional Pin Function in SPI Mode
(NSP = low)*

3	NCS	Not Chip Select
8	SCK	Serial Clock
9	A1	Device ID Bit 1
13	SOC	Serial Out Chain
28	SI	Serial In
29	SOB	Serial Out Bus
32	A0	Device ID Bit 0
33	A2	Select Chain / Bus
34	A4	Enable Interrupt Report SOC/SOB

Separate supply voltages at VB1..4 are possible. All GNDA pins must be connected up externally. GNDA must be connected to GNDD externally when just one voltage supply is available. VCC and VDD can be powered either mutually or separately.

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed. Absolute Maximum Ratings are no Operating Conditions. Integrated circuits with system interfaces, e.g. via cable accessible pins (I/O pins, line drivers) are per principle endangered by injected interferences, which may compromise the function or durability. The robustness of the devices has to be verified by the user during system development with regards to applying standards and ensured where necessary by additional protective circuitry. By the manufacturer suggested protective circuitry is for information only and given without responsibility and has to be verified within the actual system with respect to actual interferences.

(Legend: x = 1..16, y = 1..4)

Item No.	Symbol	Parameter	Conditions	Min. Max.		Unit
				Min.	Max.	
G001	VCC, VDD	Supply Voltage		-0.3	6	V
G002	VBy	Driver Supply Voltage		-0.3	40	V
G003	V(IOx)	Voltages at IO1...16	IOx = off; see additional remark ¹	-10	40	V
G004	Idc(IOx)	Current in IO1...16	see Figure 1	-500	150	mA
G005	Ipk(IOx)	Pulse current in IO1...16	IOx = hi, $\tau = 2$ ms, $T \leq 2$ s see Figure 2	-1.0		A
G006	I _{max} ()	Current in VCC, VDD		-100	100	mA
G007	I _{max} (VBy)	Current in VB1...4		-8	8	A
G008	Ic()	Current in NCS, NWR, NRD, A0...4, D0...7, NRES, CLK, BLFQ, POE, NSP, RSET, VREF	D0...7 with input function	-20	20	mA
G009	I()	Current in D0...7, NINT,	D0...7 with output function	-25	25	mA
G010	I _{lu} ()	Pulse current in NCS, NWR, NRD, A0...4, D0...7, NRES, CLK, BLFQ, NINT, NSP, POE, IO1...16, RSET, VREF (latch up test)	Pulse width < 10 μ s, all inputs / outputs open	-100	100	mA
G011	Vd()	ESD-voltage, all pins	HBM 100 pF discharged over 1.5 k Ω		2	kV
G012	Vb()	Burst transients at IO1...16	after IEC 1000-4-4		4	kV
G013	T _j	Chip temperature		-40	150	$^{\circ}$ C
G014	T _s	Storage temperature		-40	150	$^{\circ}$ C

¹⁾ If the voltage supplies can not be guaranteed to be present at the time signals appear at the pins IO1..IO16, additional diodes or sufficient current limiting ohmic resistors have to be connected in series to the IO-pins to prevent reverse back biasing of the device.

THERMAL DATA

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, all inputs on defined logic states (high or low)

Item No.	Symbol	Parameter	Conditions	Min. Typ. Max.			Unit
				Min.	Typ.	Max.	
T01	Ta	Ambient temperature	extended temperature range on request	-40		85	$^{\circ}$ C
T02	Rthja	Thermal resistance chip/ambient	package mounted on PCB		55		K/W

ELECTRICAL CHARACTERISTICS

Operating conditions: $V_{CC} = V_{DD} = 3 \dots 5.5 \text{ V}$, $V_{By} = 12 \dots 36 \text{ V}$, $G_{NDA} = G_{NDD} = 0 \text{ V}$, $R_{SET} = 10 \text{ k}\Omega \pm 1\%$. All inputs on defined logic states (high or low), $T_j = -40 \dots 125 \text{ }^\circ\text{C}$ unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VCC	Permissible Supply Voltage VCC		3		5.5	V
002	I(VCC)	Supply Current in VCC			10	20	mA
003	I(VCC)	Supply Current in VCC	no supply voltage VBy			30	mA
004	VDD	Permissible Supply Voltage VDD		3		5.5	V
005	I(VDD)	Supply Current in VDD (static)	all logic inputs lo = 0 V or hi=VDD		3	6	mA
006	I(VDD)	Supply Current in VDD (dynamic)	continuous reading cycle all 200ns, data word '00' and 'FF' is alternating read, CL(D0... 7) = 200 pF			30	mA
007	I(VDD)	Supply Current in VDD	all logic inputs lo=0.8V		3		mA
008	I(VDD)	Supply Current in VDD	all logic inputs hi=2.0V		5		mA
009	VBy	Permissible Supply Voltage VB1...4 (operating range)		12		36	V
010	I(VBy)	Supply Current in VB1...4	POE = hi, IOx = hi, unbelastet		7	20	mA
011	I(VBy)	Supply Current in VB1...4	IOx = off		5	10	mA
012	Vc(lo)	ESD Clamp Voltage lo at VCC, VDD, VB1...4, RSET, VREF	I() = -10 mA	-1.4		-0.3	V
013	Vc(hi)	ESD Clamp Voltage hi at VCC, VDD	I() = 10 mA	6			V
014	Vc(hi)	ESD Clamp Voltage hi at VB1...4	I() = 10 mA	30		55	V
015	Vc(lo)	ESD Clamp Voltage lo at IO1...16	I() = 10 mA, IOx = off	-25		-19	V
016	Vc(lo)	ESD Clamp Voltage hi at IO1...16	I() = 10 mA	30		55	V
017	Vc(hi)	ESD Clamp Voltage hi at NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NINT, POE, NSP	Vc(hi) = V() - VDD, D0...7 as input, I() = 10 mA	0.4		1.5	V
018	Vc(lo)	ESD Clamp Voltage lo at NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NINT, POE, NSP	D0...7 as input, I() = -10 mA	-1.5		-0.4	V
019	I _{fl} (IOx)	Leakage Current of I/O Pins (x=1..16) beyond operating conditions	VCC = 0 V and VDD = 0 V, VBy = 2..30 V)	-0.2			mA
I/O Stages: High-Side Driver IO1...16							
101	Vs(hi)	Saturation Voltage hi	Vs(hi) = VBy - V(IOx), I(IOx) = -15 mA; see Fig. 1			0.2	V
102	Vs(hi)	Saturation Voltage hi	Vs(hi) = VBy - V(IOx), I(IOx) = -150 mA; see Fig. 1			0.6	V
103	Vs(hi)	Saturation Voltage hi for pulse load	Vs(hi) = VBy - V(IOx), I(IOx) = -500 mA, $\tau = 2 \text{ ms}$, $T \leq 2 \text{ s}$; see Fig. 2			2	V
104	Isc(hi)	Overcurrent Cut-off	V(IOx) = 0 .. VBy - 3 V	-1.6		-0.51	A
105	It(jscs)	Threshold Current for Overcurrent Message		-1.2		-0.51	A
106	Vc(lo)	Free-wheeling Clamp Voltage low	I(IOx) = -150 mA	-18		-12	V
107	SR(hi)	Slew Rate hi	CL = 0 ... 100 pF, I(IOx) = -150 mA	5		17	V/ μ s

ELECTRICAL CHARACTERISTICS

Operating conditions: $V_{CC} = V_{DD} = 3 \dots 5.5 \text{ V}$, $V_{By} = 12 \dots 36 \text{ V}$, $G_{NDA} = G_{NDD} = 0 \text{ V}$, $R_{SET} = 10 \text{ k}\Omega \pm 1\%$. All inputs on defined logic states (high or low), $T_j = -40 \dots 125 \text{ }^\circ\text{C}$ unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
108	SR() _{lo}	Slew Rate _{lo}	$CL = 0 \dots 100 \text{ pF}$, $I(\text{IOx}) = -150 \text{ mA}$	5		17	V/ μ s
109	tp _{lh} ()	Propagation Delay until IOx: _{lo} \rightarrow _{hi}	$V(\text{IOx}) > V_0(\text{IOx}) + 1 \text{ V}$			6	μ s
110	tph() _{lo}	Propagation Delay until IOx = off	$V(\text{IOx}) < 80 \% (V_{By} - V_s(\text{IOx})_{hi})$			6	μ s
I/O Stages: Current Sources at IO1...16							
201	l _{pd} ()	Pull-down Current Source (200 μ A)	$V(\text{IOx}) = 3 \text{ V} \dots V_{By}$;	160	200	240	μ A
202	l _{pd} ()	Pull-down Current Source (600 μ A)	$V(\text{IOx}) = 3 \text{ V} \dots V_{By}$;	510	600	690	μ A
203	l _{pd} ()	Pull-down Current Source (2 mA)	$V(\text{IOx}) = 3 \text{ V} \dots V_{By}$;	1.6	2	2.4	mA
204	l _{pu} ()	Pull-up Current Source (200 μ A)	IOx = off, $V(\text{IOx}) = 0 \text{ V} \dots V_{By} - 3 \text{ V}$	150	200	250	μ A
205	l _{pu} ()	Pull-up Current Source (600 μ A)	IOx = off, $V(\text{IOx}) = 0 \text{ V} \dots V_{By} - 3 \text{ V}$	510	600	690	μ A
206	l _{pu} ()	Pull-up Current Source (2 mA)	IOx = off, $V(\text{IOx}) = 0 \text{ V} \dots V_{By} - 3 \text{ V}$	1.6	2	2.4	mA
207	tp() _{lon}	Turn-on Time Current Source aktiv	$I(\text{IOx}) > 90 \% I_{pd}(\text{IOx})$ resp. $I(\text{IOx}) > 90 \% I_{pu}(\text{IOx})$			5	μ s
208	tp() _{loff}	Turn-off Time Current Source inaktiv	$I(\text{IOx}) < 10 \% I_{pd}(\text{IOx})$ resp. $I(\text{IOx}) < 10 \% I_{pu}(\text{IOx})$			5	μ s
209	l _{fu} ()	Leakage Current	IOx with Input Function or Output Function with IOx = off; $V_{By} = 30 \text{ V}$ $I_{L2} = I_{H2} = I_{L1} = I_{H1} = I_{L0} = I_{H0} = 0$, $V(\text{IOx}) = 0 \text{ V} \dots V_{By}$	-50		70	μ A
210	l _{rb} ()	Leakage Current	Conditions see Item-No. 209; $V(\text{IOx}) = -10 \text{ V} \dots 0 \text{ V}$, $V_{By} = 30 \text{ V}$	-1.5			mA
211	l _{rb} ()	Leakage Current	Conditions see Item-No. 209; only Input Function $V(\text{IOx}) = V_{By} \dots V_{By} + 0.3 \text{ V}$			250	μ A
212	l _{rb} ()	Leakage Current	Conditions see Item-No. 209; only Input Function $V(\text{IOx}) = V_{By} + 0.3 \text{ V} \dots V_{By} + 2 \text{ V}$			1	mA
213	l _{rb} ()	Leakage Current	no supply voltages V_{By} $V(\text{IO})_{\text{max}} = 36 \text{ V}$			5	mA
I/O Stages: Comparator IO 1..16							
301	V _t () _{hi}	Threshold voltage hi	IOx with input function			82	%VCC
302	V _t () _{lo}	Threshold voltage lo	IOx with input function	66			%VCC
303	V _t () _{hys}	Hysteresis	IOx with input function, $V_t(\text{hys}) = V_t(\text{hi}) - V_t(\text{lo})$	100			mV
304	V _t () _{hi}	Threshold voltage hi referenced to V_{By}	IOx with output function, $V_t(\text{hi}) = V_{By} - V(\text{IOx})$	5.0			V
305	V _t () _{lo}	Threshold voltage lo referenced to V_{By}	IOx with output function, $V_t(\text{lo}) = V_{By} - V(\text{IOx})$			6.7	V
306	V _t () _{hys}	Hysteresis	IOx with output function, $V_t(\text{hys}) = V_t(\text{lo}) - V_t(\text{hi})$	100			mV
307	tp(IOx-Dx)	Propagation Delay Input IOx to Data Output Dx	I/O-Filter inactive			20	μ s
Thermal Shutdown							
401	T _{off} 1	Overtemperatur threshold level 1: warning		120		145	$^\circ\text{C}$
402	T _{on} 1	Level 1 Release		115		140	$^\circ\text{C}$
403	T _{hys} 1	Level 1 Hysteresis	$T_{hys1} = T_{off1} - T_{on1}$	2		7	$^\circ\text{C}$
404	T _{off} 2	Overtemperatur threshold level 2: shutdown		140		165	$^\circ\text{C}$
405	T _{on} 2	Level 2 Release		120		145	$^\circ\text{C}$
406	T _{hys} 2	Level 2 Hysteresis	$T_{hys2} = T_{off2} - T_{on2}$	13		35	$^\circ\text{C}$
407	ΔT	Temperature Difference Level 2 to Level 1	$\Delta T = T_{off2} - T_{off1}$	13		35	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 k Ω \pm 1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
Bias and Low Voltage Detection							
501	VCCon, VDDon	Turn-on Threshold VCC, VDD (Power-on release)		2.4	2.6	2.9	V
502	VCCoff, VDDoff	Undervoltage Threshold VCC, VDD (Power-down reset)		2.3	2.5	2.8	V
503	VCChys, VDDhys	Hysteresis	VCChys = VCCon - VCCoff, VDDhys = VDDon - VDDoff	60	100	140	mV
504	tmin()lv	Power Down Time required for low voltage detection	VCC = 0.8 V .. VCCoff, VDD = 0.8 V .. VDDoff	1			μ s
505	tpoff	Propagation Delay until Reset after Low Voltage at VCC, VDD				12	μ s
506	Vrefad	Reference Voltage for A/D-Converter		2.6	2.75	3.0	V
A/D-Converter							
701	VR1	ADC - Measurement Range 1	Current and voltage measurement High at IO, SELAD = '0b001' resp. '0b010', EME = 0	VBy - 0.6 V		VBy	V
702	VR2	ADC - Measurement Range 2	Voltage measurement High at IO, SELAD = '0b010', EME = 1	VBy - 5V		VBy	V
703	VR3	ADC - Measurement Range 3	Voltage measurement Low at IO, SELAD = '0b100', EME = 0	0		0.6	V
704	VR4	ADC - Measurement Range 4	Voltage measurement Low at IO SELAD = '0b100'; VB or VBG measurement SELAD = '0b101' or. '0b110', EME = 1	0		5	V
705	VR5	ADC - Measurement Range 5	Total voltage measurement range SELAD = '0b011'	0		VB	V
706	VR6	ADC - Measurement Range 6	Temperature measurement SELAD = '0b111'	-40		125	°C
707	Vbitlo	Bit-Equivalent of voltage	EME = 0		0.6		mV
708	Vbithi	Bit-Equivalent of voltage	EME = 1		5.4		mV
709	Dtemp1	Digital value of temperature measurement 1	SVREF = 0, TEMP = (774-Dtemp1)/TKtemp1 Tj = -40°C Tj = 27°C Tj = 95°C	826 670 519	863 712 563	900 755 608	
710	TKtemp1	Temperature coefficient 1	SVREF = 0	2.16	2.22	2.27	1/°C
711	Dtemp2	Digital value of temperature measurement 2	SVREF = 1, V(VREF) = 2.5V \pm 0.2% TEMP = (861-Dtemp2)/TKtemp2 Tj = -40°C Tj = 27°C Tj = 95°C	931 761 585	957 800 632	984 839 679	
712	TKtemp2	Temperature coefficient 2	SVREF = 1, V(VREF) = 2.5V \pm 0.2%	2.26	2.41	2.55	1/°C
713	f _{ICLK}	Internal oscillating frequency		0.9	1.25	1.5	MHz
714	t _{SAR1}	Conversion time SAR-converter 1	Current measurement SELAD = '0b001'		154 / f _{ICLK}		μ s
715	t _{SAR2}	Conversion time SAR-converter 2	Voltage measurement Low resp. High; SELAD = '0b010' resp. '0b100'		90 / f _{ICLK}		μ s
716	t _{SAR3}	Conversion time SAR-converter 3	Total voltage measurement SELAD = '0b011'; VBy voltage measurement SELAD = '0b101'; VBG voltage measurement SELAD = '0b110'; temperature measurement SELAD = '0b111'		26 / f _{ICLK}		μ s
717	D _{VBG,1}	Digital value of VBG measurement (external reference)	SELAD = '0b110', SVREF = 1	480	520	560	
718	D _{VBY,1}	Digital value of VBy measurement (external reference)	SVREF = 1, V(VBy) = 36 V, SELAD = '0b101'	940	990	1022	
719	DR _{VBY,1}	Relative value of VBy measurement (external reference)	SVREF = 1; DR _{VBY,1} = D _{VBY,1} (V) / D _{VBY,1} V(VBy) = 24 V, SELAD = '0b101' V(VBy) = 12 V, SELAD = '0b101'	64.6 31.3	66.6 33.3	68.6 35.2	% %

ELECTRICAL CHARACTERISTICS

Operating conditions: $V_{CC} = V_{DD} = 3 \dots 5.5 \text{ V}$, $V_{By} = 12 \dots 36 \text{ V}$, $GNDA = GNDD = 0 \text{ V}$, $R_{SET} = 10 \text{ k}\Omega \pm 1\%$. All inputs on defined logic states (high or low), $T_j = -40 \dots 125 \text{ }^\circ\text{C}$ unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
720	$D1_{IO,1}$	Digital value using VR1 range (external reference)	$SELAD = '0b010'$, $EME = '0b0'$, $SVREF = 1$, $V(IOx) = V(VBy) - 0.6 \text{ V}$	840	900	1022	
721	$DR1_{IO,1}$	Digital relative value using VR1 range (external reference)	$SELAD = '0b010'$, $EME = '0b0'$, $SVREF = 1$; $DR1_{IO,1} = D1_{IO,1}(V) / D1_{IO,1}$; $V(IOx) = V(VBy) - 0.3 \text{ V}$ $V(IOx) = V(VBy) - 0.1 \text{ V}$	46 12	49 15	52 18	% %
722	$D2_{IO,1}$	Digital absolute value using VR2 range (external reference)	$SELAD = '0b010'$, $EME = '0b1'$, $SVREF = 1$, $V(IOx) = V(VBy) - 5.0 \text{ V}$	870	930	1022	
723	$DR2_{IO,1}$	Digital relative value using VR2 range (external reference)	$SELAD = '0b010'$, $EME = '0b1'$, $SVREF = 1$; $DR2_{IO,1} = D2_{IO,1}(V) / D2_{IO,1}$; $V(IOx) = V(VBy) - 2.5 \text{ V}$ $V(IOx) = V(VBy) - 0.6 \text{ V}$	48 9.5	50 11.5	52 14	% %
724	$D3_{IO,1}$	Digital absolute value using VR3 range (external reference)	$SELAD = '0b100'$, $EME = '0b0'$, $SVREF = 1$, $V(IOx) = 0.6 \text{ V}$;	880	940	1022	
725	$DR3_{IO,1}$	Digital relative value using VR3 range (external reference)	$SELAD = '0b100'$, $EME = '0b0'$, $SVREF = 1$; $DR3_{IO,1} = D3_{IO,1}(V) / D3_{IO,1}$; $V(IOx) = 0.3 \text{ V}$ $V(IOx) = 0.1 \text{ V}$	48 14.5	50 16	52 18.5	% %
726	$D4_{IO,1}$	Digital absolute value using VR4 range (external reference)	$SELAD = '0b100'$, $EME = '0b1'$, $SVREF = 1$; $V(IOx) = 5.0 \text{ V}$	870	930	1022	
727	$DR4_{IO,1}$	Digital relative value using VR4 range (external reference)	$SELAD = '0b100'$, $EME = '0b1'$, $SVREF = 1$; $DR4_{IO,1} = D4_{IO,1}(V) / D4_{IO,1}$ $V(IOx) = 2.5 \text{ V}$ $V(IOx) = 0.6 \text{ V}$	48 9.5	50 11.5	52 14	% %
728	$D5_{IO,1}$	Digital absolute value using VR5 range (external reference)	$SELAD = '0b011'$, $SVREF = 1$, $V(IOx) = 36.0 \text{ V}$	930	980	1022	
729	$DR5_{IO,1}$	Digital relative value using VR5 range (external reference)	$SELAD = '0b011'$, $SVREF = 1$; $DR5_{IO,1} = D5_{IO,1}(V) / D5_{IO,1}$ $V(IOx) = 24.0 \text{ V}$ $V(IOx) = 5.0 \text{ V}$	64.6 11.8	66.6 13.8	68.6 15.8	% %
730	$DC_{IO,1}$	Digital value of current measurement (external reference)	$SELAD = '0b001'$, $SVREF = 1$, $I(IOx) = 150 \text{ mA}$	700	800	1022	
731	$DRC_{IO,1}$	Relative value of current measurement (external reference)	$SELAD = '0b001'$, $SVREF = 1$; $DRC_{IO,1} = DC_{IO,1}(I) / DC_{IO,1}$ $I(IOx) = 75 \text{ mA}$ $I(IOx) = 15 \text{ mA}$	48 6.2	51 9.2	54 12.2	% %
732	$D_{VBy,0}$	Digital value of VBG measurement (internal reference)	$SELAD = '0b110'$, $SVREF = 0$	435	460	485	
733	$D_{VBy,0}$	Digital value of VBG measurement (internal reference)	$SVREF = 0$, $V(VBy) = 36 \text{ V}$, $SELAD = '0b101'$	830	880	1022	
734	$DR_{VBy,0}$	Relative value using VR1 range (internal reference)	$SVREF = 0$, $SELAD = '0b101'$; $DR_{VBy,0} = D_{VBy,0}(V) / D_{VBy,0}$ $V(VBy) = 24 \text{ V}$ $V(VBy) = 12 \text{ V}$	64.6 31.3	66.6 33.3	68.6 35.3	% %
735	$D1_{IO,0}$	Digital value using VR1 range (internal reference)	$SELAD = '0b010'$, $EME = '0b0'$, $SVREF = 0$, $V(IOx) = V(VBy) - 0.6 \text{ V}$	760	820	1022	
736	$DR1_{IO,0}$	Relative value using VR1 range (internal reference)	$SELAD = '0b010'$, $EME = '0b0'$, $SVREF = 0$; $DR1_{IO,0} = D1_{IO,0}(V) / D1_{IO,0}$ $V(IOx) = V(VBy) - 0.3 \text{ V}$ $V(IOx) = V(VBy) - 0.1 \text{ V}$	46 12	49 15	52 18	% %
737	$D2_{IO,0}$	Digital value using VR2 range (internal reference)	$SELAD = '0b010'$, $EME = '0b1'$, $SVREF = 0$, $V(IOx) = V(VBy) - 5.0 \text{ V}$	790	840	1022	
738	$DR2_{IO,0}$	Relative value using VR2 range (internal reference)	$SELAD = '0b010'$, $EME = '0b1'$, $SVREF = 0$; $DR2_{IO,0} = D2_{IO,0}(V) / D2_{IO,0}$ $V(IOx) = V(VBy) - 2.5 \text{ V}$ $V(IOx) = V(VBy) - 0.6 \text{ V}$	48 9.5	50 11.5	52 14	% %
739	$D3_{IO,0}$	Digital value using VR3 range (internal reference)	$SELAD = '0b100'$, $EME = '0b0'$, $SVREF = 0$, $V(IOx) = 0.6 \text{ V}$	790	840	1022	

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 k Ω \pm 1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
740	DR3 _{IO,0}	Relative value using VR3 range (internal reference)	SELAD = '0b100', EME = '0b0', SVREF = 0; DR3 _{IO,0} = D3 _{IO,0} (V) / D3 _{IO,0} V(IOx) = 0.3V V(IOx) = 0.1V	48 14.5	50 16	52 18.5	% %
741	D4 _{IO,0}	Digital value using VR4 range (internal reference)	SELAD = '0b100', EME = '0b1', SVREF = 0, V(IOx) = 5.0V	790	840	1022	
742	DR4 _{IO,0}	Relative value using VR4 range (internal reference)	SELAD = '0b100', EME = '0b1', SVREF = 0; DR4 _{IO,0} = D4 _{IO,0} (V) / D4 _{IO,0} V(IOx) = 2.5V V(IOx) = 0.6V	48 9.5	50 11.5	52 14	% %
743	D5 _{IO,0}	Digital value using VR5 range (internal reference)	SELAD = '0b011', SVREF = 0 V(IOx) = 36.0V	810	870	1022	
744	DR5 _{IO,0}	Relative value using VR5 range (internal reference)	SELAD = '0b011', SVREF = 0; DR5 _{IO,0} = D5 _{IO,0} (V) / D5 _{IO,0} V(IOx) = 24.0V V(IOx) = 5.0V	64.6 11.8	66.6 13.8	68.6 15.8	% %
745	DC _{IO,0}	Digital value of current measurement (internal reference)	SELAD = '0b001', SVREF = 0, I(IOx) = 150mA	720	820	1022	
746	DRC _{IO,0}	Digital value of current measurement (internal reference)	SELAD = '0b001', SVREF = 0; DRC _{IO,0} = DC _{IO,0} (I) / DC _{IO,0} I(IOx) = 75mA I(IOx) = 15mA	48 6.2	51 9.2	54 12.2	% %
Input RSET							
B01	V(RSET)	Voltage at RSET		1.15	1.22	1.30	V
B02	R(RSET)	Range value for RSET		9	10	14	k Ω
Burst-Indication							
C01	VSPon	Input On-Threshold for burst recognition		1.3		2.9	V
C02	VSPoff	Input Off-Threshold for Burst-recognition		1.4		3	V
C03	tpoff	Delay time to Reset after spike at VCC, VDD	Spike duration: 10 ns	2		110	μ s
Pin monitoring GNDA, GNDD							
H01	Vt() _{gnd}	Threshold voltage for open circuit detection on pins GNDA, GNDD		35		65	mV
H02	tmin() _{gnd}	Minimum duration for open circuit detection	V(GNDA,GNDD) = 0 V ... Vt() _{gnd}	1			μ s
H03	tpoff	Delay time to reset after open circuit detection at GNDA, GNDD				15	μ s
Undervoltage detection VB							
I01	VByon	Undervoltage message VB1...4 on		10.6	11.2	11.8	V
I02	VByoff	Undervoltage message VB1...4 off		10.0	10.6	11.2	V
I03	VByhys	Hysteresis	VByhys = VByon - VByoff	400			mV
I04	tmin() _{lv}	Minimum duration for Power-Down detection	VBy = 0.8 V ... VByoff	1			μ s
I05	tpoff	Delay time for undervoltage message VB1...4				6	μ s
μC-Interface, I/O-Logic, Frequency divider, Interrupt							
K01	Vt() _{hi}	Threshold voltage High at Schmitt-Trigger-Inputs NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NSP, POE	D0...7 with input function			2	V

ELECTRICAL CHARACTERISTICS

Operating conditions: $V_{CC} = V_{DD} = 3 \dots 5.5 \text{ V}$, $V_{By} = 12 \dots 36 \text{ V}$, $G_{NDA} = G_{NDD} = 0 \text{ V}$, $R_{SET} = 10 \text{ k}\Omega \pm 1\%$. All inputs on defined logic states (high or low), $T_j = -40 \dots 125 \text{ }^\circ\text{C}$ unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
K02	$V_t(\text{lo})$	Threshold voltage Low at Schmitt-Trigger-Inputs NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NSP, POE	D0...7 with input function	0.8			V
K03	$V_t(\text{hys})$	Schmitt-Trigger-Hysteresis at inputs NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NSP, POE	$V_t(\text{hys}) = V_t(\text{hi}) - V_t(\text{lo})$; D0...7 mit Eingangsfunktion	150			mV
K04	$V_s(\text{hi})$	Saturation voltage high an NINT, Dx	$V_s(\text{hi}) = V_{DD} - V(\)$; $I(\) = -4 \text{ mA}$			0.8	V
K05	$V_s(\text{lo})$	Saturation voltage low an NINT, Dx	$I(\) = 4 \text{ mA}$			0.49	V
K06	$I_{pd}(\)$	Pull Down current sources at A0...4, NRES, CLK, BLFQ, D0...7, POE	$V(\) = 1 \text{ V} \dots V_{DD}$	2		70	μA
K07	$I_{pu}(\)$	Pull Up current sources at NSP, NCS, NWR, NRD	$V(\) = 0 \text{ V} \dots V_{DD} - 1 \text{ V}$	-70		2	μA
K08	$t_p(\text{POE-IOx})$	Delay time output enable: POE to IOx disabled	$R_L = 240 \Omega \dots 1 \text{ k}\Omega$, POE: hi \rightarrow lo to $V(\text{IOx}) < 80\% (V_{By} - V_s(\text{IOx})_{hi})$			6	μs
K09	$t_w(\text{lo})$	Permissible pulse width for enable/disable at POE		600			ns
K10	$t_w(\)$	Permissible burst pulse width at POE				100	ns
K11	$t_{min}(\text{nres})$	minimum duration for reset at NRES		200			ns
Frequency BLFQ, CLK							
P01	$t_d(\)$	maximum frequency at CLK				TBD	MHz
P02	$t_d(\)$	maximum frequency at BLFQ				TBD	MHz

Characteristics: Diagrams

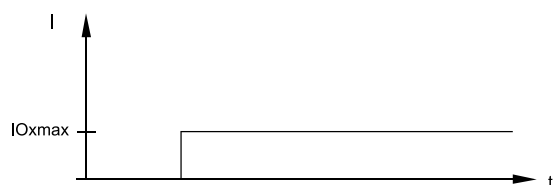


Figure 1: DC load

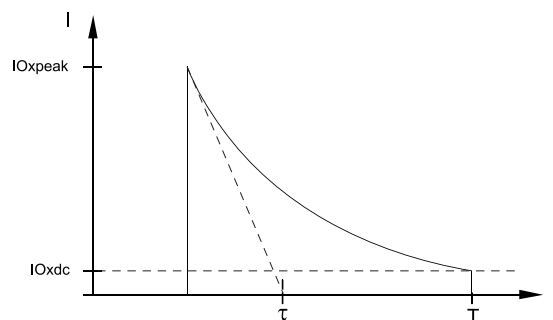


Figure 2: Pulse load

OPERATING REQUIREMENTS: Parallel μ C Interface

Operating Conditions: $V_{CC} = V_{DD} = 3...5.5$ V, $V_{By} = 12...36$ V, $G_{NDA} = G_{NDD} = 0$ V, $R_{SET} = 10$ k $\Omega \pm 1$ %
 $T_a = 0...70$ °C, $CL() = 150$ pF, input level lo = 0.8 V, hi = 2.2 V, reference levels according to figure 3

Item No.	Symbol	Parameter	Conditions			Unit
				Min.	Max.	
Read Cycle						
I001	t_{AR1}, t_{AR2}	Setup Time: NCS, A0...4 set before NRD hi \rightarrow lo	see Figure 4	30		ns
I002	t_{RA}	Hold Time: NCS, A0...4 set before NRD lo \rightarrow hi	see Figure 4	0		ns
I003	t_{RD}	Wait Time : Data valid after NRD hi \rightarrow lo	see Figure 4		120	ns
I004	t_{DF}	Hold Time: Data Bus high impedance after NRD lo \rightarrow hi	see Figure 4		65	ns
I005	t_{RL}	Required Read Signal Duration at NRD		50		ns
Write Cycle						
I006	t_{AW1}, t_{AW2}	Setup Time: NCS, A0...4 set before NWR lo \rightarrow hi	see Figure 4	30		ns
I007	t_{DW}	Setup time : Data valid before NWR lo \rightarrow hi	see Figure 4	100		ns
I008	t_{WA}	Hold time: NCS, A0...4 stable after NWR lo \rightarrow hi	see Figure 4	10		ns
I009	t_{WD}	Hold time: Data valid after NWR lo \rightarrow hi	see Figure 4	10		ns
I010	t_{WL}	Required Write Signal Duration at NWR	see Figure 4	50		ns
Read/Write Timing						
I011	t_{cyc}	Recovery Time between cycles: NRD lo \rightarrow hi to NRD hi \rightarrow lo, NRD lo \rightarrow hi to NWR hi \rightarrow lo, NWR lo \rightarrow hi to NWR hi \rightarrow lo, NWR lo \rightarrow hi to NRD hi \rightarrow lo	see Figure 4	165		ns

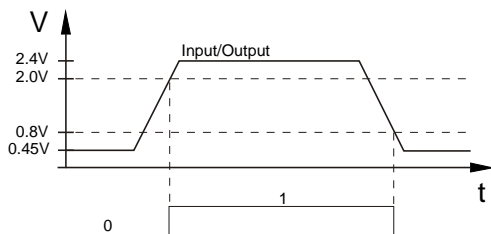


Figure 3: Reference levels for displayed values of time

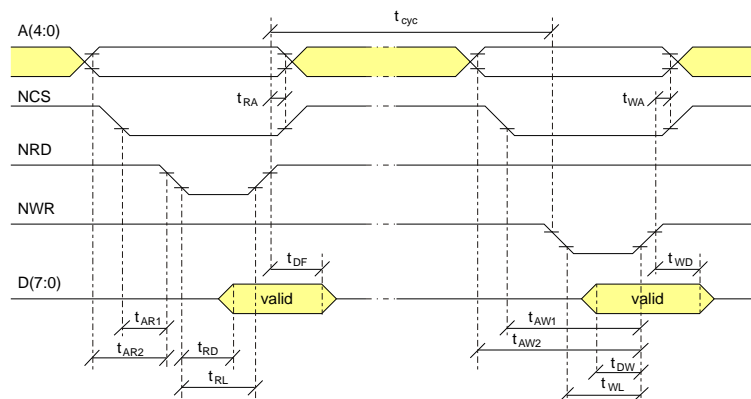


Figure 4: Read and write cycle for the parallel interface

OPERATING REQUIREMENTS: Serial μ C Interface

Operating Conditions: $V_{CC} = V_{DD} = 3...5.5$ V, $V_{By} = 12...36$ V, $G_{NDA} = G_{NDD} = 0$ V, $R_{SET} = 10$ k $\Omega \pm 1$ %
 $T_a = 0...70$ °C, $CL() = 150$ pF, input level lo = 0.8 V, hi = 2.2 V, reference levels according to figure 3

Item No.	Symbol	Parameter	Conditions			Unit
				Min.	Max.	
Gruppe 2.0 EN						
I111	t_{sCCL}	Setup time: NCS hi \rightarrow lo to SCK(A3) lo \rightarrow hi	see Figure 5	50		ns
I112	t_{sDCL}	Setup time: SI(D0) stabil before SCK(A3) lo \rightarrow hi	see Figure 5	40		ns
I113	t_{hDCL}	Hold time: SI(D0) stabil after SCK(A3) lo \rightarrow hi	see Figure 5	30		ns
I114	t_{CLh}	Clock duration SCK(A3) hi	see Figure 5	100		ns
I115	t_{CLl}	Clock duration SCK(A3) lo	see Figure 5	100		ns
I116	t_{CSsh}	Pulse duration NCS hi	see Figure 5	100		ns
I117	t_{pCLD}	Delay time: SOC(D1) resp. SOB(D2) stable after SCK(A3) hi \rightarrow lo	see Figure 5	0	50	ns
I118	t_{pCSD}	Delay time: SOC(D1) resp. SOB(D2) high impedance after NCS lo \rightarrow hi	see Figure 5	0	50	ns

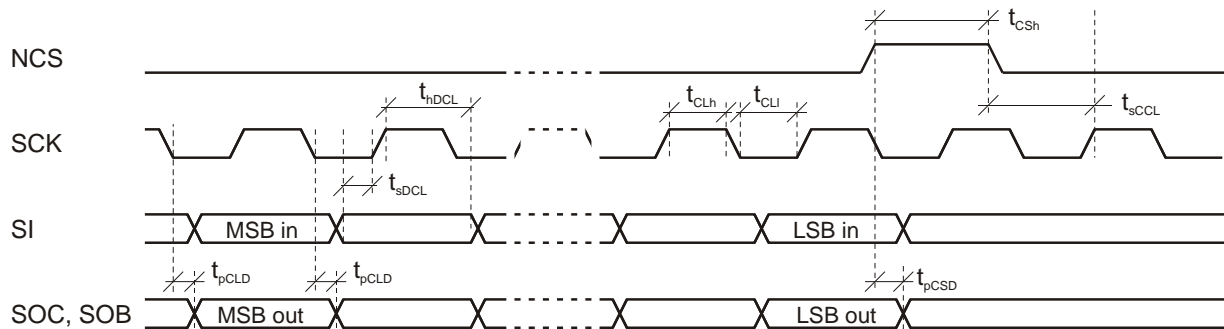


Figure 5: μ C interface in SPI mode

PROGRAMMING

Register Overview	Page 14	PN1...0	Flash Frequency Settings
Input Register	Page 15	SEBLQ	Flash Frequency Reference
IN16...1	Input Register, Status I/O-Pin	SECLK1...0	System Clock
Change of Input Messages	Page 15	Control Word 4	Page 24
DCH16...1	Change of Input Messages	EOI	End of Interrupt
Interrupt Messages	Page 16	BYPSCF	Bypass SC Filter
DCHI	Input Change Interrupt	SCF3...0	SC Filter Timing
IET2...1	Overtemperatur Interrupt	Control Word 5	Page 24
ISCS	Overcurrent Interrupt	SELES3...0	Select I/O-Stage for AD Converter
ET2...1	Overtemperatur	Control Word 6	Page 25
SCS	Overcurrent	SELAD2...0	Settings for ADC-Measurements
IEOC	ADC Interrupt	EME	Extended Measurement Enable
ISD	Interrupt - Bursts on VDD	EW	Enable ADC-Measurement
IUSD	Interrupt - Undervoltage at VDD	SVREF	Select VREF
IUSA	Interrupt - Undervoltage at VCC	Interconnection Error, Device-ID	Page 25
EOC	ADC End-Of-Conversion	IBA	Interconnection Error
USD	Undervoltage VDD	USVB	Undervoltage VB
USA	Undervoltage VCC	NRESA	NRES = '0'
Overcurrent	Page 17	DID4...0	Device ID
ISCI16...1	Overcurrent-Messages, Interrupt		
SC16...1	Overcurrent-Status, actual		
A/D Converter Data	Page 18		
D9...0	ADC-Measurement Value		
Output Register	Page 18		
OUT16..0	Output Register High-Side Driver		
Flash Puls Enable	Page 18		
PEN16...0	Enable		
Interrupt-Enable	Page 19		
IEN16...1	Input Change Enable		
SCEN16...1	Overcurrent Enable		
Control Word 1	Page 20		
BYP3...0	I/O-Filter-Bypass		
FL1...0	I/O-Filter		
FH1...0	I/O-Filter		
Control Word 2	Page 21		
NIOH, NIOL	I/O-Pin-Functions		
IL2...0	Current sources		
IH2...0	Current sources		
Control Word 3	Page 23		

Register Overview							
Adress							
A(4...0)	A4	A3	A2	A1	A0	Write	Read
0x00	0	0	0	0	0	-	Input Register A ^{1,2}
0x01	0	0	0	0	1	-	Input Register B ^{1,2}
0x02	0	0	0	1	0	-	Input Change Message A ^{1,3}
0x03	0	0	0	1	1	-	Input Change Message B ^{1,3}
0x04	0	0	1	0	0	-	Interrupt Message Register A
0x05	0	0	1	0	1	-	Interrupt Message Register B
0x06	0	0	1	1	0	-	Overcurrent Message A ^{1,4}
0x07	0	0	1	1	1	-	Overcurrent Message B ^{1,4}
0x08	0	1	0	0	0	-	Overcurrent Status A ¹
0x09	0	1	0	0	1	-	Overcurrent Status B ¹
0x0A	0	1	0	1	0	-	A/D-Converter Data 1
0x0B	0	1	0	1	1	-	A/D-Converter Data 2
0x0C	0	1	1	0	1		Output Register A ¹
0x0D	0	1	1	1	0		Output Register B ¹
0x0E	0	1	1	1	1		Flash Pulse Enable A ¹
0x0F	1	0	0	0	0		Flash Pulse Enable B ¹
0x10	1	0	0	0	1		Interrupt-Enable Input Change A ^{1,5}
0x11	1	0	0	1	0		Interrupt-Enable Input Change B ^{1,5}
0x12	1	0	0	1	1		Interrupt-Enable Overcurrent A ¹
0x13	1	0	1	0	0		Interrupt-Enable Overcurrent B ¹
0x14	1	0	1	0	1		Control Word 1A (I/O Filter) ¹
0x15	1	0	1	1	0		Control Word 1B (I/O Filter) ¹
0x16	1	0	1	1	1		Control Word 2A (I/O Pin Functions) ¹
0x17	1	1	0	0	0		Control Word 2B (I/O Pin Functions) ¹
0x18	1	1	0	0	1		Control Word 3A (Flash Pulse Settings) ¹
0x19	1	1	0	1	0		Control Word 3B (Flash Pulse Settings) ¹
0x1A	1	1	0	1	1		Control Word 4 (Overcurrent Filter Settings)
0x1B	1	1	1	0	0		Control Word 5 (I/O Stage Selection for AD Converter)
0x1C	1	1	1	0	1		Control Word 6 (AD Converter Settings)
0x1D	0	1	1	0	0	-	Interconnection Error, Device-ID
0x1E	1	1	1	1	0		Test Register 1
0x1F	1	1	1	1	1		Test Register 2

Table 7: Register assignment

1. A: I/O-Stages 1...8, B: I/O-Stages 9...16
2. Reads the input or reads back the outputs, depending on I/O pin mode
3. For I/O pins in input mode (register is '0' in output mode)
4. For I/O pins in output mode (register is '0' in input mode)
5. Only writable in input mode

Input Register A (read only)								Adr. 0x00
reading of inputs / output feedback								
								reset entry: 0x00
Bit Name	7 IN8	6 IN7	5 IN6	4 IN5	3 IN4	2 IN3	1 IN2	0 IN1
Bit7...0	0	Input/Output IOx read '0'						(r)
IN8...1	1	Input/Output IOx read '1'						

Input Register B (read only)								Adr. 0x01
reading of inputs / output feedback								
								reset entry: 0x00
Bit Name	7 IN16	6 IN15	5 IN14	4 IN13	3 IN12	2 IN11	1 IN10	0 IN9
Bit7...0	0	Input/Output IOx read '0'						(r)
IN16...9	1	Input/Output IOx read '1'						

INx indicates the state for IOx (via I/O filter or bypass).

Change-of-input Message A (read only)								Adr. 0x02
for I/O stages in input mode								
								reset entry: 0x00
Bit Name	7 DCH8	6 DCH7	5 DCH6	4 DCH5	3 DCH4	2 DCH3	1 DCH2	0 DCH1
Bit7...0	0	No change of state at the input IOx or no interrupt enable						(r)
DCH8...1	1	Input IOx has had a change of state enabled for interrupt messages						

Change-of-input Message B (read only)								Adr. 0x03
for I/O stages in input mode								
								reset entry: 0x00
Bit Name	7 DCH16	6 DCH15	5 DCH14	4 DCH13	3 DCH12	2 DCH11	1 DCH10	0 DCH9
Bit7...0	0	No change of state at the input IOx or no interrupt enable						(r)
DCH16...9	1	Input IOx has had a change of state enabled for interrupt messages						

Interrupt Status Register A (read only)								Adr. 0x04	
reset entry: 0x00									
Bit	7	6	5	4	3	2	1	0	
Name	DCHI	IET2	IET1	ISCI	-	ET2	ET1	SCS	

Change-of-input data, overtemperatur, overcurrent (interrupts stored)			
Bit7	0	No message	(r)
DCHI	1	Interrupt through change-of input message	
Bit6	0	No message	(r)
IET2	1	Interrupt through excessive temperature level 2	
Bit5	0	No message	(r)
IET1	1	Interrupt through excessive temperature level 1	
Bit4	0	No message	(r)
ISCI	1	Interrupt through overcurrent message	

Excessive temperature status, overcurrent status (real time signals, at the time of readout)			
Bit2	0	No error message	(r)
ET2	1	Excessive temperature level 2 (shutdown)	
Bit1	0	No error message	(r)
ET1	1	Excessive temperature level 1 (warning)	
Bit0	0	No error message	(r)
SCS	1	Overcurrent status (e.g. caused by low-side short circuit)	

Interrupt Status Register B (read only)								Adr. 0x05	
reset entry: 0x00									
Bit	7	6	5	4	3	2	1	0	
Name	IEOC	ISD	IUSD	IUSA	-	EOC	USD	USA	

A/D-Converter, Bursts, Undervoltage (interrupts stored)			
Bit7	0	No message	(r)
IEOC	1	Interrupt by the A/D-Converter	
Bit6	0	No message	(r)
ISD	1	Interrupt caused by bursts at VDD	
Bit5	0	No message	(r)
IUSD	1	Interrupt caused by undervoltage at VDD	
Bit4	0	No message	(r)
IUSA	1	Interrupt caused by undervoltage at VCC	

A/D-Converter, Undervoltage (real time signals, at the time of readout)			
Bit2	0	No message	(r)
EOC	1	A/D conversion completed (End of Conversion)	
Bit1	0	No message	(r)
USD	1	Undervoltage at VDD	
Bit0	0	No message	(r)
USA	1	Undervoltage at VCC	

Read access gates off changes to the register; the register is reenabled only when reset via EOI. Any successive interrupts which occur at DCHI, IET2, IET1, ISCI, IEOC, ISD, IUSD und IUSA during the read-out phase and before a reset with EOI are trapped by an interrupt pipeline. If this happens, the message at NINT resp. D1/SOC or D2/SOB cannot be deleted by EOI, i.e. NINT resp. D1/SOC or D2/SOB constantly remains on low. In this instance, EOI fills the overcurrent message from the pipeline.

Overcurrent Message A (read only)								Adr. 0x06		
reset entry: 0x00										
Bit	7	6	5	4	3	2	1	0		
Name	SCI8	SCI7	SCI6	SCI5	SCI4	SCI3	SCI2	SCI1		
Bit7...0	0	No Message								(r)
SCI8...1	1	Output IOx has had an overcurrent state enabled for interrupt messages (short circuit)								

Overcurrent Message B (read only)								Adr. 0x07		
reset entry: 0x00										
Bit	7	6	5	4	3	2	1	0		
Name	SCI16	SCI15	SCI14	SCI13	SCI12	SCI11	SCI10	SCI9		
Bit7...0	0	No Message								(r)
SCI16...9	1	Output IOx has had an overcurrent state enabled for interrupt messages (short circuit)								

Read access gates off changes to the register; the register is reenabled only when reset via EOI. Any successive interrupts which occur during the read-out phase and before a reset with EOI are trapped by an interrupt pipeline. If this happens, the message at NINT resp. D1/SOC or D2/SOB cannot be deleted by EOI, i.e. NINT resp. D1/SOC or D2/SOB constantly remains on low. In this instance, EOI fills the overcurrent message from the pipeline.

The SCIx bits may be erased selectable by reenabling IENx after disable. '0' is output for IOx pins in input mode. SCIx reports for IOx.

Overcurrent Status A (read only)								Adr. 0x08		
reset entry : 0x00										
Bit	7	6	5	4	3	2	1	0		
Name	SC8	SC7	SC6	SC5	SC4	SC3	SC2	SC1		
Bit7...0	0	No overcurrent								(r)
SC8...1	1	Overcurrent in output IOx, e.g. through a low-side short circuit								

Overcurrent Status B (read only)								Adr. 0x09		
reset entry: 0x00										
Bit	7	6	5	4	3	2	1	0		
Name	SC16	SC15	SC14	SC13	SC12	SC11	SC10	SC9		
Bit7...0	0	No overcurrent								(r)
SC16...9	1	Overcurrent in output IOx, e.g. through a low-side short circuit								

These signals act as error analysis and does not generate any interrupts (real time, no register). '0' is output for IOx pins in input mode. SCx reports for IOx.

A/D-Converter Data 1 (read only)								Adr. 0x0A	
								reset entry: 0x00	
Bit Name	7	6	5	4	3	2	1	0	
	D9	D8	D7	D6	D5	D4	D3	D2	
Bit7...0	0	Bit value is 0							(r)
D9...2	1	Bit value equals $VREFi/1024 * 2^n$, with $n = 9..2$							

A/D-Converter Data 2 (read only)								Adr. 0x0B	
								reset entry: 0x00	
Bit Name	7	6	5	4	3	2	1	0	
	D1	D0	-	-	-	-	-	-	
Bit7...0	0	Bit value is 0							(r)
D1...0	1	Bit value equals $VREFi/1024 * 2^n$, with $n = 1..0$							

Digitized result of the analog measurement for load current, I/O voltage, driver supply, internal voltage reference or temperature measurement. During the current measurement, VREFi corresponds to the saturation voltage of the internal reference transistor, otherwise it is either the internal reference voltage V(Vrefad) (bit SVREF = ' 0 ', control word 6) or the voltage at the pin Vref (bit SVREF = ' 1 ', control word 6).

Output-Register A								Adr. 0x0C	
for I/O stages with output function								reset entry: 0x00	
Bit Name	7	6	5	4	3	2	1	0	
	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	
Bit7...0	0	High-side driver "OFF"							(r)
OUT8...1	1	High-side driver "ON", i.e. normally, IOx = 1							

Output-Register B								Adr. 0x0D	
for I/O stages with output function								reset entry: 0x00	
Bit Name	7	6	5	4	3	2	1	0	
	OUT16	OUT15	OUT14	OUT13	OUT12	OUT11	OUT10	OUT9	
Bit7...0	0	High-side driver "OFF"							(r)
OUT16...9	1	High-side driver "ON", i.e. normally, IOx = 1							

OUTx switches the high-side driver for IOx.

Flash Pulse Enable A								Adr. 0x0E	
for I/O stages with output function								reset entry: 0x00	
Bit Name	7	6	5	4	3	2	1	0	
	PEN8	PEN7	PEN6	PEN5	PEN4	PEN3	PEN2	PEN1	
Bit7...0	0	Flash pulse "DISABLED"							(r)
PEN8...1	1	Flash pulse "ENABLED"							

PENx enables the flash pulse for IOx.

Flash Pulse Enable B								Adr. 0x0F		
for I/O stages with output function										
reset entry: 0x00										
Bit	7	6	5	4	3	2	1	0		
Name	PEN16	PEN15	PEN14	PEN13	PEN12	PEN11	PEN10	PEN9		
Bit7...0	0	Flash pulse "DISABLED"								(r)
PEN16...9	1	Flash pulse "ENABLED"								

PENx enables the flash pulse for IOx.

Change-of-input Interrupt Enable A								Adr. 0x10		
for I/O stages with input function										
reset entry: 0x00										
Bit	7	6	5	4	3	2	1	0		
Name	IEN8	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1		
Bit7...0	0	"DISABLED" for interrupt								(r)
IEN8...1	1	"ENABLED" for interrupt: A hi \rightarrow lo or lo \rightarrow hi change of state at the input IOx triggers an interrupt.								

Change-of-input Interrupt Enable B								Adr. 0x11		
for I/O stages with input function										
reset entry: 0x00										
Bit	7	6	5	4	3	2	1	0		
Name	IEN16	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9		
Bit7...0	0	"DISABLED" for interrupt								(r)
IEN16...9	1	"ENABLED" for interrupt: A hi \rightarrow lo or lo \rightarrow hi change of state at the inut IOx triggers an interrupt.								

IENx enables the input IOx for interrupt. The outputs IOx can not be enabled for interrupt. The registers can only be modified in input mode.

Overcurrent Interrupt Enable A								Adr. 0x12		
reset entry: 0x00										
Bit	7	6	5	4	3	2	1	0		
Name	SCEN8	SCEN7	SCEN6	SCEN5	SCEN4	SCEN3	SCEN2	SCEN1		
Bit7...0	0	"DISABLED" for interrupt								(r)
SCEN8...1	1	"ENABLED" for interrupt: a short-circuit at IOx triggers an interrupt.								

Overcurrent Interrupt Enable B								Adr. 0x13		
reset entry: 0x00										
Bit	7	6	5	4	3	2	1	0		
Name	SCEN16	SCEN15	SCEN14	SCEN13	SCEN12	SCEN11	SCEN10	SCEN9		
Bit7...0	0	"DISABLED" for interrupt								(r)
SCEN16...9	1	"ENABLED" for interrupt: a short-circuit at IOx triggers an interrupt.								

SCENx enables the output IOx for interrupt.

Control Word 1A (I/O filters)								Adr. 0x14	
reset entry: 0x00									
	Nibble 1: I/O-Pins 5..8				Nibble 0: I/O-Pins 1..4				
Bit Name	7 BYP1	6 -	5 FH1	4 FH0	3 BYP0	2 -	1 FL1	0 FL0	

Nibble 1

Bit7 BYP1	0 1	I/O filters aktive Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state.							(r)	
Bit5..4 FH1..0		FH1	FH0	Filter times ¹						
		0	0	14.5 * $tc(SECLK)$ \pm 1 * $tc(SECLK)$						(r)
		0	1	896.5 * $tc(SECLK)$ \pm 64 * $tc(SECLK)$						
		1	0	3584.5 * $tc(SECLK)$ \pm 256 * $tc(SECLK)$						
		1	1	7168.5 * $tc(SECLK)$ \pm 512 * $tc(SECLK)$						

Nibble 0

Bit3 BYP0	0 1	I/O filter aktive Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state.							(r)	
Bit1..0 FL1..0		FL1	FL0	Filter times ¹						
		0	0	14.5 * $tc(SECLK)$ \pm 1 * $tc(SECLK)$						(r)
		0	1	896.5 * $tc(SECLK)$ \pm 64 * $tc(SECLK)$						
		1	0	3584.5 * $tc(SECLK)$ \pm 256 * $tc(SECLK)$						
		1	1	7168.5 * $tc(SECLK)$ \pm 512 * $tc(SECLK)$						

Control Word 1B (I/O filters)								Adr. 0x15	
reset entry: 0x00									
	Nibble 3: I/O-Pins 13..16				Nibble 2: I/O-Pins 9..12				
Bit Name	7 BYP3	6 -	5 FH1	4 FH0	3 BYP2	2 -	1 FL1	0 FL0	

Nibble 3

Bit7 BYP1	0 1	I/O filters aktive Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state.							(r)	
Bit5..4 FH1..0		FH1	FH0	Filter times ¹						
		0	0	14.5 * $tc(SECLK)$ \pm 1 * $tc(SECLK)$						(r)
		0	1	896.5 * $tc(SECLK)$ \pm 64 * $tc(SECLK)$						
		1	0	3584.5 * $tc(SECLK)$ \pm 256 * $tc(SECLK)$						
		1	1	7168.5 * $tc(SECLK)$ \pm 512 * $tc(SECLK)$						

Nibble 2

Bit3 BYP0	0 1	I/O filters aktive Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state.							(r)	
Bit1..0 FL1..0		FL1	FL0	Filter times ¹						
		0	0	14.5 * $tc(SECLK)$ \pm 1 * $tc(SECLK)$						(r)
		0	1	896.5 * $tc(SECLK)$ \pm 64 * $tc(SECLK)$						
		1	0	3584.5 * $tc(SECLK)$ \pm 256 * $tc(SECLK)$						
		1	1	7168.5 * $tc(SECLK)$ \pm 512 * $tc(SECLK)$						

1. SECLK: see control word 3B on page 23

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Control Word 2A (I/O pin funktions)								Adr. 0x16
								reset entry: 0x11
Nibble 1: I/O-Pins 5..8				Nibble 0: I/O-Pins 1..4				
Bit Name	7 NIOH	6 IH2	5 IH1	4 IH0	3 NIOL	2 IL2	1 IL1	0 ILO

Nibble 1

Bit7 NIOH	0 1	Input mode Output mode						(r)
Bit6..4 IH2..0		IH2	IH1	IH0	current sources			
		0	0	0	0 μ A Pull-Down			
		0	0	1	200 μ A Pull-Down		(r)	
		0	1	0	600 μ A Pull-Down			
		0	1	1	2mA Pull-Down			
		1	0	0	0 μ A Pull-Up			
		1	0	1	200 μ A Pull-Up			
		1	1	0	600 μ A Pull-Up			
		1	1	1	2mA Pull-Up			

Nibble 0

Bit3 NIOL	0 1	Input mode Output mode						(r)
Bit2..0 IL2..0		IL2	IL1	IL0	Current sources			
		0	0	0	0 μ A Pull-Down			
		0	0	1	200 μ A Pull-Down		(r)	
		0	1	0	600 μ A Pull-Down			
		0	1	1	2mA Pull-Down			
		1	0	0	0 μ A Pull-Up			
		1	0	1	200 μ A Pull-Up			
		1	1	0	600 μ A Pull-Up			
		1	1	1	2mA Pull-Up			

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Control Word 2B (I/O-Pinfunktion) Adr. 0x17

reset entry: 0x11

	Nibble 3: I/O-Pins 13..16				Nibble 2: I/O-Pins 9..12			
Bit Name	7 NIOH	6 IH2	5 IH1	4 IH0	3 NIOL	2 IL2	1 IL1	0 ILO

Nibble 3

Bit7 NIOH	0 1	Input mode Output mode						(r)
Bit6..4 IH2..0		IH2	IH1	IH0	Current sources			
		0	0	0	0 μ A Pull-Down			
		0	0	1	200 μ A Pull-Down		(r)	
		0	1	0	600 μ A Pull-Down			
		0	1	1	2mA Pull-Down			
		1	0	0	0 μ A Pull-Up			
		1	0	1	200 μ A Pull-Up			
		1	1	0	600 μ A Pull-Up			
		1	1	1	2mA Pull-Up			

Nibble 2

Bit3 NIOL	0 1	Input mode Output mode						(r)
Bit2..0 IL2..0		IL2	IL1	IL0	Current sources			
		0	0	0	0 μ A Pull-Down			
		0	0	1	200 μ A Pull-Down		(r)	
		0	1	0	600 μ A Pull-Down			
		0	1	1	2mA Pull-Down			
		1	0	0	0 μ A Pull-Up			
		1	0	1	200 μ A Pull-Up			
		1	1	0	600 μ A Pull-Up			
		1	1	1	2mA Pull-Up			

Control Word 3A (flash pulse settings)								Adr. 0x18	
Reset-Zustand : 0x00									
	Nibble 3: I/O-Pins 13..16		Nibble 2: I/O-Pins 9..12		Nibble 1: I/O-Pins 5..8		Nibble 0: I/O-Pins 1..4		
Bit Name	7	6	5	4	3	2	1	0	
	PN31	PN30	PN21	PN20	PN11	PN10	PN01	PN00	
Nibble 1									
Nibble3, Bit7..6	PN31	PN30	Flash frequency		Flash frequency				
Nibble2, Bit5..4	PN21	PN20							
Nibble1, Bit3..2	PN11	PN10							
Nibble0, Bit1..0	PN01	PN00	SEBLQ = 0		SEBLQ = 1 ¹				
	0	0	f(BLFQ)		f(SECLK)/2 ¹⁹		(r)		
	0	1	f(BLFQ/2)		f(SECLK)/2 ²⁰				
	1	0	f(BLFQ/4)		f(SECLK)/2 ²¹				
	1	1	f(BLFQ/16)		f(SECLK)/2 ²³				

1. SEBLQ: see control word 3B

Control Word 3B (reference clock)								Adr. 0x19	
reset entry: 0x00									
Bit Name	7	6	5	4	3	2	1	0	
	-	-	-	-	SECLK1	SECLK0	-	SEBLQ	
Bit0	SEBLQ	Settings for flash frequency							
SEBLQ	0	The flashing pulse is derived from the external clock signal at BLFQ (r)							
	1	The flashing pulse is derived from the system clock SECLK							
Bit3..2	SECLK1	SECLK0	Settings for system clock SECLK						
SECLK1..0	0	0	Operation with the clock signal at CLK (r)						
	0	1	Operation with the internal clock signal ICLK						
	1	0	Operation without the clock signal at CLK (filterung etc. deactivated)						
	1	1	reserved						

Control Word 4 (filter settings for overcurrent message)								Adr. 0x1A	
								reset entry : 0x00	
					Nibble3	Nibble2	Nibble1	Nibble0	
Bit Name	7	6	5	4	3	2	1	0	
	EOI	-	-	BYPSCF	SCF3	SCF2	SCF1	SCF0	
Bit7 EOI	0	No effect							(r)
	1	"DELETE"s the interrupt message (change-of-input message; interrupt status register, overcurrent message) accepts successive interrupts from the pipeline, deletes the messages at NINT resp. D1/SOC or D2/SOB when the pipeline is empty. Bit automatically resets to '0'.							
Bit4 BYPSCF	0	Filters for the overcurrent message are active							(r)
	1	Bypass for the filters: overcurrent messages are reprocessed in their unfiltered state.							
Bit3 SCF3	0	Nibble 3 Overcurrent message with 2.3ms filtering							(r)
	1	Overcurrent message with 4.6ms filtering Gives the filter times with the clock frequency at SECLK ¹ , i.e. 1.25MHz: 2.3ms aus $(2689.5 \pm 192) * tc(SECLK)$ bzw. 4.6ms aus $(5378.5 \pm 384) * tc(SECLK)$							
Bit2 SCF2	0	Nibble 2 Overcurrent message with 2.3ms filtering							(r)
	1	Overcurrent message with 4.6ms filtering							
Bit1 SCF1	0	Nibble 1 Overcurrent message with 2.3ms filtering							(r)
	1	Overcurrent message with 4.6ms filtering							
Bit1 SCF0	0	Nibble 0 Overcurrent message with 2.3ms filtering							(r)
	1	Overcurrent message with 4.6ms filtering							

1. SECLK: see control word 3B on page 23

Control Word 5 (selects I/O stage for ADC-measurements)						Adr. 0x1B		
						reset entry : 0x00		
Bit Name	7	6	5	4	3	2	1	0
	-	-	-	-	SELES3	SELES2	SELES1	SELES0
Bit3..0 SELES3..0	SELES3	SELES2	SELES1	SELES0	Selection of I/O stage			(r)
	0	0	0	0	I/O stage 1			
	0	0	0	1	I/O stage 2			
	0	0	1	0	I/O stage 3			
	0	0	1	1	I/O stage 4			
	0	1	0	0	I/O stage 5			
	0	1	0	1	I/O stage 6			
	0	1	1	0	I/O stage 7			
	0	1	1	1	I/O stage 8			
	1	0	0	0	I/O stage 9			
	1	0	0	1	I/O stage 10			
	1	0	1	0	I/O stage 11			
	1	0	1	1	I/O stage 12			
	1	1	0	0	I/O stage 13			
	1	1	0	1	I/O stage 14			
	1	1	1	0	I/O stage 15			
	1	1	1	1	I/O stage 16			

Control Word 6 (ADC settings)								Adr. 0x1C
								reset entry : 0x00
Bit Name	7	6	5	4	3	2	1	0
	-	-	SVREF	EW	EME	SELAD2	SELAD1	SELAD0
Bit2..0 SELAD2..0		SELAD2	SELAD1	SELAD0	Settings for ADC measurements			
		0	0	0	A/D-Converter disabled (r)			
		0	0	1	Current measurement IO ¹			
		0	1	0	Voltage measurement high at IO ¹			
		0	1	1	Overall voltage measurement range at IO ¹			
		1	0	0	Voltage measurement low at IO ¹			
		1	0	1	VBy voltage measurement (y:1..4) ²			
		1	1	0	VBy voltage measurement			
		1	1	1	Temperature measurement			
Bit3 EME		0	Measurement range extention "OFF" (for voltages up to 0.6V) (r)					
		1	Measurement range extention "ON" (for voltages up to 5V)					
			For voltage measurements, the range extention can be either High or Low .					
Bit4 EW		0	A/D converter "OFF" (r)					
		1	A/D converter activated					
			Bit automatically resets to '0'.					
Bit5 SVREF		0	Internal reference voltage V(VREFAD) is used (r)					
		1	External reference voltage at Pin VREF is used					

1. The corresponding I/O stage is selected via bit (3:0) of control word 5.
2. VBy is selected in control word via bits SELES(3:0). VB1 measurements apply to SELES(3:0) = 0x0...0x3, VB2 measurements apply to SELES(3:0) = 0x4...0x7, VB3 measurements apply to SELES(3:0) = 0x8...0xB and VB4 measurements apply to SELES(3:0) = 0xC...0xF.

Interconnection Error, Device Identification (read only)								Adr. 0x1D
								reset entry : 0x15
Bit Name	7	6	5	4	3	2	1	0
	IBA	USVB	NRESA	DID4	DID3	DID2	DID1	DID0
Bit7 IBA		0	No message (r)					
		1	Interconnection error, broken bond wire at GNDA or GNDD					
Bit6 USVB		0	No message (r)					
		1	Undervoltage at VB4, VB3, VB2 or VB1					
Bit5 NRESA		0	No message (r)					
		1	NRES is 0					
Bit4..0 DID4..0			Device ID for iC-JX: 0b10101 (r)					

'-' spare storage space with no funktion; '0' after reset.
(r) reset entry

DESCRIPTION OF FUNCTIONS

Interfaces

iC-JX can be operated with either a serial or parallel interface. This is set using pin NSP. When this pin is connected to VDD the device works in parallel mode. With NSP connected to ground iC-JX operates in serial mode.

Operation with a parallel interface

The parallel interface in iC-JX consists of 8 data, 5 address and 3 control lines. Address lines A4...0 are used to select the registers in iC-JX. The addresses are accepted with the falling edge of chip select signal NCS. Control lines NRD and NWR govern read and write access. A circuit diagram of the parallel micro-controller interface is given in Figure 6.

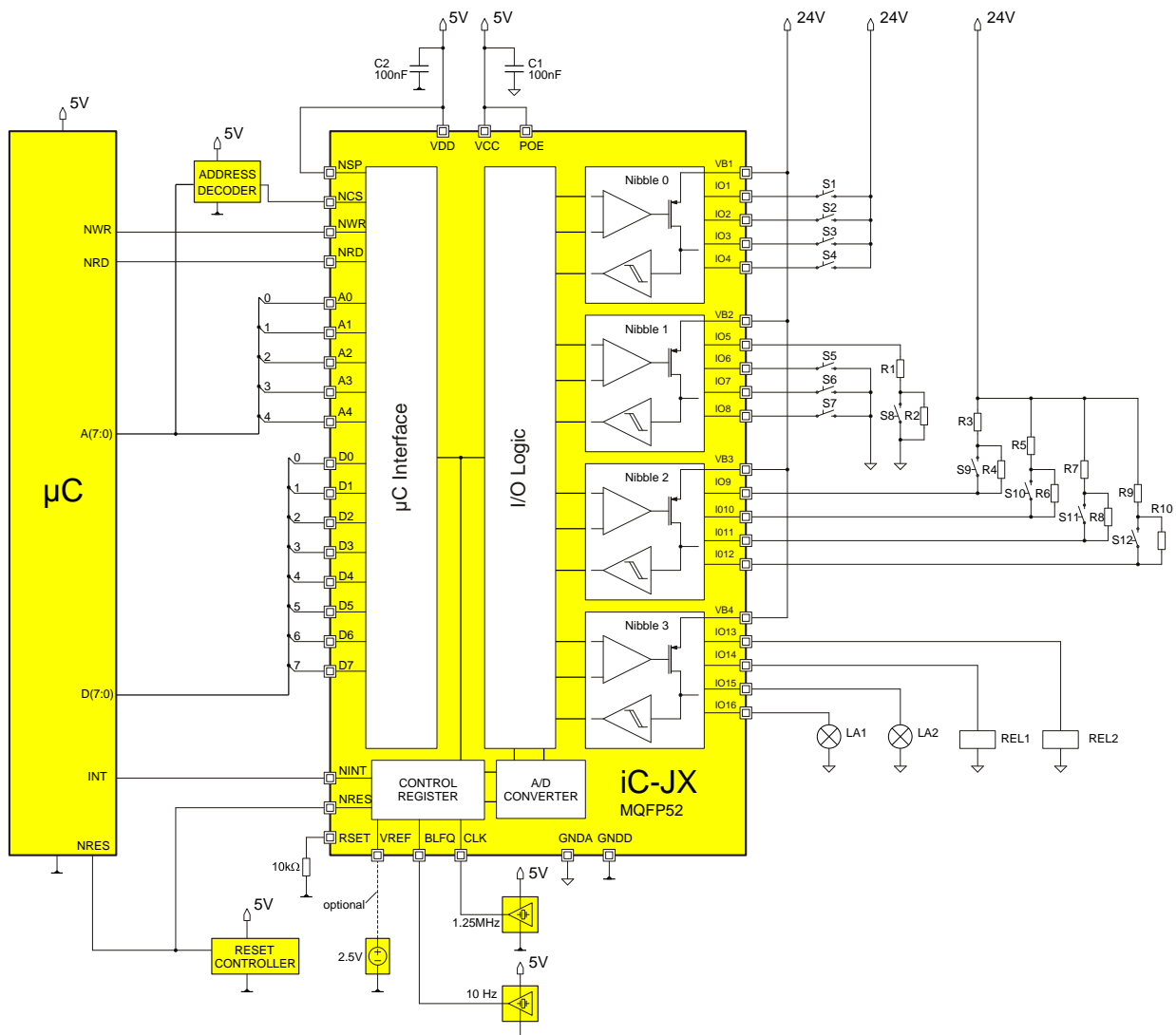


Figure 6: Example application using a parallel interface

Operation with a serial interface

To reduce the number of lines running between the microcontroller and iC-JX and thus to economize on the use of optocouplers between the former and either one or several iCs in a unit, for example, an extended

serial-peripheral interface (SPI) has been integrated into iC-JX. In order to ensure communication between the iC-JX and standard micro controllers, address and data words are both eight bit wide. A possible wiring is shown in Figure 7.

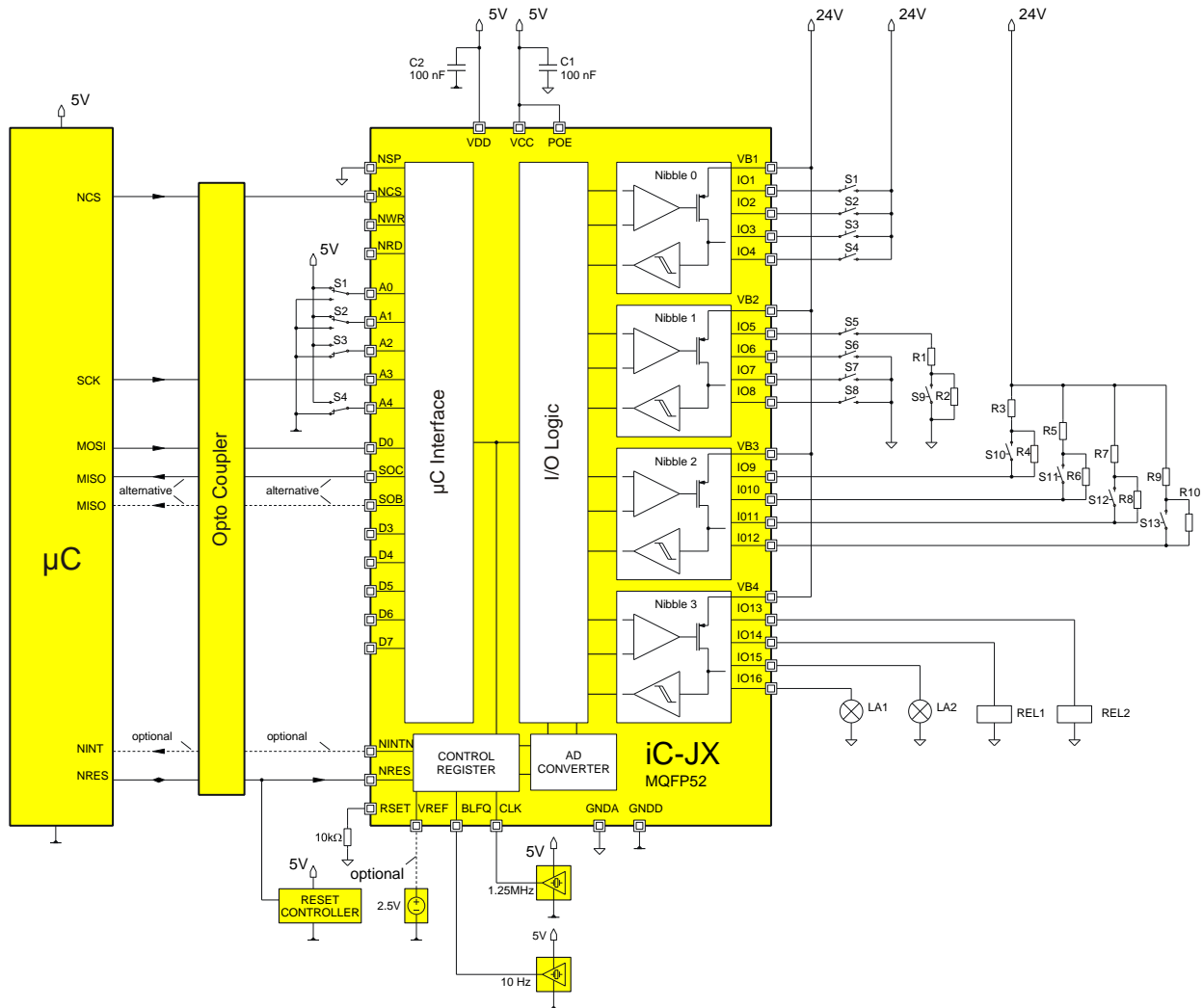


Figure 7: Example application using a serial interface

Several iC-JXs can be operated on an SPI. If the devices are to be configured as a chain, up to three can be placed in a row; with buses, four devices can be used. To this end iC-JX's SPI has both a clock input (SCK) and chip select input (NCS) and a data input (SI) and data output for chain operation (SOC, Serial Out Chain) and bus operation (SOB, Serial Out Bus). The configuration is set using pin A2. If this is at 0, the devices are in chain operation; if this is at '1', the chips switch to bus configuration.

In chain configuration (see Figure 8, top) output SOC of a device is connected up to the SI data input of the following chip; output SOB is not used. During the addressing sequence (1 byte of communication) all iC-JXs are switched through transparently so that all devices receive the transmitted address simultaneously. Only the addressed chip then goes into data transfer

mode; the others remain transparent so that communication between the controller and addressed iC-JX can take place without delay. It must be noted here that even in transparent mode each iC-JX has a certain transmit time which has an effect on the maximum data frequency of the overall system. The advantage of this configuration lies in the fact that it is possible to read out the values of an address in all devices very quickly.

In bus configuration (see Figure 8, bottom) all SI inputs and SOB outputs are switched in parallel; the SOC outputs are not used. Addressing the devices ensures that only one of the chips outputs data to SOB; the outputs of the inactive iCs are switched to tristate. This type of configuration differs from chain configuration in that it permits higher clock rates and also allows up to four iC-JXs to be connected up to an SPI bus.

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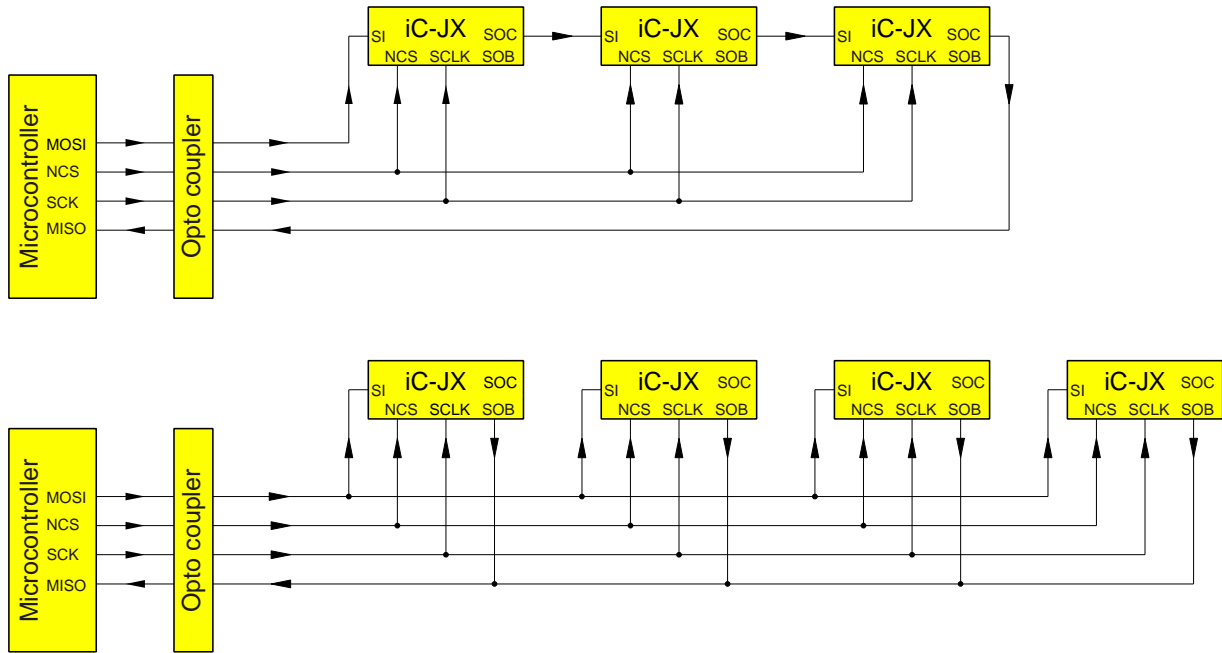


Figure 8: Possible SPI configurations

If no communication takes place on the SPI the chips can send interrupts to the controller by switching the master MISO line to 0. To this end all iC-JXs in chain configuration are switched through transparently (see Figure 9). In bus configuration the relevant chip drives a 0 at its SOB output towards the pull-up resistors at the outputs of the other devices.

Using pin A4 settings can be made as to whether interrupts are signaled to the master via the SOB or SOC (0 = no interrupt message; 1 = interrupt message). The message must be deactivated in bus configuration if further devices are present on the SPI bus as otherwise data can collide on the bus which is not desirable here.

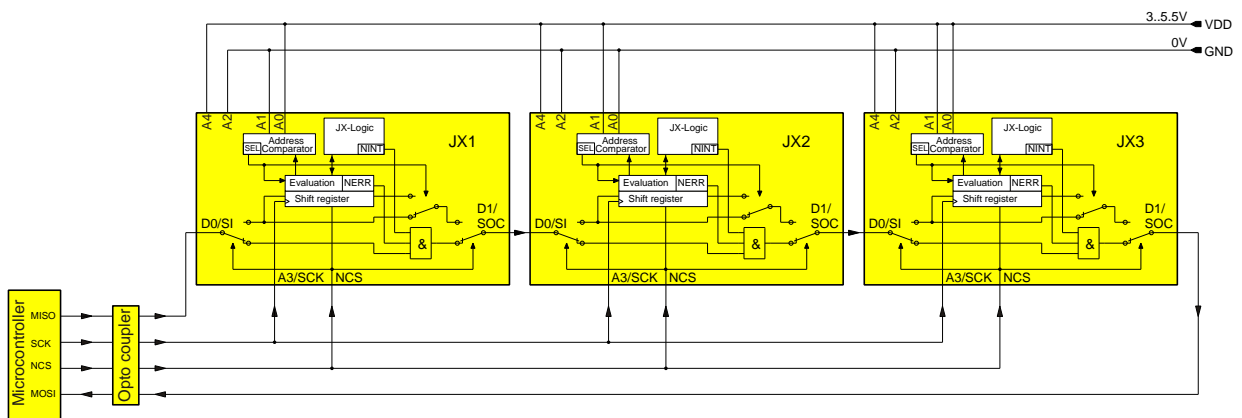


Figure 9: Addressing and interrupt messaging scheme in chain configuration

The first byte of communication (see Figure 10) consists of the 2-bit chip address (BA1:0), the 5-bit reg-

ister address (RA4:0) and a read-not-write (RNW) bit. The device ID is set for each chip using pins A(1:0).

Note must be taken here of the fact that in chain configuration the device ID 0b00 is not permissible. If it is set, the device acts as if it did not exist (and is permanently transparent). This makes it possible to test the deactivation of a chip without blocking the interface. Used in chain configuration, the address 0b00 addresses all iC-JXs simultaneously in a process known as broad-

casting (see page ??); the other addresses are used to select an individual chip. In chain configuration up to three devices can thus be driven on an SPI master. In bus configuration address 0b00 has no special function, making it possible to address four iC-JXs with one NCS line.

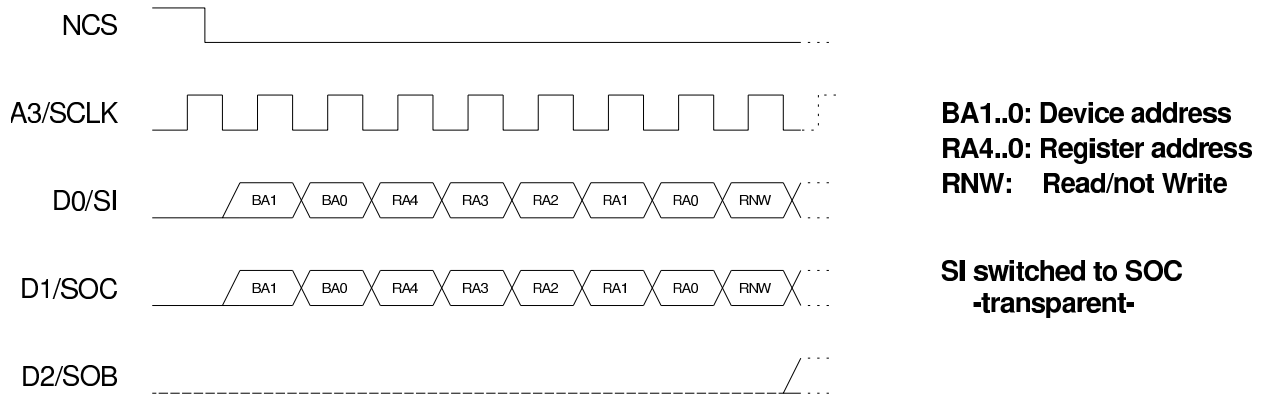


Figure 10: Addressing sequence

Reading from an iC-JX (Figure 11):

In both types of configuration one or more values can be read during a transmit cycle. The first byte sent by the controller (master) is the address the data is to be read out from. The activated iC-JX (slave) sends the address back in the next byte by way of verification

while the master sends an NOP (no operating) byte. The slave then sends the required data. The master sends the number of bytes to be read out minus one (in this case the value 0). To increase security the number byte is split into two nibbles which are encoded with the original and inverted value (0 \rightarrow 0b00001111).

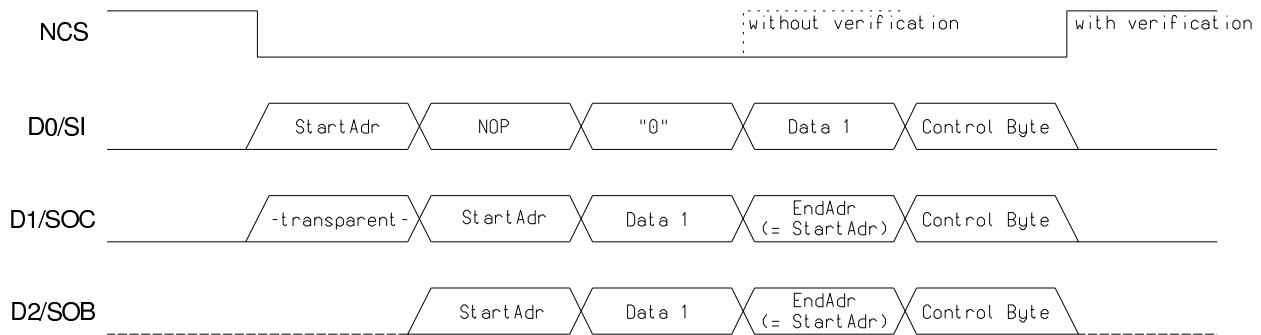


Figure 11: Reading a single register value

If verification in whatever form is dispensed with, the master can end the read cycle at this point. The master otherwise sends the received data back to the slave which then returns the address of the read register (in this instance the start address) by way of verification. If this does not match the one originally sent by the master, the master can then abort communication and repeat if necessary. If the address is correct, in the next stage of the procedure the master transmits the control byte optimized for maximum error recognition (0b01011001).

For its part the slave checks that the returned data is correct; if this is so, it then also transmits the control byte 0b01011001. In the event of error an inverted value of 0b10100110 is sent. During the transmission of this control byte the setup also checks whether the signals at SI and SOx are synchronous. If this is not the case (due to a spike occurring at SCK, for example), the slave transmits the inverted control byte as soon as it has detected the error. The master recognizes a correct transmission by the fact that the control byte has reached it without error.

If data from several consecutive registers is to be read out (see Figure 12), the autoincrement function enables an abbreviated transmission protocol to be run using iC-JX. Here the master does not send a 0 code after the address of the first register value and the NOP byte but the number of registers to be read out minus one (an entry of 1..15 results in a readout of 2..16 bytes). Here, too, the inverted value is transmitted in the second nibble of the byte. The addressed iC-JX then transmits the consecutive register values and af-

ter one byte checks the data returned from the master for errors. Once the required number of register values has been sent the slave transmits the address of the last register addressed, followed by the control byte 0b01011001 with error-free transmission or the inverted value 0b10100110 with an error in transmission. During transmission of the control byte the synchronism of the signals at SI and SOx is again checked; if these are not synchronous, on recognition of this fact the slave then transmits the inverted control byte.

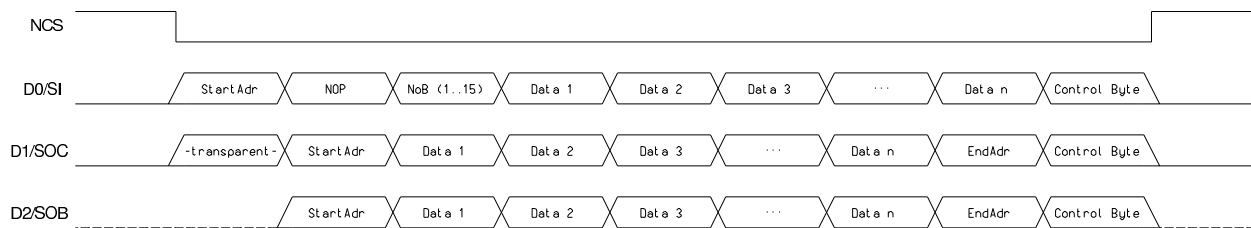


Figure 12: Reading several values of consecutive register addresses (autoincrement)

Writing to an iC-JX (Figure 13, Figure 14):

In the write process one or several registers can be written to during a transmit cycle. To this end the master first sends the start address and the numerical amount of data to be transmitted minus one. As in the read process this value is transmitted as two nibbles (non-inverted and inverted) to increase security.

Data from consecutive addresses is then sent. iC-JX returns the master data with a delay of one byte, allowing the master to constantly monitor whether an error has occurred during the addressing sequence or data transmission. If an error is detected, the master can prevent the faulty data being accepted by the slave registers by ending communication.

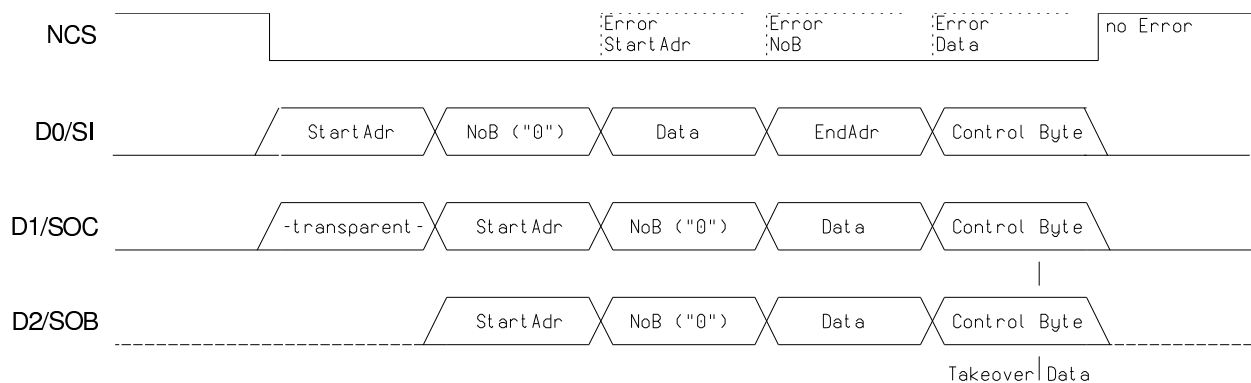


Figure 13: Writing one register value

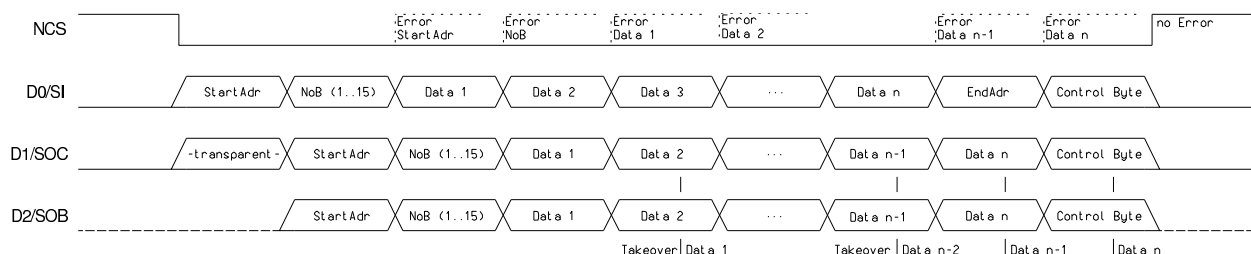


Figure 14: Writing several register values

Error handling

In order to reduce processing time complex technology, such as CRC, etc., is not used for error handling. The transmitted addresses and data are instead returned by the recipient to the sender where they are compared to the original data transmitted.

Should the master detect an error, it can abort communication in such a way so as to prevent incorrect

values being written to the slaves.

If an individually addressed slave determines that the data it has sent has been returned to it incorrectly or that the number of clock pulses is not a multiple of 8 bits, it can signal this error to the master by inverting the closing control byte.

RSET settings

iC-JX can either generate an internal reference current or permit external current settings via pin RSET. Setting the current externally is the more precise option here; to this end it is recommended that pin RSET be linked up to a 10 k Ω resistor connected to ground..

I/O stages in input mode funktion

Input registers (add. 0x00 and 0x01: reading the inputs

A high at IOx generates a high signal at bit INx. Any change to an input signal is accepted via digital filtering only after the selected filter time has expired. Here, the input comparator of each I/O stage reverses the count direction of a 3-bit counter. The counter output changes only when the final status has been reached. The counters are reset to a value of 3 by a low signal at reset input NRES. The counter is clocked externally by pin CLK or by clock ICLK, generated internally.

The scaling factor for the clock frequency and the input filter bypass can be programmed separately for all four nibbles (see control word 1, addresses 0x14 and 0x15). Switching the bypass (BYP1...4) permits operation without an external clock signal (see below).

Once the change-of-input message has been enabled in the change-of-input interrupt enable register (addresses 0x10 and 0x11) a change of level at one of the I/O pins is signaled to the microcontroller. If iC-JX is operated at the parallel interface the level at pin NINT is set to 0. If the device is operated at the serial interface a change of level is indicated by a 0 at pin SO(D1) resp SOB (D2), depending upon configuration (see SPI interfacd, page 26). The microcontroller can determine which I/O stage has had a change of input by reading out the input register.

I/O stages in output mode

Input registers (addresses 0x00 and 0x01): reading the output feedback

A high at IOx generates a high signal at INx. This allows the microcontroller to make a direct check of the switching state and, with the help of the programmable high-side current sources of 200 μ A, 600 μ A and 2 mA, to monitor the channel for any cable fractures. As with the reading of inputs the feedback signals can be output in their filtered or unfiltered state. The microcontroller can determine which I/O stage has had a change of input by reading out the input register.

Programmable Current Sources

(Adr. 0x16 und 0x17)

The programmable pull-up- resp. pull-down current sources can be set independently of the I/O mode (either input or output mode). In both modes current values of 200 μ A, 600 μ A or 2 mA are available either as

pull-up or pull down.

ADC measurements

ADC measurements: measuring current (Adr. 0x1C)

In this mode the current in each output stage can be measured. Here, the saturation voltage from an internal reference transistor is used for comparison. Each output stage has its own reference transistor in order to guarantee a precise value. The reference voltage is equivalent to the saturation voltage of the output stage transistor with a nominal current of 150 mA; the output digital value thus corresponds to the current intensity in the output stage.

To evaluate current variations in the output stage the controller must perform an initial measurement with a known reference current. Based on this value a monitoring of the load current can then be performed. The output stage thereby is selected via SELES(3:0) in control word 5 (Adr. 0x1B).

ADC measurements: measuring voltage (Adr. 0x1C)

iC-JX enables voltage at the I/O stage to be recorded. The range for voltage measured at the output stage lies between $V_B - 5$ V and V_B (bit EME = 1) and between $V_B - 0.6$ V and V_B (EME = 0). When measuring in conjunction with pull-up current sources the range lies between 0 V and 5 V (EME = 1) and between 0 V and 0.6 V (EME = 0).

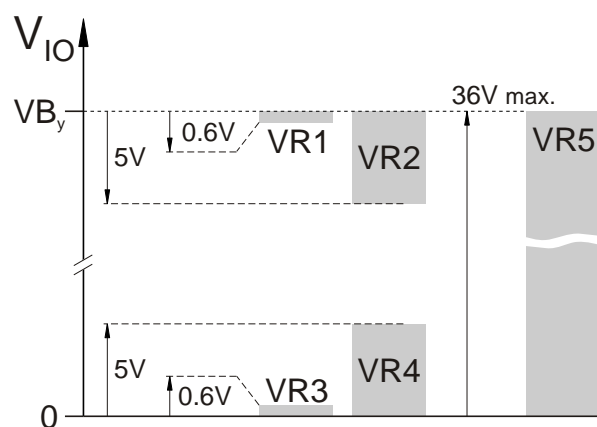


Figure 15: ADC measurement ranges

The iC-JX measures voltages at the I/O stages in different ranges. The range "Voltage Measurement High at IO" is between $V_B - 5$ V and V_B (Bit EME = 1) resp. between $V_B - 0.6$ V and V_B (EME = 0). In the mode "Voltage Measurement Low at IO" the range is between 0 and 5 V (Bit EME = 1) resp. between 0 and 0.6 V and V_B (EME = 0).

For the mode "Overall Voltage Measurement at IO" the voltage at the selected I/O stage is downscaled first by a factor of 1/15 using a resistive voltage divider to permit measurement of the full voltage range from rail to rail. The user must be aware of a input current drawn by the voltage divider of approximately $V(\text{IO})/200\text{k}\Omega$. The selection of the I/O stage is done via control word 5 (Adr. 0x1B).

ADC Measurements: VBy and VBG Measurements (Adr. 0x1C)

The internal reference voltage VBG and the external supply voltages VB1 to VB4 can also be measured. For VB1 to VB4, the voltage is downscaled first by a factor of 1/15. Selection is done via SELES (3:0) in control word 5 (Adr. 0x1B) as described in the following table.

SELES(3:0)	VB - Messung
0x0 .. 0x3	VB1
0x4 .. 0x7	VB2
0x8 .. 0xB	VB3
0xC .. 0xF	VB4

ADC Measurements: Temperature Measurement (Adr. 0x1C)

In this feature the internal chip temperature can be determined.

ADC Measurements: External Vref (Adr. 0x1C)

To improve accuracy of the A/D conversion, an external reference voltage at pin VREF can be used by setting the bit SVREF to '0b1'. The value of the external voltage reference should be about $2.5\text{V} \pm 0.2\%$.

ADC Measurements: Output

A 10 bit digital value as a result of A/D conversion is available for output currents and output voltages at a selected I/O stage, for chip temperature and supply voltages Vby and the internal bandgap voltage VBG. Except for the current measurement, the internal voltage $V(\text{VREFAD})$ (for Bit SVREF = '0') or an external voltage at pin Vref (for Bit SVREF = '1') are used as reference. The end of A/D conversion is signalled by a low signal '0' at NINT resp. D1/SOC or D2/SOB.

Output register (Adr. 0x0C und 0x0D):

Switches the various output stages on and off (for POE = 1).

Flash pulse enable (addresses 0x0E und 0x0F):

Enables flash mode

This function enables each of the various output stages to be set to flash mode, providing the value of the corresponding output register is 1. The flash frequency is derived from BLFQ or, alternatively, can be generated

from CLK or from the internally generated ICLK (via SEBLQ in control word 3B, address 0x1A). Different flash frequencies can be set for all four nibbles.

Interrupts

Interrupt readings at NINT can be triggered by a change of (filtered) input signal, by an overcurrent message signaled at an I/O pin (due to a short circuit, for example), by undervoltage at VCC or VDD, by bursts at VDD, by the end of A/D conversion or by exceeding maximum temperature thresholds (2 stages). Interrupt outputs for each individual I/O stage can be caused by a change of input, or, with stages in output mode, by a short circuit. The relevant interrupt enables determine which messages are stored and which are displayed. The display of interrupt messages caused by excessive temperature, A/D conversion, undervoltage or bursts is not maskable; this particular function is permanently enabled.

When an event occurs which is enabled to produce an interrupt message pin NINT is set to 0 when a parallel interface is used. If the device is being operated with a serial interface outputs D1/SOC or D2/SOB are set to 0 when an interrupt occurs if no communication is made via the interface itself and pin A4 ist set to '1'.

By reading out the interrupt status register (addresses 0x04 and 0x05) the nature of the message can be determined and the I/O stage causing the interrupt located. Thus with a change-of-input message the problematic I/O stage is shown in the corresponding register (addresses 0x02 and 0x03); with an overcurrent interrupt the overcurrent status register (addresses 0x06 and 0x07) pinpoints the I/O stage with a short circuit. Interrupts are deleted by simply setting EOI in control word 4 (address 0x1A). This bit then automatically resets to 0. If during operation the I/O mode is switched, i.e. from input to output mode, all interrupt messages are deleted via EOI.

To avoid interrupt messages caused by other sources in the time between the readout of a status register and the deletion of the current interrupt being overlooked successive interrupts are stored in a pipeline. If successive interrupts occur outputs NINT resp. D1/SOC or D2/SOB remain at 0 after the present interrupt has been deleted using EOI. The new interrupt source is displayed in the interrupt status register and in the specific status registers.

Overcurrent messages

If an overload occurs at one of the outputs the current in IOx is limited. In this instance an interrupt message is triggered, providing relevant interrupt enables have been set for overcurrent messages (addresses 0x12 and 0x13) and the filter time set with control word 4 (address 0x1A) has elapsed. ISCI is then set in the interrupt status register (address 0x04) and the relevant bit for the I/O stage causing the problem is set

in the overcurrent message register (addresses 0x06 and 0x07).

At addresses 0x08 and 0x09 the actual, unfiltered overcurrent status of each I/O stage can be read; a global scan of all I/O stages is also possible via bit SCS in the interrupt status register. This shows whether any of the I/O stages have overcurrent at the time of the readout. This short-circuit messaging allows permanent monitoring of the output transistors and clear allocation of error message to affected I/O stage. Filtering of the overcurrent message can be shutdown using a bypass; this bypass can be activated for all I/O stages together using BYPSCF in control word 4 (address 0x1A).

Temperature monitoring

iC-JX has a two-stage temperature monitor circuit.

Stage 1: A warning interrupt is generated if the first temperature threshold (Toff1 at ca. 132 °C) is exceeded. Suitable measures to decrease the power dissipation of the driver can be implemented using the microcontroller.

Stage 2: If the second temperature threshold is exceeded (Toff2 at ca. 152 °C), a second interrupt is generated. At the same time the output transistors and the I/O stage current sources are shutdown and the output register and flash pulse enable deleted. Once the temperature has returned to below the level of Toff1 the current sources are reactivated. The output register and flash pulse enable have to be respecified to reactivate the output stages

The interrupt status register (address 0x04) provides information as to the temperature interrupt stage but also on the current status of the temperature monitor. ET2 and ET1 statically indicate when Toff2 and Toff1 are exceeded, whereby stored interrupt messages IET2 and IET1 and the display at NINT via EOI = 1 can be deleted (control word 4, address 0x1A).

Undervoltage detection: VCC and VDD

When the supply voltage at VCC or VDD is switched on the output transistors are only released by the undervoltage detector after power-on enables VCCon or VDDon have been reached. Should the supply voltage drop to VCCoff or VDDoff during operation the I/O stages are disabled, i.e. the output transistors are turned off and the device reset. At the same time interrupt outputs are set. USD and USA in interrupt status register B (address 0x05) statically indicate undervoltage at VCC and VDD. Stored interrupt messages IUSD and IUSA and the display at NINT or SO(D1)

can be deleted by setting EOI to 1 in control word 4 (address 0x1A). Should the supply voltage then again rise to VCCon or VDDon, iC-JX assumes a reset state.

Undervoltage detection: VB1...4

In order to guarantee the fail-safe operation of connected loads voltage VB is also monitored. If the voltage drops below threshold VBoff the I/O outputs are disabled. Neither a device reset nor an interrupt message to the microcontroller are then triggered. Once voltage VB again rises above VBon the I/O outputs are re-enabled. The microcontroller can read out the status of voltage VB at bit DID1 in the device ID register (address 0x0C). In the event of error (VB < VBoff) this bit is set to 1.

Pin monitoring GNDD and GNDA

iC-JX includes a pin watchdog circuit which monitors the connection between the two ground pins GNDA and GNDD. The microcontroller can detect a possible error, such as a disconnected iC lead, for example, by reading bit IBA in the device ID register. In the event of error this is set to 1. If such a case of an error is present, then the potential of the missing ground pin is raised, which can lead to the shift of the trigger levels.

Burst detection at VDD

As in principle bursts at VDD can influence the contents of registers iC-JX monitors spikes in the supply. If any hazard is detected interrupt outputs are set to 0. Stored interrupt message ISD (interrupt status register B, address 0x05) can be deleted by setting EOI to 1 in control word 4 (address 0x1A).

Device identification

An identification code has been introduced to enable identification of iC-JX. Bit pattern 0b10101 can be read out at address 0x0D.

Reset

A reset (NRES = 0) sets the register entries to the reset values given in the tables.

Operation without the BLFQ signal

Should no clock signal be available at pin BLFQ iC-JX can generate an internal flash pulse from the external clock signal at pin CLK or from clock signal ICLK which is generated internally. For the flash frequency to be derived from the system clock pulse bit SEBLQ in control word 3B (address 0x19) must be set to 1. The flash period is then calculated by dividing by 2¹⁹.

Operation without the CLK signal

iC-JX can also be operated without a clock pulse at pin CLK. Using control word 3B (address 0x1A) the device can be set to an internally generated clock frequency; In this instance all filter functions remain fully available.

Via SECLK(1:0) in control word 3B the clocked filtering for the I/O signals and overcurrent messaging can also be deactivated. The same behavior can be obtained by setting BYP0, BYP1, BYP2 and BYP3 in control word 1 (addresses 0x14 and 0x15) together with BYPSCF in control word 4 (address 0x1A); all filters are avoided by way of a bypass circuit. Here it must be noted that interferences in the line can lead to the unwanted display of interrupts.

Forced shutdown of output stages

The output stages can be forcibly shutdown at input POE. A '1' enables logic access to the drivers; a '0' disables this. This function allows a processor-independent watchdog to lock the outputs in the event of error, for example. An integrated pull-down resistor increases safety.

DESIGN REVIEW: Notes On Chip Functions

iC-JX X2 (and previous)		
No.	Function, Parameter/Code	Description and Application Hints
1	Leakage current beyond operating conditions (Electrical Characteristics Item No. 019)	During operation, supply voltages VCC, VDD and VB1..VB4 must already be present and stable to avoid elevated leakage currents at pins IOx (x=1..16).

Table 8: Notes on chip functions regarding iC-JX chip version X2 and previous versions

iC-JX X3		
No.	Function, Parameter/Code	Description and Application Hints
1	Leakage current beyond operating conditions (Electrical Characteristics Item No. 019)	Leakage currents < 200 μ A

Table 9: Notes on chip functions regarding iC-JX version X3

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We understand suitable application of our published designs to be state-of-the-art technology which can no longer be classed as inventive under the stipulations of patent law. Our explicit application notes are to be treated only as mere examples of the many possible and extremely advantageous uses our products can be put to.

iC-JX

16-FOLD 24 V HIGH-SIDE DRIVER WITH μ C INTERFACE



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ORDERING INFORMATION

Type	Package	Order Designation
iC-JX Evaluation Board	MQFP52 -	iC-JX MQFP52 iC-JX EVAL JX2D

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