BiSS Interface

PROTOCOL DESCRIPTION (BiSS C unidirectional)

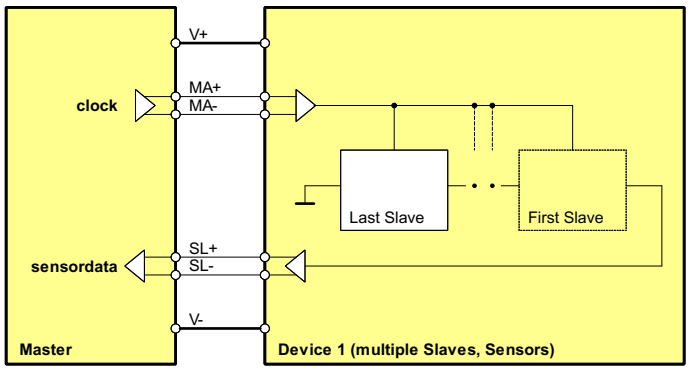
FEATURES

- Unidirectional sensor interface
- Synchronous, real-time-capable data transmission
- Fast, serial, safe
- Point-to-point or multiple slaves networks
- Compact and cost-effective
- Open standard
- Hardware compatible with SSI (Synchronous Serial Interface)
- Directly usable IP modules available

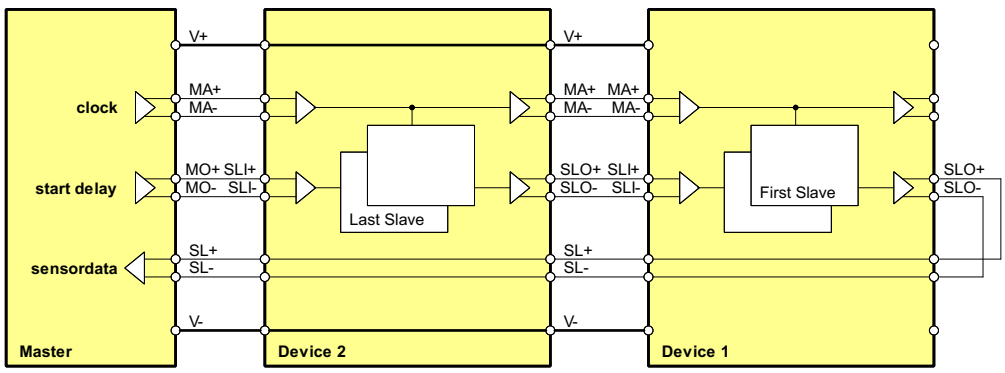
APPLICATIONS

- Driver controllers
- Smart sensors
- Safe actuators

BLOCK DIAGRAM



Sensor bus (1 Device / multiple Slaves) resp. point-to-point (Master / Device)



Sensor bus (queued Devices with multiple Slaves each)

BRIEF DESCRIPTION

This specification describes a serial interface protocol for the synchronous, fast and safe exporting of sensor data.

For more information contact iC-Haus via **www.biss-interface.com**.

In point-to-point configuration, only one device with one or more slaves (sensors) is connected to the master. The master transmits the clock signal to the slave(s) via the MA line. The SL line carries the sensor data directly from the first slave back to the master. The BiSS interface has only two unidirectional differential lines in point-to-point configuration and is hardware compatible with the SSI interface. In point-to-point configuration the input SLI of the 'Last Slave' is connected to '0'.

In bus configuration, all devices, which may also each include multiple slaves, are connected in a chain. Each slave therefore has two terminals (SLO and SLI) with drivers provided for high speed differential signals if applicable. The MA line supplies the clock signal from the master simultaneously to all slaves and the SLO and SLI lines connect the master and all slaves in a chain.

The term 'First Slave' refers to the slave whose data is transmitted to the master first. Its output SLO is directly connected to the return line to the master SL. In the bus configuration the control line MO of the master is connected to the input SLI of the 'Last Slave'. Any desired number of slaves can be connected to a BiSS C interface. All slaves can then transmit their data to the master sequentially in a single frame via several logical channels.

The data format parameters of the individual data channels, including the type of information, number of bits and CRC format, are specified for each slave in its data sheet. These transmission parameters can be pre-programmed in the controller and referenced via an ID or lookup table, or manually entered.

In addition to using a 'Full BiSS Master', which permits the connection of any desired slaves, 'Custom BiSS Masters' can operate with limited data channel parameters, and therefore only work together with one or a few slaves. This option enables implementations of BiSS masters with few resources in small FPGAs and with very little RAM.

OPERATING DESCRIPTION

The BiSS C (unidirectional) protocol enables the simultaneous transmission of sensor data (SD) from all slaves to the master.

The BiSS frame

The isochronous transmission of BiSS frames is typically used for cyclical scanning systems. Here each cycle begins with the transmission of a BiSS frame, then the interface remains in the idle state up to the beginning of the next cycle (MA = MO = SLOX = "1"). The cycle duration is therefore at least equal to the duration of a BiSS frame, and may be as long as desired.

The BiSS frame (transmission frame) is started by the master transmitting the clock on the MA line. Here the first rising edge on MA is used for the synchronization of all slaves to enable the isochronous scanning of sensor data. With the 2nd rising edge from MA, all slaves generate their "Ack" (Acknowledge) signal by setting their SLO line to "0"; it remains active (SLO = "0") until the start bit arrives at the input SLI of the respective slave. In point-to-point configuration (see Figure 1), the start bit received by the Master is generated by the last slave; it detects point-to-point configuration from the fact that its input SLI is already "0" at the start of a frame. The start bit is then passed on synchronously with the clock MA from each slave delayed by one clock pulse.

The bit following the start bit is always "0" in BiSS C unidirectional. Beginning with the 2nd bit after the start bit and up to the timeout of the BiSS frame, the data range follows, which transmits the sensor data from the slaves to the master according to the data format of the slave.

The BiSS frame ends with the BiSS timeout. In this time no further clock pulses are sent on the MA line by the master. At the end of data transmission, the master sets its output MO to the idle state "1". The slaves then pass on this "1" received at SLI to their output SLO as soon as they have detected the expiration of the timeout themselves. This ensures that the BiSS timeout on the line SL is only signalled to the master when all connected slaves have detected the timeout. When the BiSS timeout expires, all slaves return to the idle state; all lines are set to the high signal level ("1") in the process. In point-to-point configuration, the last slave signals expiry of the BiSS time-out without waiting for a predecessor. The other slaves then pass on the "1" received at SLI to their output SLO.

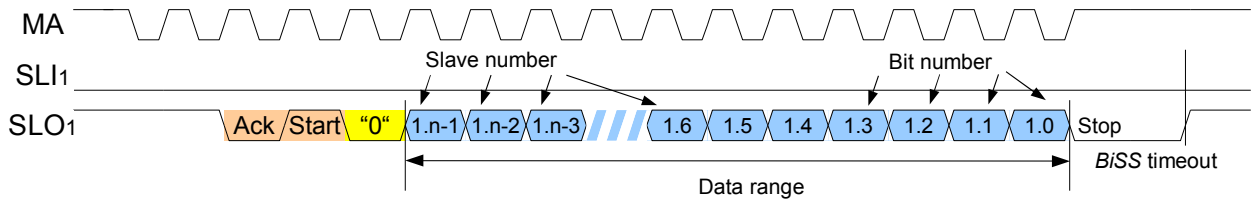


Figure 1: *BiSS* frame (point-to-point configuration)

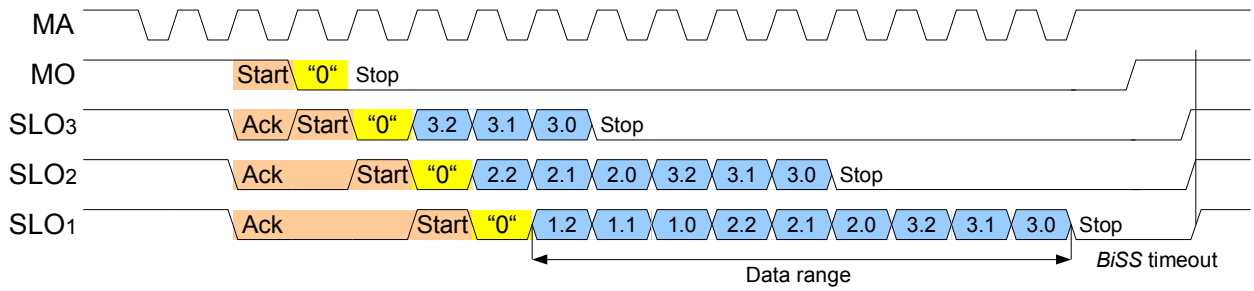


Figure 2: *BiSS* frame with 3 slaves (bus configuration)

Processing time per request
If a slave requires additional processing time before outputting its sensor data, e.g. for A/D conversion or for memory access, it can request this by delaying the start bit. The master detects the delayed start bit and generates the additionally required MA clock pulses.

If a device in point-to-point configuration consists of several slaves, then all except the last slave must temporarily save the data of their predecessor received at SLI and then send this data to SLO following their own data. The slave with the longest processing time specifies the entire processing time; it is advisable to position it as the last slave.

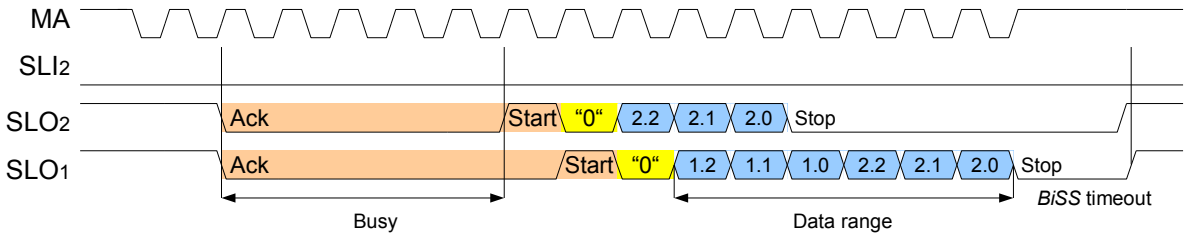


Figure 3: Requests for processing time (point-to-point configuration)

Processing time per parameter
In bus configuration, the master delays transmitting the start bit on the MO line. For this purpose, the master must be configured to the longest delay time of all connected slaves.

If the processing time required by the slave is variable, the maximum required processing time must be set. Specified times are converted by the controller into clock pulses with the currently set bus clock speed, rounded up. This setting is configured in the master.

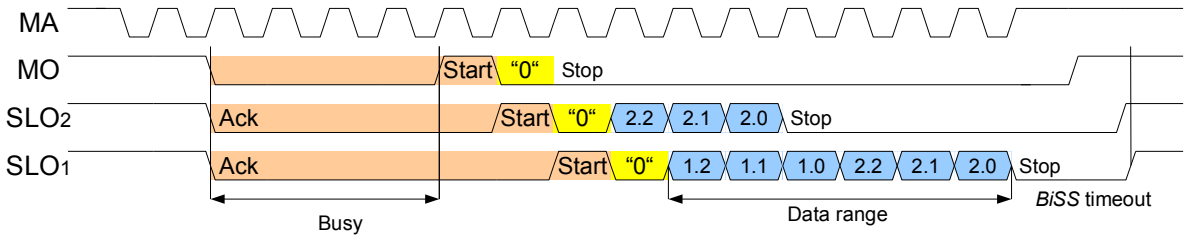


Figure 4: Parameterized processing time (bus configuration)

Line delay compensation
At high data rates, the MA line must have the same line topology and be provided with the same line drivers as the chain SLI-SLO. As a result, MA and SLI are assigned the same additional-time-dependent delay and remain synchronized. The total signal delay of the chain from the clock pulse MA to the output of the first slave (signal SL) can be measured out by the master and compensated with a corresponding shifting of the scanning of the slave signals (See Figure 5).

In addition, the data output to MO is delayed if the line delay is greater than one period. To determine the line delay, the delay from the two rising MA edges to the falling edge of the Ack bit of the slave response (SL: "Ack") is used; it is ideally zero.

The line delay compensation enables accelerated communication with high data rates of typically 10 Mbit/s. It recalculated for each BiSS frame, and therefore also takes aging and temperature-dependent drift into account.

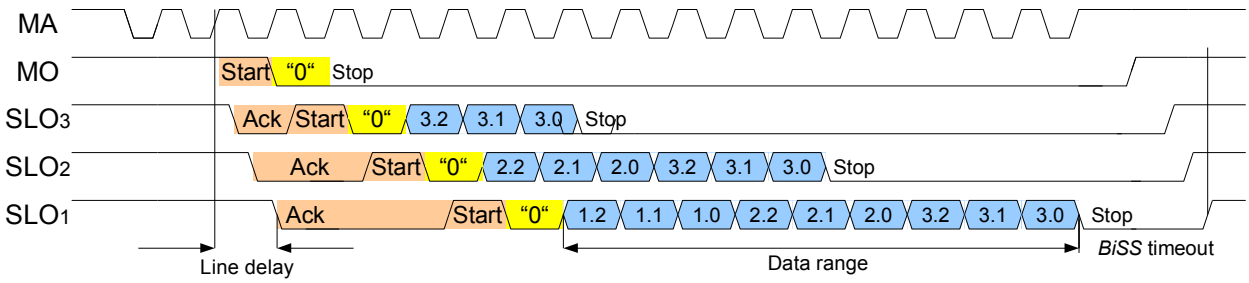


Figure 5: Line Delay compensation by the master

Bus reset
After switch-on or an error, the master must maintain a break of 40 µs prior to data transmission. This ensures that the BiSS timeout has expired and all slaves are ready. In point-to-point configuration the last slave is not defined before the first MA pulse, which also causes the SL line to remain set to zero. The master must either generate a pulse to MA or start the first cycle without taking SL into account.

SENSOR DATA COMMUNICATION

The data area
The data area is used to transmit sensor data from the slaves to the master. The entire data area is divided into logical data channels. The position and length of the individual data channels is described for each slave in its parameters. A slave can have no, one or several data channels for sensor data.

The master must be programmed with the parameters of the individual data channels in their sequence and the sequence of the connected slaves to be able to correctly assign their bits. The check bits (CRC) contained for each data channel are used to detect transmission errors and bit offsets.

The data from the first slave reaches the master directly after the "0" bit. The further data channels follow without separation by start or stop bits. The length of the data area is the sum of the length of all data channels. The slave numbering is carried out in the sequence of the data transmission, and is therefore counted in the reverse sequence of the signal direction SLI → SLO.

The slaves can only correctly signal the BiSS timeout in the BiSS frame if all SLO lines have the signal level "0" at the start of the BiSS timeout. If an error occurs, the BiSS frame can be cancelled with a timeout of 40 µs at any time.

The BiSS C unidirectional master transmits "0" on the MO line following the start bit until no further clock pulses are sent on MA. Then MO returns to its idle state ("1").

The data channels
A data channel is a logical unit used for secured data transmission and describes the related parameters and data contents. A data channel occupies a parameterized length in the data area of the BiSS frame and in the memory of the master (number of data and CRC bits).

The data sheet details the parameters necessary for secured data transmission and the description of the data contents. The controller must be configured in accordance with these parameters.

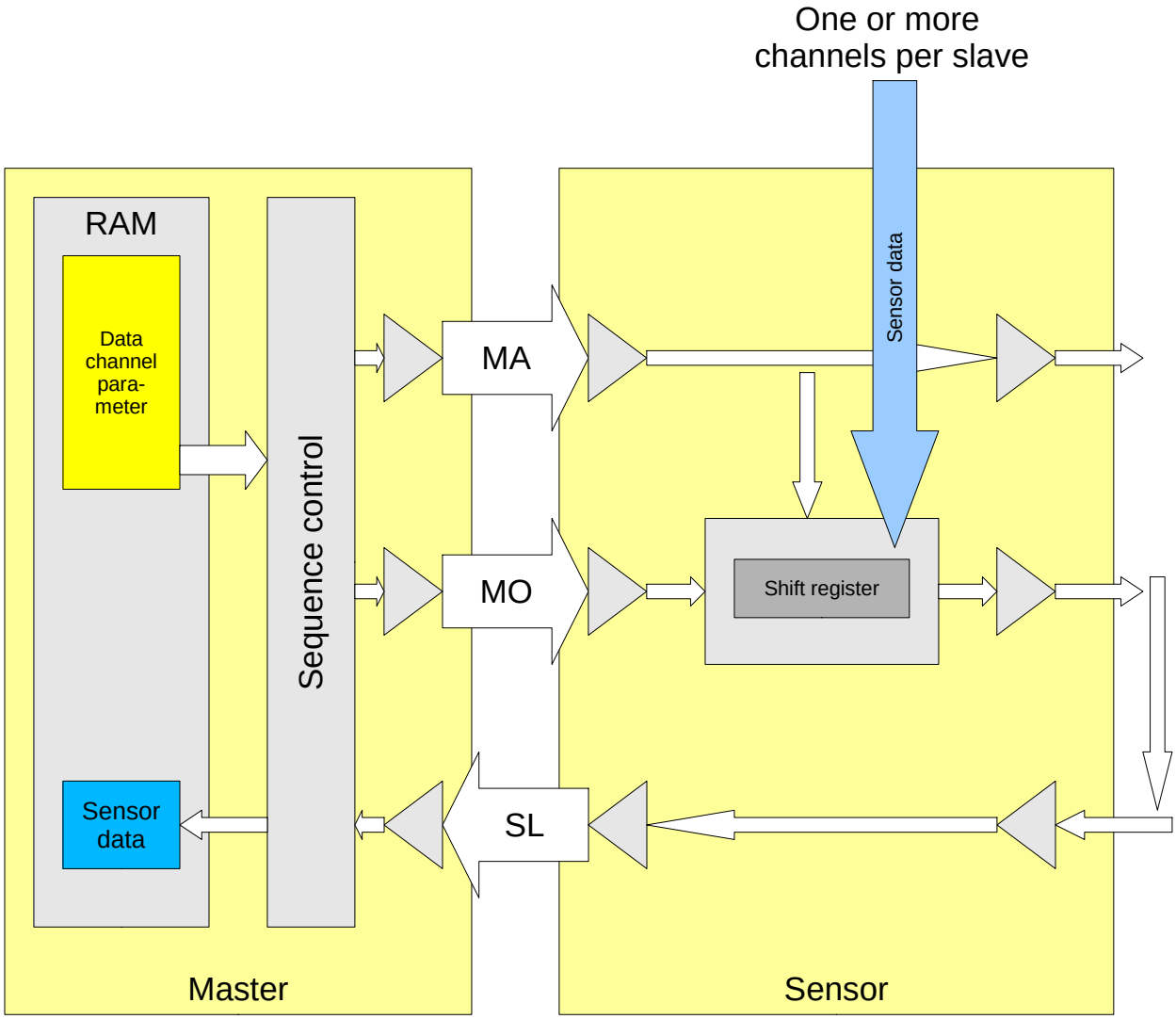


Figure 6: Configuration and transmission of sensor data

The data channel parameters
The following parameters are defined for data channels:

- Number of bits (1. . . 64)
- Processing time (0 µs. . . t_{busy_s})
- Data alignment (left or right-justified)
- CRC polynomial (for 0. . . 8 CRC bits)

Processing time for single-cycle data
The processing time begins simultaneously in all slaves with the first rising edge of MA. In the parameters the processing time is either specified as a time unit or in MA clock pulses; a dependency on the frame length is permissible. The maximum processing time is t_{busy_s} (see Characteristics, below).

The data values
All data values are transmitted with the most significant bit first ("MSB first"). A data value itself can consist of several bit groups, e.g. a measured value and several error flags.

The composition and alignment of the data values are defined in the data sheet of the slave. Figure 7 shows data alignment with a data length of 13 bits, stored in a 16-bit wide word in the master.

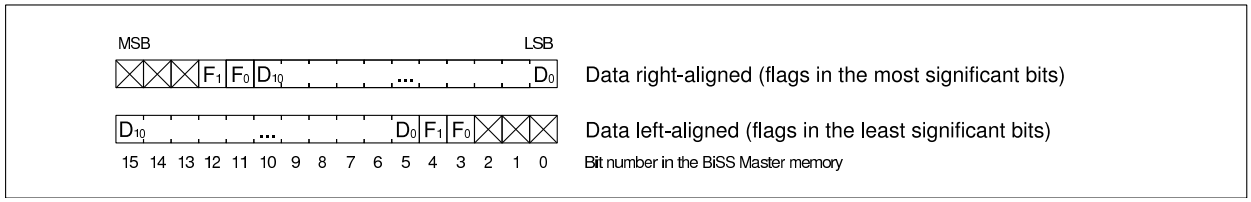


Figure 7: Alignment of data values

Invalid values
It is recommended that the data value zero ("0") be reserved as invalid for the detection of an incorrectly configured transmission direction of a data channel for single-cycle data. The master also transmits the data value zero if no new data are available for an actuator data channel at the start of the BiSS frame. Usually, the value zero ("0") is avoided in the valid data by using at least one bit of the data value as a "0"-active error bit.

CRC transmission checking
Each data channel include a CRC in addition to its data value. The properties of the CRC are specified in the parameters of the data channel. The CRC polynomial also indicates the transmitted CRC bits; 0 to 8 bits are possible. The CRC bits are always transmitted inverted, and with the most significant bit first.

If other checking methods are used to protect a data channel, or if the maximum number of bits is not sufficient for a CRC, then the CRC is deactivated (CRC polynomial = 0). The check bits are then transmitted within the (maximum of 64 bits per data channel) normal data bits and stored in the memory of the master. The check bits can now be checked with software.

CHARACTERISTICS

Nr.	Symbol	Parameter	Condition	Min.	Max.	Unit
01	$1/T_{MA}$	Clock frequency	signal MA	80	[1]	kHz
02	$1/T_{MAmin}$	Minimum clock frequency	signal MA, all slave supported clock frequency	80	10000	kHz
03	t_{MAl}	Clock signal low level duration	MA = "0"	[1]	12.5	µs
04	t_{MAh}	Clock signal high level duration	MA = "1"	[1]	12.5	µs
05	$t_{BiSS\text{-}Timeout}$	*BiSS* timeout		12.5 [2]	40	µs
06	$t_{BiSS\text{-}Timeout\_a}$	Adaptive *BiSS*-Timeout for slaves with automatic *BiSS*-Timeouts adaption on T_{MA} sampling frequency: $1/T_{CLK}$	$T_{CLK} \leq 1.5 \cdot T_{MA}$ $T_{CLK} \geq 1.5 \cdot T_{MA}$	$1.5 \cdot T_{MA}$ $1.0 \cdot T_{CLK}$	$1.5 \cdot T_{MA} + 3.0 \cdot T_{CLK}$ $1.5 \cdot T_{MA} + 3.0 \cdot T_{CLK}$	
07	$t_{LineDelay}$	Delay MA → SL	Measurable within a *BiSS*-Frame from the second rising MA edge to the first falling SL edge	0	40	µs
08	$t_{LineJitter}$	Delay jitter MA → SL	within a *BiSS* frames	-25	25	$\%T_{MA}$
09	t_{busy_s}	Processing time for single cycle data		0	40	µs

[1] The maximum clock-pulse rate is dependent on the transmission medium (see BiSS Interface - Physical Layer) and on the individual devices. The maximum clock-pulse rate is, among other things, defined by the device datasheet.
[2] The Min column is obsolete after automatic bit rate detection or for custom *BiSS* C unidirectional slaves. An insufficiant timeout can only be detected as a general communication error.

Table 1: Table of characteristic

TERMS AND ABBREVIATIONS

Term	Meaning
Bus establishment	Detecting all slaves including parameterizing and error handling.
Master	Interface device between *BiSS* C unidirectional bus and control.
Device	Physical unit. Contains one or multiple slaves.
Slave	Logic unit within a device. Occupies one single ID and uses none, one or multiple data channel.
BiSS-Frame	Cyclically executed and carries single cycle data completely and one bit at a time of register data.
BiSS-Timeout	Timeout give by the connected slaves. Separates following *BiSS* frames.
"First slave"	The slave with the data which are transmitted first with the *BiSS* frame.
"Last slave"	The slave with the data which are transmitted last with the *BiSS* frame.
Data area	The bits in the *BiSS* frame which the data channels transmit.
Data channel	A logical channel which contains the data and check bits of a data value and is parameterized as such.
Data value	A value which is transmitted protected. It can contain additional bits and bit groups, however is treated by the *BiSS* master as a number.
Register bank	A switchable area of 64 registers in which registers or memory of the slave can be displayed.
Controller	The controller is the higher-ranking logic of the *BiSS* master. This is usually understood to be the processor which controls the *BiSS* master and the software running on it.
Big Endian	Byte sequence with which the highest-value byte is saved at the lowest-value address.

Table 2: Table of terms

Abbreviation	Meaning	Description
SCD	Single-Cycle Data	A value transmitted completely in one *BiSS* frame.
DCH	Data Channel	Logical unit used for secured data transmission.
SLI	Slave In	Data input of the *BiSS* C unidirectional slave.
SLO	Slave Out	Data output of the *BiSS* C unidirectional slave.
MO	Master Out	Data output of the *BiSS* C unidirectional master.
MA	Master Clock	Clock pulse output of the *BiSS* C unidirectional master.
SL	Slave return	Data input of the *BiSS* C unidirectional master.
EDS	Electronic Data Sheet	Electronic Data Sheet.
XML	eXtensible Markup Language	A language for describing documents.
CRC	Cyclic Redundancy Check	Procedure for transmission checking.
MSB	Most Significant Bit	Highest-value bit
LSB	Least Significant Bit	Lowest-value bit

Table 3: Table of abbreviations